

Data sheet acquired from Harris Semiconductor SCHS035C – Revised September 2003

CMOS Quad Exclusive-OR Gate

High-Voltage Types (20-Volt Rating)

■ CD4030B types consist of four independent Exclusive-OR gates. The CD4030B provides the system designer with a means for direct implementation of the Exclusive-

The CD4030B types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (VDD)

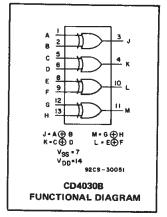
CD4030B Types

Features:

- Medium-speed operation—tpHL, tpLH = 65 ns (typ.) at $V_{DD} = 10 \text{ V, C}_{L} = 50 \text{ pF}$
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 µA at 18 V over full packagetemperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range):

1 V at V_{DD} = 5 V 2 V at V_{DD} = 10 V 2.5 V at V_{DD} = 15 V

■ Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"



Applications:

- Even and odd-parity generators and checkers
- Logical comparators
- Adders/subtractors
- General logic functions

DC INPUT CURRENT, ANY ONE INPUT ±10mA POWER DISSIPATION PER PACKAGE (PD): For T_A = +100°C to +125°C...... Derate Linearity at 12mW/°C to 200mW

Voltages referenced to VSS Terminal)-0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS-0.5V to V_{DD} +0.5V

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

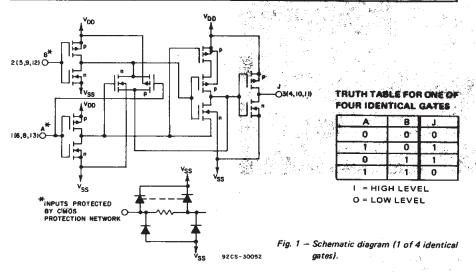
FOR TA = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW OPERATING-TEMPERATURE RANGE (TA).....-55°C to +125°C STORAGE TEMPERATURE RANGE (T_{stg}).....-65°C to +150°C LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max +265°C

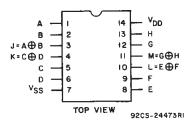
RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIM			
CHARACTERISTIC	MIN.	MAX.	UNITS	
Supply-Voltage Range (For T _A = Full Package: Temperature Range)	3.	18	V	



TERMINAL DIAGRAM Top View



CD4030B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARAC-	CONI	OITIO	NS	LIMITS AT INDICATED TEMPERATURES (°C)							
TERISTIC	v _o	VIN	v_{DD}						+25	,	T
	(V)	(V)	(V)	-55	-40	+85	+125	Min.	Тур.	Max.	S
Quiescent		0,5	5	0.25	0.25	7.5	7.5		0.01	0.25	
Device	_	0,10	10	0.5	0.5	15	15	-	0.01	0.5	μ
Current, I _{DD}		0,15	15	1	1	30	30	-	0.01	1	
Max.	-	0,20	20	5	5	150	150	_	0.02	5	
Output Low (Sink)	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	_	
Current	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	_	
I _{OL} Min.	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	_	
Output High (Source) Current, IOH Min.	4.6	0,5	5	-0.64	-0.61	0.42	-0.36	-0.51	-1	-	'n
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	_	ŀ
	9.5	0,10	10	-1.6	1.5	-1.1	-0.9	-1.3	-2.6		1
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8		1
Output Voltage:	_	0,5	5		0	.05	_	0	0.05	Γ	
Low-Level,		0,10	10		0	.05	_		0.05]	
VOL Max.	-	0,15	15		0	.05	-	0	0.05],	
Output Voltage:	_	0,5	5		4	.95	4.95	5		1	
High-Level,	_	0,10	10		9	.95		9.95	10	_	1
V _{OH} Min.	_	0,15	15		14	.95		14.95	15	-	1
Input Low	0.5,4.5	ı	5		1	.5		_	_	1.5	
Voltage,	1,9	-	10			3		_	-	3	
V _{IL} Max.	1.5,13.5	-	15			4		-	_	4	١,
Input High	0.5,4.5	_	5			3.5		3.5	_	_]
Voltage,	1,9	_	10			7	J	. 7		-	
V _{1H} Min.	1.5,13.5	_	15			11		11	_		
Input Current IN Max.	_	0,18	18	±0.1	±0.1	±1	±1	_	±10 ⁻⁵	±0.1	4

DYNAMIC ELECTRICAL CHARACTERISTICS at T $_A$ = 25°C; Input t $_r$, t $_f$ = 20 ns, C $_L$ = 50 pF, R $_L$ = 200 K Ω

	CONDITIONS						
CHARACTERISTIC	V _{DD}	LIM	UNITS				
		(V)	Тур.	Max.			
Propagation Delay Time,	-	5	140	280			
	tPLH, tPHL	10	65	130	ns		
		15	50	100			
		5	100	200	ns		
Transition Time,	^t THL ^{, t} TLH	10	50	100			
		15	40	80			
Input Capacitance,	CIN	Any Input	5	7.5	ρF		

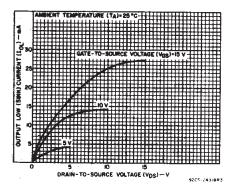


Fig. 2 — Typical output low (sink) current characteristics.

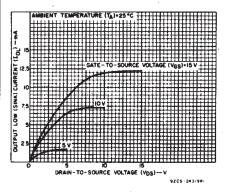


Fig. 3 – Minimum output low (sink) current characteristics.

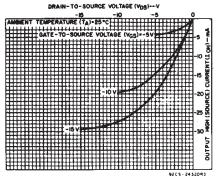


Fig. 4 — Typical output high (source) current characteristics.

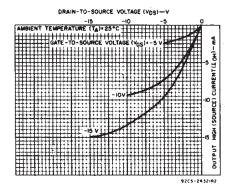


Fig. 5 – Minimum output high (source) current characteristics.

CD4030B Types

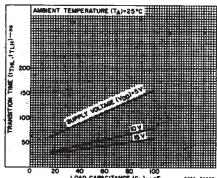


Fig. 6 — Typical transition time as a function of load capacitance.

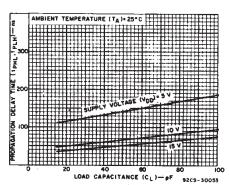


Fig. 7 — Typical propagation delay time as a function of load capacitance.

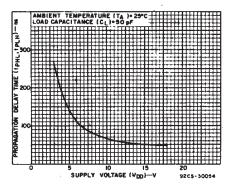


Fig. 8 — Typical propagation delay time as a function of supply voltage.

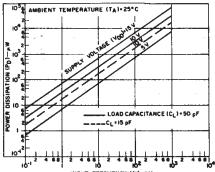


Fig. 9 — Typical dynamic power dissipation as a function of input frequency.

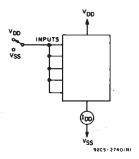


Fig. 10 - Quiescent-device current test circuit.

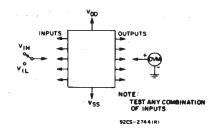


Fig. 11 — Input-voltage test circuit.

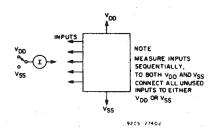


Fig. 12 - Input-current test circuit.

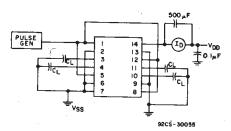
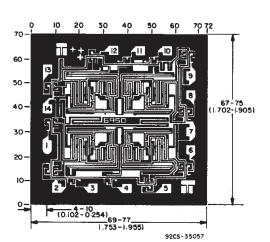


Fig. 13 – Dynamic power dissipation test circuit.



Dimensions and pad layout for CD4030BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).



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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
CD4030BE	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD4030BEE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD4030BF	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
CD4030BF3A	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
CD4030BM	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4030BM96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4030BM96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4030BM96G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4030BME4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4030BMG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4030BMT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4030BMTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4030BMTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4030BNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4030BNSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4030BNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4030BPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4030BPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	



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Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
CD4030BPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4030BPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4030BPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD4030BPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
JM38510/05353BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
M38510/05353BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF CD4030B, CD4030B-MIL:





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• Military: CD4030B-MIL

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

All ulmensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4030BM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4030BMT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4030BNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4030BPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

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*All dimensions are nominal

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4030BM96	SOIC	D	14	2500	346.0	346.0	33.0
CD4030BMT	SOIC	D	14	250	346.0	346.0	33.0
CD4030BNSR	SO	NS	14	2000	346.0	346.0	33.0
CD4030BPWR	TSSOP	PW	14	2000	346.0	346.0	29.0

14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
 - Sody length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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