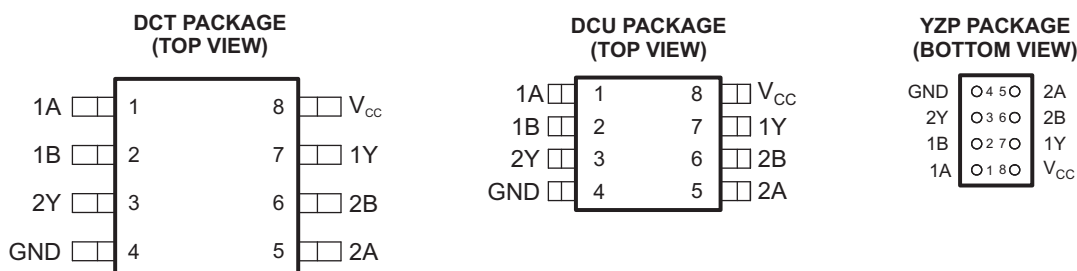


FEATURES

- Available in Texas Instruments NanoFree™ Package
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 5.3 ns at 3.3 V
- Low Power Consumption, 10- μ A Max I_{CC}
- ± 24 -mA Output Drive at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

This dual 2-input NAND gate with Schmitt-trigger inputs is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC2G132 contains two inverters and performs the Boolean function $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic. The device functions as two independent inverters, but because of Schmitt action, it has different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device can be triggered from the slowest of input ramps and still give clean jitter-free output signals.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

| T_A | PACKAGE ⁽¹⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING ⁽²⁾ |
|---------------|--|--------------|-----------------------|---------------------------------|
| -40°C to 85°C | NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free) | Reel of 3000 | SN74LVC2G132YZPR | __ _D5_ |
| | SSOP – DCT | Reel of 3000 | SN74LVC2G132DCTR | C3B_ _ _ |
| | VSSOP – DCU | Reel of 3000 | SN74LVC2G132DCUR | C3B_ |
| | | Reel of 250 | SN74LVC2G132DCUT | |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

(2) DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.
DCU: The actual top-side marking has one additional character that designates the assembly/test site.

YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

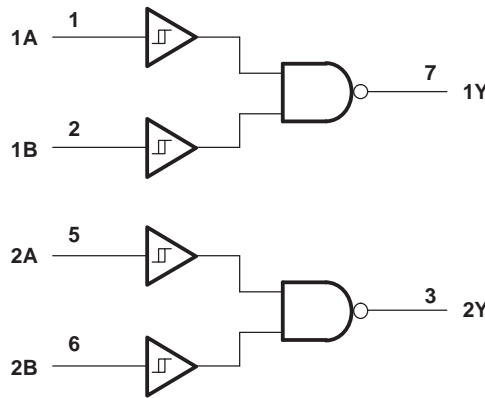
SN74LVC2G132
DUAL 2-INPUT NAND GATE
WITH SCHMITT-TRIGGER INPUTS

SCES547C—FEBRUARY 2004—REVISED JANUARY 2007

FUNCTION TABLE
(EACH GATE)

| INPUTS | | OUTPUT Y |
|--------|---|-------------|
| A | B | |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---------------|---|-------------|----------------|------|
| V_{CC} | Supply voltage range | -0.5 | 6.5 | V |
| V_I | Input voltage range ⁽²⁾ | -0.5 | 6.5 | V |
| V_O | Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾ | -0.5 | 6.5 | V |
| V_O | Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾ | -0.5 | $V_{CC} + 0.5$ | V |
| I_{IK} | Input clamp current | $V_I < 0$ | -50 | mA |
| I_{OK} | Output clamp current | $V_O < 0$ | -50 | mA |
| I_O | Continuous output current | | ±50 | mA |
| | Continuous current through V_{CC} or GND | | ±100 | mA |
| θ_{JA} | Package thermal impedance ⁽⁴⁾ | DCT package | 220 | °C/W |
| | | DCU package | 227 | |
| | | YZP package | 102 | |
| T_{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7

Recommended Operating Conditions⁽¹⁾

| | | MIN | MAX | UNIT | |
|-----------------|--------------------------------|--------------------------|-----------------|------|----|
| V _{CC} | Supply voltage | Operating | 1.65 | 5.5 | V |
| | | Data retention only | 1.5 | | |
| V _I | Input voltage | 0 | 5.5 | V | |
| V _O | Output voltage | 0 | V _{CC} | V | |
| I _{OH} | High-level output current | V _{CC} = 1.65 V | | -4 | mA |
| | | V _{CC} = 2.3 V | | -8 | |
| | | V _{CC} = 3 V | | -16 | |
| | | V _{CC} = 4.5 V | | -24 | |
| I _{OL} | Low-level output current | V _{CC} = 1.65 V | | 4 | mA |
| | | V _{CC} = 2.3 V | | 8 | |
| | | V _{CC} = 3 V | | 16 | |
| | | V _{CC} = 4.5 V | | 24 | |
| T _A | Operating free-air temperature | -40 | 85 | °C | |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74LVC2G132
DUAL 2-INPUT NAND GATE
WITH SCHMITT-TRIGGER INPUTS

SCES547C—FEBRUARY 2004—REVISED JANUARY 2007

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|---|---------------------------|--|-----------------------|--------------------|------|------|
| V _{T+} Positive-going input threshold voltage | | 1.65 V | 0.79 | | 1.16 | V |
| | | 2.3 V | 1.11 | | 1.56 | |
| | | 3 V | 1.5 | | 1.87 | |
| | | 4.5 V | 2.16 | | 2.74 | |
| | | 5.5 V | 2.61 | | 3.33 | |
| V _{T-} Negative-going input threshold voltage | | 1.65 V | 0.39 | | 0.62 | V |
| | | 2.3 V | 0.58 | | 0.87 | |
| | | 3 V | 0.84 | | 1.14 | |
| | | 4.5 V | 1.41 | | 1.79 | |
| | | 5.5 V | 1.87 | | 2.29 | |
| ΔV _T Hysteresis (V _{T+} - V _{T-}) | | 1.65 V | 0.37 | | 0.62 | V |
| | | 2.3 V | 0.48 | | 0.77 | |
| | | 3 V | 0.56 | | 0.87 | |
| | | 4.5 V | 0.71 | | 1.04 | |
| | | 5.5 V | 0.71 | | 1.11 | |
| V _{OH} | I _{OH} = -100 μA | 1.65 V to 5.5 V | V _{CC} - 0.1 | | | V |
| | I _{OH} = -4 mA | 1.65 V | 1.2 | | | |
| | I _{OH} = -8 mA | 2.3 V | 1.9 | | | |
| | I _{OH} = -16 mA | 3 V | 2.4 | | | |
| | I _{OH} = -24 mA | | 2.3 | | | |
| | I _{OH} = -32 mA | 4.5 V | 3.8 | | | |
| V _{OL} | I _{OL} = 100 μA | 1.65 V to 5.5 V | | | 0.1 | V |
| | I _{OL} = 4 mA | 1.65 V | | | 0.45 | |
| | I _{OL} = 8 mA | 2.3 V | | | 0.3 | |
| | I _{OL} = 16 mA | 3 V | | | 0.4 | |
| | I _{OL} = 24 mA | | | | 0.55 | |
| | I _{OL} = 32 mA | 4.5 V | | | 0.55 | |
| I _I | A or B inputs | V _I = 5.5 V or GND | 1.65 V to 5.5 V | | ±1 | μA |
| I _{off} | | V _I or V _O = 5.5 V | 0 | | ±10 | μA |
| I _{CC} | | V _I = V _{CC} or GND, I _O = 0 | 1.65 V to 5.5 V | | 10 | μA |
| ΔI _{CC} | | One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND | 3 V to 5.5 V | | 500 | μA |
| C _I | | V _I = V _{CC} or GND | 3.3 V | | 3.5 | pF |

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 15$ pF (unless otherwise noted) (see [Figure 1](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$ | | $V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$ | | $V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$ | | $V_{CC} = 5\text{ V}$ $\pm 0.5\text{ V}$ | | UNIT |
|-----------|-----------------|----------------|--|-----|---|-----|---|-----|---|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_{pd} | A or B | Y | 4 | 16 | 2.5 | 7 | 2 | 5.3 | 1.5 | 4.4 | ns |

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30$ pF or 50 pF (unless otherwise noted) (see [Figure 2](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$ | | $V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$ | | $V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$ | | $V_{CC} = 5\text{ V}$ $\pm 0.5\text{ V}$ | | UNIT |
|-----------|-----------------|----------------|--|-----|---|-----|---|-----|---|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_{pd} | A or B | Y | 4 | 16 | 3 | 7.5 | 2 | 6 | 2 | 5 | ns |

Operating Characteristics

$T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | $V_{CC} = 1.8\text{ V}$ | $V_{CC} = 2.5\text{ V}$ | $V_{CC} = 3.3\text{ V}$ | $V_{CC} = 5\text{ V}$ | UNIT |
|-----------|-------------------------------|---------------------|-------------------------|-------------------------|-------------------------|-----------------------|------|
| | | | TYP | TYP | TYP | TYP | |
| C_{pd} | Power dissipation capacitance | $f = 10\text{ MHz}$ | 17 | 18 | 18 | 20 | pF |

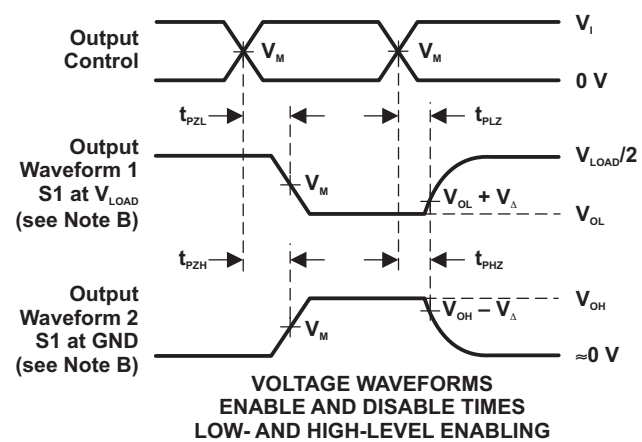
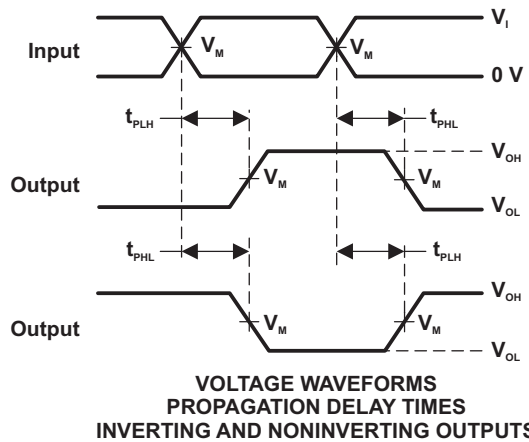
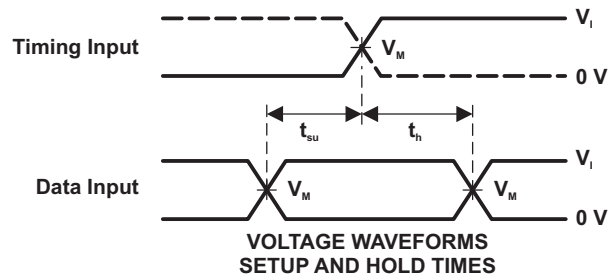
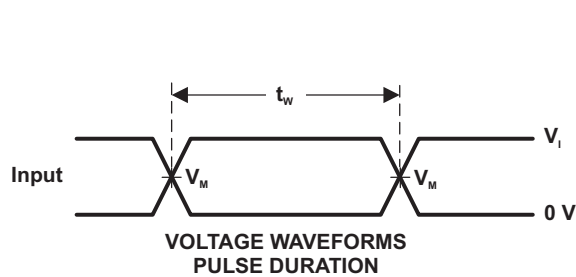
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

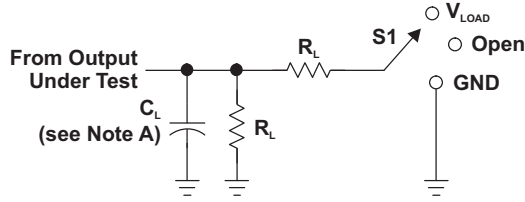
| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
| | V_I | t/t_i | | | | | |
| $1.8\text{ V} \pm 0.15\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M Ω | 0.15 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | 3 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 15 pF | 1 M Ω | 0.3 V |
| $5\text{ V} \pm 0.5\text{ V}$ | V_{CC} | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M Ω | 0.3 V |



- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_o = 50\ \Omega$.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
F. t_{PZL} and t_{PZH} are the same as t_{en} .
G. t_{PLH} and t_{PHL} are the same as t_{pd} .
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

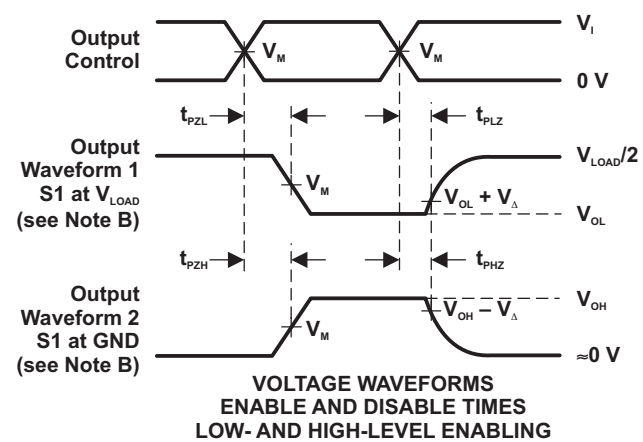
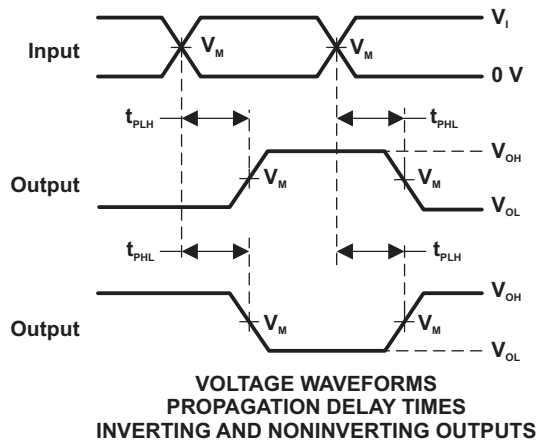
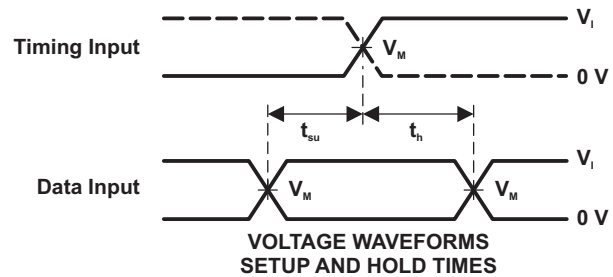
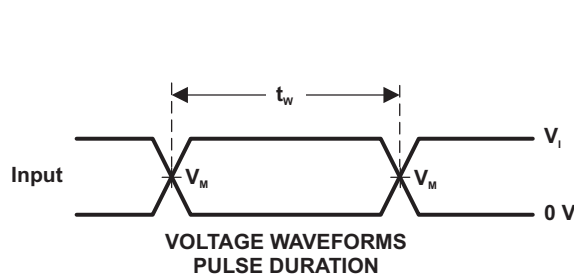
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
| | V_I | t/t_i | | | | | |
| $1.8\text{ V} \pm 0.15\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | 3 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| $5\text{ V} \pm 0.5\text{ V}$ | V_{CC} | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 Ω | 0.3 V |



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_o = 50\ \Omega$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{on} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|----------------------|------------------------------|-----------------------------|
| 74LVC2G132DCTRE4 | ACTIVE | SM8 | DCT | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| 74LVC2G132DCTRG4 | ACTIVE | SM8 | DCT | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| 74LVC2G132DCURE4 | ACTIVE | US8 | DCU | 8 | | TBD | Call TI | Call TI | |
| 74LVC2G132DCURG4 | ACTIVE | US8 | DCU | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| 74LVC2G132DCUTE4 | ACTIVE | US8 | DCU | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVC2G132DCTR | ACTIVE | SM8 | DCT | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVC2G132DCUR | ACTIVE | US8 | DCU | 8 | 3000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | |
| SN74LVC2G132DCUT | ACTIVE | US8 | DCU | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVC2G132YZPR | ACTIVE | DSBGA | YZP | 8 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC2G132DCUR | US8 | DCU | 8 | 3000 | 180.0 | 9.0 | 2.05 | 3.3 | 1.0 | 4.0 | 8.0 | Q3 |
| SN74LVC2G132DCUR | US8 | DCU | 8 | 3000 | 180.0 | 8.4 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| SN74LVC2G132YZPR | DSBGA | YZP | 8 | 3000 | 180.0 | 8.4 | 1.02 | 2.02 | 0.63 | 4.0 | 8.0 | Q1 |

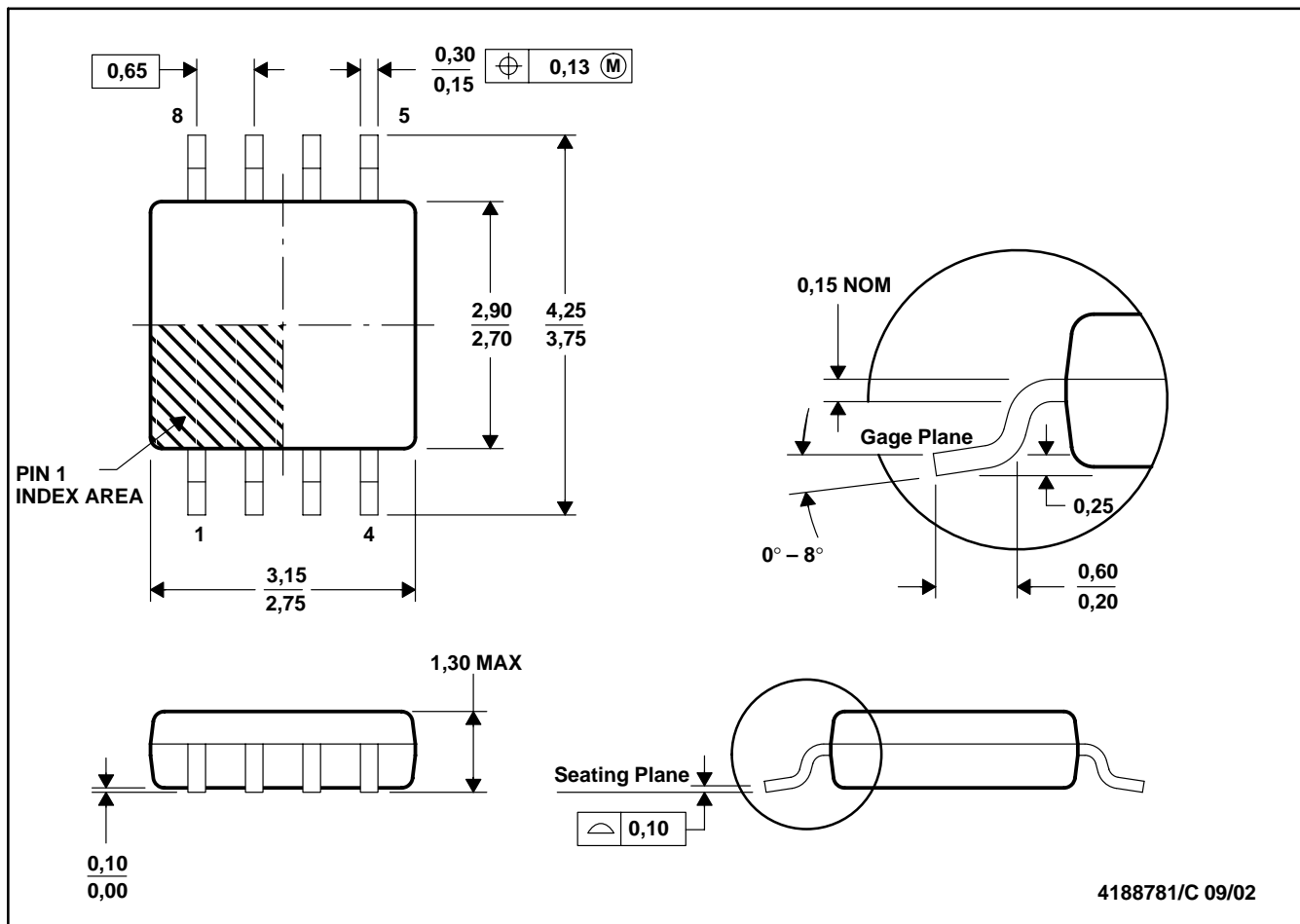
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC2G132DCUR | US8 | DCU | 8 | 3000 | 182.0 | 182.0 | 20.0 |
| SN74LVC2G132DCUR | US8 | DCU | 8 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74LVC2G132YZPR | DSBGA | YZP | 8 | 3000 | 220.0 | 220.0 | 34.0 |

DCT (R-PDSO-G8)

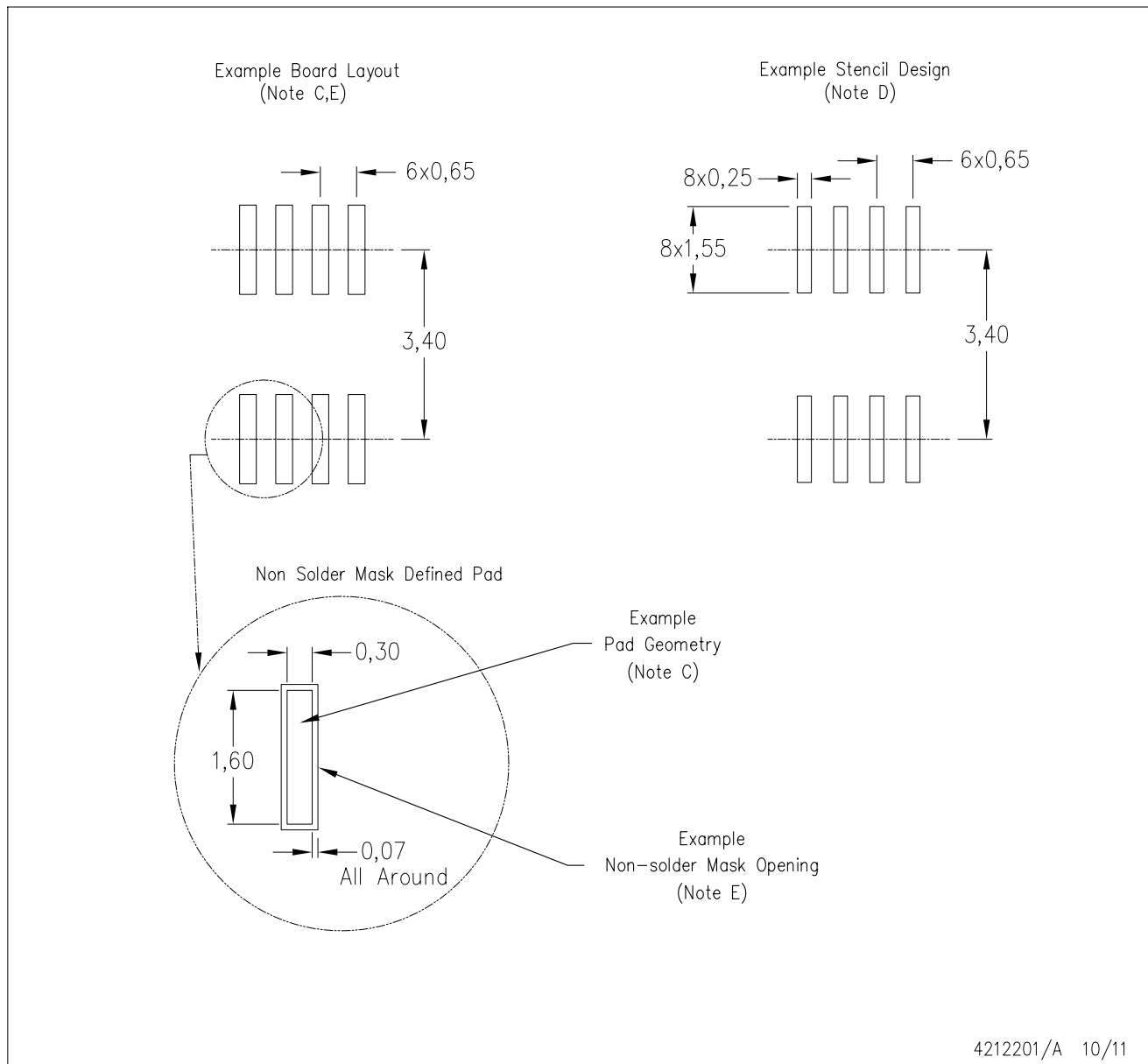
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion
 - D. Falls within JEDEC MO-187 variation DA.

DCT (R-PDSO-G8)

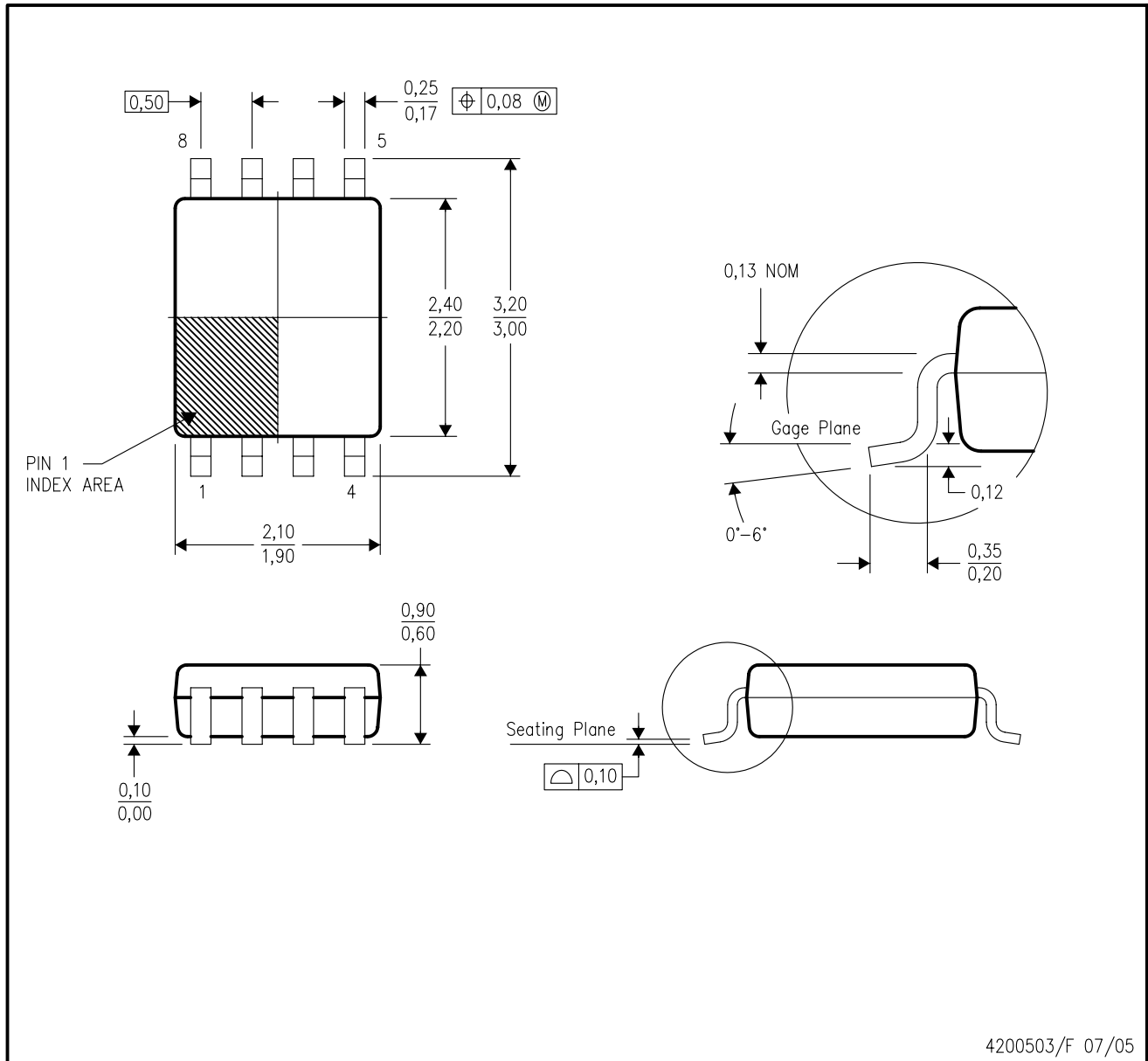
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DCU (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-187 variation CA.

DCU (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)

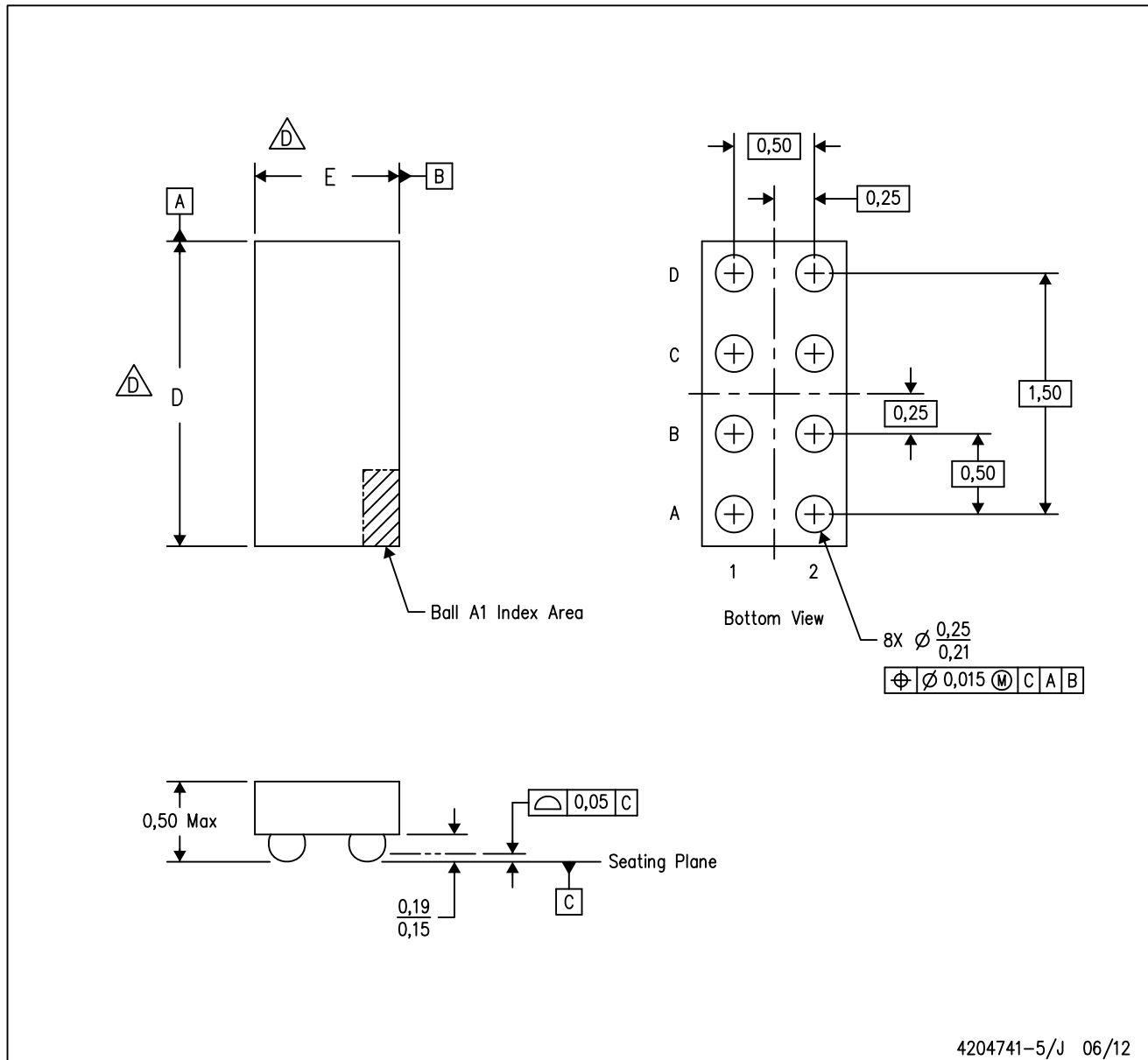


4210064/C 04/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

YZP (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - \triangle The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
 - E. This package is a Pb-free solder ball design. Refer to the 8 YEP package (drawing 4204725) for tin-lead (SnPb).

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