CD54AC02, CD74AC02 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

SCHS304C - JANUARY 2001 - REVISED JUNE 2002

- AC Types Feature 1.5-V to 5.5-V Operation and Balanced Noise Immunity at 30% of the Supply Voltage
- Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption
- Balanced Propagation Delays
- ±24-mA Output Drive Current
 Fanout to 15 F Devices
- SCR-Latchup-Resistant CMOS Process and Circuit Design
- Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015

CD54AC02...F PACKAGE CD74AC02...E OR M PACKAGE (TOP VIEW) 14 VCC 1Y 1A [13**∏** 4Y 1B 🛮 3 12 4B 2Y 🛮 11 🛮 4A 2A 10 3Y 2B [6 9 🛮 3B 8[] 3A GND [] 7

description

The 'AC02 devices contain four independent 2-input NOR gates that perform the Boolean function $Y = \overline{A} \cdot \overline{B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

ORDERING INFORMATION

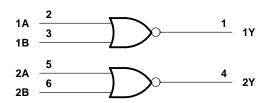
| TA | PAC | KAGET | PART NUMBER MARKI CD74AC02E CD74AC0 CD74AC02M AC02M | | |
|----------------|----------|---------------|---|-------------|--|
| | PDIP – E | Tube | CD74AC02E | CD74AC02E | |
| –55°C to 125°C | SOIC - M | Tube | CD74AC02M | A COOM | |
| -55 0 10 125 0 | | Tape and reel | CD74AC02M96 | ACUZIVI | |
| | CDIP – F | Tube | CD54AC02F3A | CD54AC02F3A | |

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each gate)

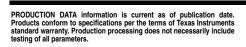
| INP | JTS | OUTPUT |
|-----|-----|--------|
| Α | В | Y |
| Н | Χ | L |
| Х | Н | L |
| L | L | Н |

logic diagram (positive logic)





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| Supply voltage range, V _{CC} | 0.5 V to 6 V |
|--|----------------|
| Input clamp current, $I_{ K }(V_{ } < 0 \text{ or } V_{ } > V_{CC})$ (see Note 1) | ±20 mA |
| Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC}) (see Note 1) | ±50 mA |
| Continuous output current, I _O (V _O = 0 to V _{CC}) | ±50 mA |
| Continuous current through V _{CC} or GND | ±100 mA |
| Package thermal impedance, θ_{JA} (see Note 2): E package | 80°C/W |
| M package | 86°C/W |
| Storage temperature range, T _{sto} | -65°C to 150°C |

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 3)

| | | | T _A = 2 | T _A = 25°C | | TO C | –55°C TO 125°C | | UNIT |
|----------------|------------------------------------|--|--------------------|-----------------------|------|---------|-------------------|------|--------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| Vcc | Supply voltage | | 1.5 | 5.5 | 1.5 | 5.5 | 1.5 | 5.5 | V |
| | | V _{CC} = 1.5 V | 1.2 | | 1.2 | | 1.2 | | |
| ۷ıн | High-level input voltage | V _{CC} = 3 V | 2.1 | | 2.1 | | 2.1 | | V |
| | | V _{CC} = 5.5 V | 3.85 | | 3.85 | | 3.85 | | |
| | | V _{CC} = 1.5 V | | 0.3 | | 0.3 | | 0.3 | |
| V_{IL} | Low-level input voltage | V _{CC} = 3 V | | 0.9 | | 0.9 | | 0.9 | V |
| | | V _{CC} = 5.5 V | | 1.65 | | 1.65 | | 1.65 | |
| ٧ _I | Input voltage | | 0 | VCC | 0 | VCC | 0 | VCC | V |
| ٧o | Output voltage | | 0 | VCC | 0 | VCC | 0 | VCC | V |
| loh | High-level output current | V _{CC} = 4.5 V to 5.5 V | | -24 | | -24 | | -24 | mA |
| loL | Low-level output current | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ | | 24 | | 24 | | 24 | mA |
| Δt/Δν | Input transition rise or fall rate | $V_{CC} = 1.5 \text{ V to } 3 \text{ V}$ | | 50 | | 50 | | 50 | ns/V |
| ΔυΔν | input transition rise of fall fate | $V_{CC} = 3.6 \text{ V to } 5.5 \text{ V}$ | | 20 | | 20 | | 20 | 115/ V |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

^{2.} The package thermal impedance is calculated in accordance with JESD 51-7.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | | T _A = 25°C | | –40°C TO 85°C | | –55°C TO 125°C | | UNIT | |
|-----------|---|---------------------------------------|-------|-----------------------|------|------------------|------|-------------------|------|------|--|
| | | | VCC | MIN | MAX | MIN | MAX | MIN | MAX | | |
| | | | 1.5 V | 1.4 | | 1.4 | | 1.4 | | | |
| | VI = VIH or VIL | $I_{OH} = -50 \mu A$ | 3 V | 2.9 | | 2.9 | | 2.9 | | | |
| | | | 4.5 V | 4.4 | | 4.4 | | 4.4 | | | |
| Voн | | $I_{OH} = -4 \text{ mA}$ | 3 V | 2.58 | | 2.48 | | 2.4 | | V | |
| | | $I_{OH} = -24 \text{ mA}$ | 4.5 V | 3.94 | | 3.8 | | 3.7 | | | |
| | | $I_{OH} = -50 \text{ mA}^{\dagger}$ | 5.5 V | | | | | 3.85 | | | |
| | | I _{OH} = -75 mA [†] | 5.5 V | | | 3.85 | | | | | |
| | | I _{OL} = 50 μA | 1.5 V | | 0.1 | | 0.1 | | 0.1 | | |
| | | | 3 V | | 0.1 | | 0.1 | | 0.1 | | |
| | | | 4.5 V | | 0.1 | | 0.1 | | 0.1 | | |
| VOL | $V_I = V_{IH} \text{ or } V_{IL}$ | I _{OL} = 12 mA | 3 V | | 0.36 | | 0.44 | | 0.5 | V | |
| | | I _{OL} = 24 mA | 4.5 V | | 0.36 | | 0.44 | | 0.5 | | |
| | | $I_{OL} = 50 \text{ mA}^{\dagger}$ | 5.5 V | | | | | | 1.65 | | |
| | | $I_{OL} = 75 \text{ mA}^{\dagger}$ | 5.5 V | | | | 1.65 | | | | |
| lı | V _I = V _{CC} or GND | | 5.5 V | | ±0.1 | | ±1 | | ±1 | μΑ | |
| lcc | $V_I = V_{CC}$ or GND, | IO = 0 | 5.5 V | | 4 | | 40 | | 80 | μΑ | |
| Ci | | | | | 10 | | 10 | | 10 | pF | |

[†] Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 1.5 V, C_L = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | –40°C TO 85°C | | –55°C TO 125°C | | UNIT |
|------------------|-----------------|----------------|------------------|-----|-------------------|-----|------|
| | (INFOT) | (001F01) | MIN | MAX | MIN | MAX | |
| ^t PLH | A or B | V | | 131 | | 144 | no |
| ^t PHL | AUID | ī | | 131 | | 144 | ns |

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V, C_L = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | –40°(85° | | –55°C 125 | UNIT | |
|------------------|-----------------|----------------|--------------|------|--------------|------|----|
| | (1141 01) | (001101) | MIN | MAX | MIN | MAX | |
| t _{PLH} | A or B | V | 4.1 | 14.6 | 4 | 16.1 | no |
| t _{PHL} | AUID | ī | 4.1 | 14.6 | 4 | 16.1 | ns |

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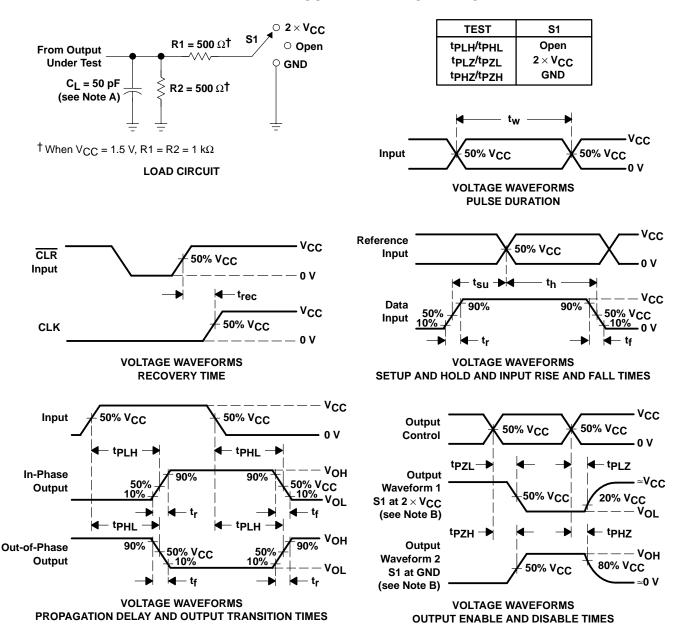
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V, C_L = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | –40°0 85° | | –55°C TO 125°C | | UNIT |
|------------------|-----------------|----------------|--------------|------|-------------------|------|------|
| | (1141 01) | (0011 01) | MIN | MAX | MIN | MAX | |
| t _{PLH} | A or B | V | 3 | 10.4 | 2.9 | 11.5 | no |
| ^t PHL | AUIB | 1 | 3 | 10.4 | 2.9 | 11.5 | ns |

operating characteristics, V_{CC} = 5 V, T_A = 25°C

| | PARAMETER | TYP | UNIT |
|----|-------------------------------|-----|------|
| Cr | Power dissipation capacitance | 55 | pF |

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and test-fixture capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_f = 3$ ns, $t_f = 3$ ns. Phase relationships between waveforms are arbitrary.
- D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
- E. The outputs are measured one at a time with one input transition per measurement.
- F. tpLH and tpHL are the same as tpd.
- G. tpzL and tpzH are the same as ten.
- H. tpLz and tpHz are the same as tdis.

Figure 1. Load Circuit and Voltage Waveforms



PACKAGE OPTION ADDENDUM

www.ti.com 15-Oct-2009

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|-----------------|--------------------|------|----------------|----------------------------|------------------|------------------------------|
| CD54AC02F3A | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| CD74AC02E | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74AC02EE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74AC02M | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC02M96 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC02M96E4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC02M96G4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC02ME4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC02MG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

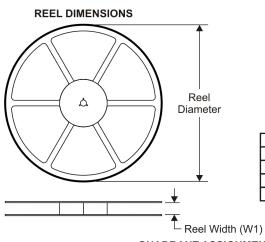
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION





| A0 | Dimension designed to accommodate the component width |
|----|---|
| В0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | | | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|-----------------|--------------------|----|------|--------------------------|--------------------------|---------|---------|---------|------------|-----------|------------------|
| CD74AC02M96 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |





*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74AC02M96 | SOIC | D | 14 | 2500 | 346.0 | 346.0 | 33.0 |

14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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