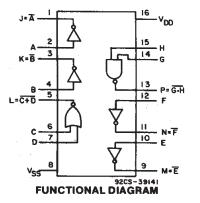


Data sheet acquired from Harris Semiconductor SCHS090C - Revised October 2003

CD4572UB Types



of 'B' Series CMOS Devices."

CMOS Hex Gate

Four Inverters, One 2-Input NOR Gate, One 2-Input NAND Gate

Features:

- Pin 7 NOR input positioned adjacent to V_{ss} for easy use of gate as an inverter
- Pin 15 NAND input positioned adjacent to VDD for easy use of gate as an inverter
- Standard symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 µA at 18 V over full package-temperature range: 100 nA at 18 V and 25° C

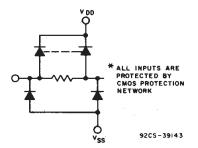
■ 5-V, 10-V, and 15-V parametric ratings

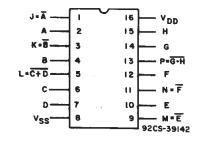
Meets all requirements of JEDEC Standard No. 13B, "Standard Specifications for Description of 'B' Series **CMOS Devices**"

The CD4572UB types are supplied in 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

with direct implementation of inverter, NAND, and NOR functions and supplements the existing family of CMOS gates. The CD4572UB devices meet all requirements of JEDEC Standard No. 13B, "Standard Specifications for Description

CD4572UB Hex Gate provides the system designer





TERMINAL ASSIGNMENT

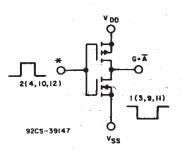
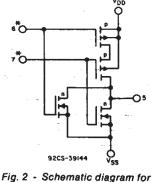


Fig. 1 - Schematic diagram of one of four identical inverters.



the 2-input NOR gate.

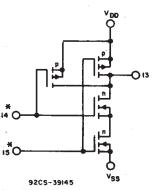


Fig. 3 - Schematic diagram for the 2-input NAND gate.



CD4572UB Types



MAXIMUM RATINGS, Absolute-Maximum Values:				,
DC SUPPLY-VOLTAGE RANGE, (V _{DD}) Voltages referenced to V _{SS} Terminal) INPUT VOLTAGE RANGE, ALE INPUTS	ಸ್ಕಾರ ಬ್ಯಾಂಟ್ಯಾನ್ ಬೌಂಕ್ ರಂಭ್ಯ	e ut to real	A. 1	
Voltages referenced to VSS Terminal)				+20
INPUT VOLTAGE RANGE, ALL INPUTS			0.5V to VDD	+0.5
DC INPUT CURRENT, ANY ONE INPUT			·····±	:10mA
POWER DISSIPATION PER PACKAGE (PD):		858 (A. 1915)	5	
For T _A = -55°C to +100°C				WmOC
For T _A = +100°C to +125°C		Derate	Linearity at 12mW/OC to 20	00mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	the state of the second state	化学生 化化学	The second se	
FOR TA = FULL PACKAGE-TEMPERATURE RANGE (10	
FOR $T_A = FULL PACKAGE-TEMPERATURE RANGE (OPERATING-TEMPERATURE RANGE (T_A)$	All Package Types}		55°C to +1	12500
OPERATING-TEMPERATURE RANGE (TA)	All Package Types}		55°C to +1	12500
OPERATING-TEMPERATURE RANGE (T _A) STORAGE TEMPERATURE RANGE (T _{sta})	All Package Types}		55°C to +1 65°C to +1	125°C
OPERATING-TEMPERATURE RANGE (TA)	All Package Types}		55°C to +1 65°C to +1	125°C

જેવી પૈયા તે જિલ્લાન વિજ્ઞાણ મહાલ મહાલ પ્રાપ્ય છે. તે પ્રાપ્ય તે પ્રાપ્ય દ્વાર પ્રાપ્ય તે લાગ તે છે. દ્વાર પ્રા વર્ષ વાર વ્યવસાય વારા કે જ વિજ્ઞાણ પ્રાપ્ય છે. આ ગામને પ્રાપ્ય વ્યવસાય થઈ હેલા કર્યો સાથ પ્રાપ્ય લોક્સ કરવા તે વે વાર છે. જે વે વ્યવસાય વાર જે જે સાથ વ્યવસાય વ્યવસાય વાર પ્રાપ્ય લોક્સ, વર પ્રાપ્ય સ્થાપ્ય સાથ વ્યવસાય

RECOMMENDED OPERATING CONDITIONS

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For maximum reliability, nominal operating conditions should be selected so that operation is always within the 1. an tha suidh. Anns 12.50 following ranges: . -

QUADAOTEDICTIO	LIN	UNITS	
CHARACTERISTIC	Min.	Max.	UNITS
Supply-Voltage Range (For T _A =Full Package-Temperature Range)	3	18	V

STATIC ELECTRICAL CHARACTERISTICS

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	CO	NDITIO	NS								
CHARACTERISTIC	V0 (V)	VIN (V)	V _{DD} (V)		AITS AT	INDICA	TED TEN	MPERAT	+25	°C)	UNITS
		. ,		-55	-40	+85	+125	Min.	Тур.	Max.	
	<u> </u>	0, 5	5	0.25	0.25	7.5	7.5	—	0.01	0.25	
Quiescent Device		0, 10	10	0.5	0.5	15	15	—	0.01	0.5	μA
Current, Ipp Max.	—	0, 15	15	1	1	30	30	—	0.01	1	
		0, 20	20	5	5	150	150	—	0.02	5	
Output Low	0.4	0, 5	5	0.64	0.61 🕆	0.42	0.36	0.51	1	—	
(Sink) Current	0.5	0, 10	10	1:6	1.5	1,1	0.9	1.3	2.6	_	
lo∟ Min.	1.5	0, 15	15	4.2	4	2.8	2.4	3.4	6.8	. —	
Output High	4.6	0, 5	5	-0.64	-0.61	-0.42	-0.36	-0.51	1 _⊁	—	- mA
(Source)	2.5	0, 5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	· · · · · ·	110
Current,	9.5	0, 10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	. —	
loн Min.	13.5	0, 15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8		
Output Voltage:		0, 5	5		0.0)5			0	0.05	
Low-Level,		0, 10	10		0.0)5		—	0	0.05	
Vo∟ Max.		0, 15	15		0.0)5			0	0.05	
Output Voltage:	—	0, 5	5		4.9	95		4.95	5		5
High-Level,		0, 10	10		9.9	95		9.95	10	—	
V _{он} Min.	—	0, 15	15		14.	95		14.95	15	_	v
Input Low	0.5, 4.5		5		1			-		1	v
Voltage,	1, 9		10		2					2	
VIL Max.	1.5, 13.5	_	15		2.	5				2.5	
Input High	0.5, 4.5	<u> </u>	5	4				4			
Voltage,	1,9		10	8				8		—	
V _{IH} Min.	1.5, 13.5		15		12	.5		12.5			
Input Current, I _{IN} Max.	-	0, 18	18	±0.1	±0.1	±1	±1	_	±10 ⁻⁵	±0.1	μA

CD4572UB Types

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LINUTO		
CHARACTERISTIC	STMBUL	V _{DD} (V)	Min.	Тур.	Max.	
		5		100	200	1
Propagation Delay Time	t _{PHL} , t _{PLH}	10		55	110	
		15	<u> </u>	40	85	
		5	_	100	200	- ns
Transition Time	t _{THL} , t _{TLH}	10	_	50	100	
		15	_	40	80	
Input Capacitance	CIN	Any Input	-	10	15	pF

DYNAMIC ELECTRICAL CHARACTERISTICS at TA=25°C, Input tr,tr=20 ns, CL=50 pF, RL=200 KΩ

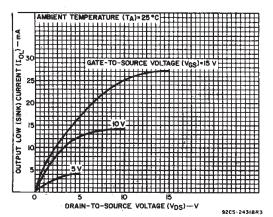


Fig. 4 - Typical output low (sink) current characteristics.

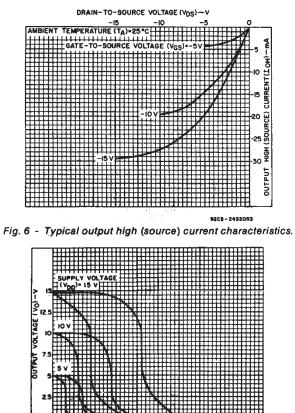


Fig. 8 - Minimum and maximum inverter voltage transfer characteristics.

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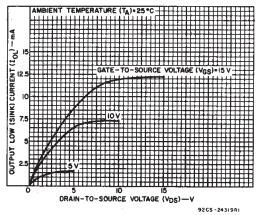


Fig. 5 - Minimum output low (sink) current characteristics.

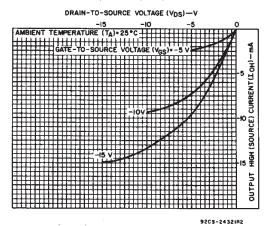
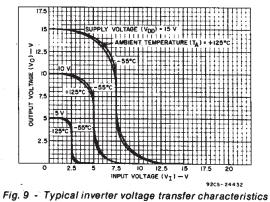
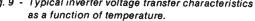
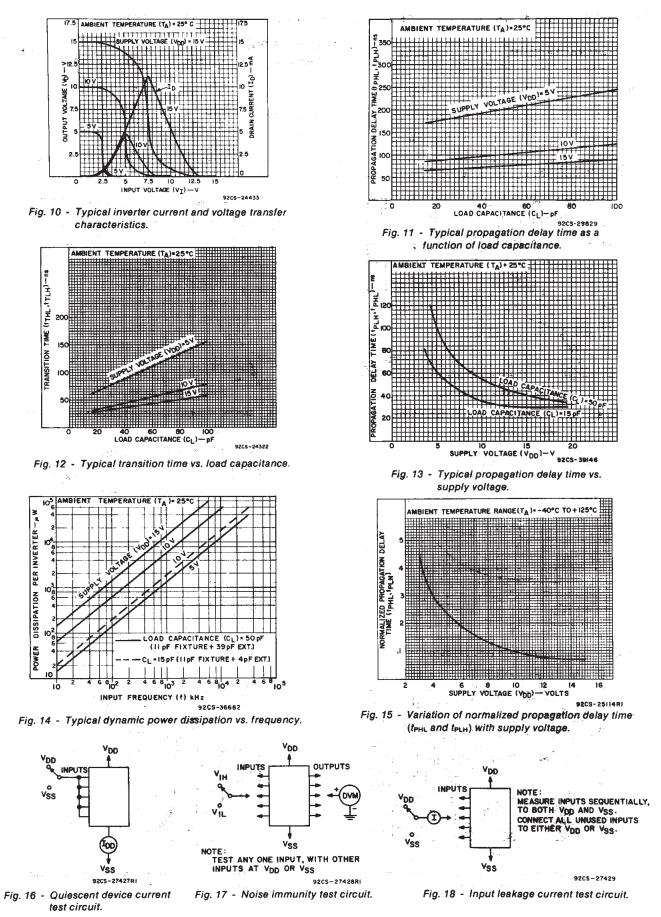


Fig. 7 - Minimum output high (source) current characteristics.







CD4572UB Types

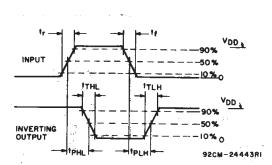
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 $M_{\rm eff} = g_{12} g_{12}^{\rm eff}$

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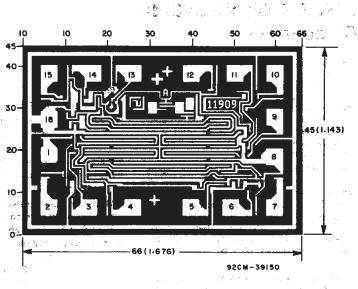
Fig: 19 - Transition times and propagation delay times, combination logic.

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exclusion of the second of the second of **Dimensions and pad layout for CD4572UBH.** The asi8-second second second of the second s

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10⁻³ inch).

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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
CD4572UBE	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Contact TI Distributor or Sales Office
CD4572UBEE4	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Contact TI Distributor or Sales Office
CD4572UBM	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CD4572UBME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CD4572UBMG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CD4572UBMT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CD4572UBMTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CD4572UBMTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CD4572UBNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CD4572UBNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CD4572UBNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CD4572UBPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CD4572UBPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CD4572UBPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.



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28-Aug-2010

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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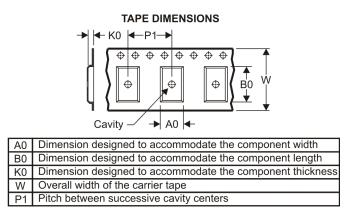
PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4572UBNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4572UBPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

30-Jul-2010



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4572UBNSR	SO	NS	16	2000	346.0	346.0	33.0
CD4572UBPWR	TSSOP	PW	16	2000	346.0	346.0	29.0

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



4211283-4/D 06/11

D (R-PDSO-G16) PLASTIC SMALL OUTLINE Stencil Openings (Note D) Example Board Layout (Note C) -16x0,55 - 14x1,27 -14x1,27 16x1,95 4,80 4,80 Example Non Soldermask Defined Pad Example Pad Geometry (See Note C) 0,60 Example 2,00 Solder Mask Opening

(See Note E)

NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

← 0,07 All Around

- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994. β . This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153



LAND PATTERN DATA



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 \bigcirc Gage Plane ₽ 0,25 7 1 1,05 0,55 0-10 Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS ** 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G**)

14-PINS SHOWN

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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