SDAS006B - APRIL 1982 - REVISED DECEMBER 1994

 Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

These devices contain four independent 2-input exclusive-OR gates. They perform the Boolean functions $Y = A \oplus B$ or $Y = \overline{AB} + A\overline{B}$ in positive logic.

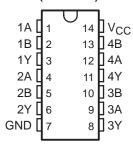
A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

The SN54ALS86 and SN54AS86A are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS86 and SN74AS86A are characterized for operation from 0°C to 70°C.

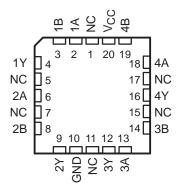
FUNCTION TABLE (each gate)

INP	UTS	OUTPUT
Α	В	Υ
L	L	L
L	Н	Н
Н	L	Н
Н	Н	L

SN54ALS86, SN54AS86A . . . J PACKAGE SN74ALS86, SN74AS86A . . . D OR N PACKAGE (TOP VIEW)

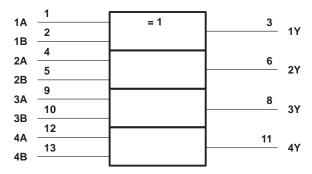


SN54ALS86, SN54AS86A . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, and N packages.

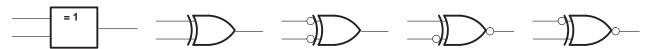


SDAS006B - APRIL 1982 - REVISED DECEMBER 1994

exclusive-OR logic

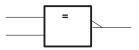
An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

EXCLUSIVE-OR



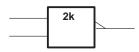
These are five equivalent exclusive-OR symbols valid for an 'ALS86 or 'AS86A gate in positive logic. Negation may be shown at any two ports.

LOGIC-IDENTITY ELEMENT



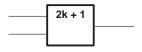
The output is active (low) if all inputs are at the same logic level (i.e., A = B).

EVEN-PARITY ELEMENT



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

SDAS006B - APRIL 1982 - REVISED DECEMBER 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V _{CC}	
Input voltage, V _I	
Operating free-air temperature range, TA: SN54AL	S86 –55°C to 125°C
SN74AL	S86 0°C to 70°C
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SI	154ALS8	36	SI	174ALS8	36	LINUT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
IOH	High-level output current			-0.4			-0.4	mA
loL	Low-level output current			4			8	mA
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		SN	I54ALS8	36	SN	174ALS8	16			
PARAMETER	TEST CO	TEST CONDITIONS			MAX	MIN	TYP‡	MAX	UNIT	
VIK	$V_{CC} = 4.5 \text{ V},$	$I_{\parallel} = -18 \text{ mA}$			-1.5			-1.5	V	
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -2	2		V _{CC} -2)		V	
V	V 45V	$I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	V	
V _{OL}	V _{CC} = 4.5 V	$I_{OL} = 8 \text{ mA}$					0.35	0.5	V	
Ц	$V_{CC} = 5.5 \text{ V},$	V _I = 7 V			0.1			0.1	mA	
lін	$V_{CC} = 5.5 V,$	$V_{I} = 2.7 V$			20			20	μΑ	
I _I L	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.1			-0.1	mA	
ΙΟ§	V _{CC} = 5.5 V,	V _O = 2.25 V	-20		-112	-30		-112	mA	
ICC	V _{CC} = 5.5 V,	All inputs at 4.5 V		3.9	5.9		3.9	5.9	mA	

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L R _L	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω , T_A = MIN to MAX¶				
	, ,	,	SN54ALS86		SN74ALS86			
			MIN	MAX	MIN	MAX		
^t PLH	A or B	V	3	22	3	17		
^t PHL	(other input low)	Y	2	14	2	12	ns	
t _{PLH}	A or B	V	3	22	3	17	ns	
^t PHL	(other input high)	1	2	12	2	10	115	

 $[\]P$ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



[§] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SDAS006B - APRIL 1982 - REVISED DECEMBER 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V _{CC}	7 V
Input voltage, V _I	7 V
Operating free-air temperature range, T _A : SN54AS86A	55°C to 125°C
SN74AS86A	0°C to 70°C
Storage temperature range	65°C to 150°C

recommended operating conditions

		SN54AS86A			SN	UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX	UNII
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			8.0			8.0	V
loh	High-level output current			-2			-2	mA
l _{OL}	Low-level output current			20			20	mA
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	TEST CONDITIONS			154AS86	A	SN	174AS86	Α	
PARAMETER				TYP‡	MAX	MIN	TYP‡	MAX	UNIT
VIK	$V_{CC} = 4.5 \text{ V},$	$I_{I} = -18 \text{ mA}$			-1.2			-1.2	V
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -2 \text{ mA}$	VCC -2)		V _{CC} -2)		V
VoL	V _{CC} = 4.5 V,	$I_{OL} = 20 \text{ mA}$		0.35	0.5		0.35	0.5	V
lį	V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA
lН	V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μΑ
I _Ι Γ	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.5			-0.5	mA
ΙΟ [§]	V _{CC} = 5.5 V,	V _O = 2.25 V	-30		-112	-30		-112	mA
Іссн	$V_{CC} = 5.5 \text{ V},$	$V_{I(A)} = 4.5 \text{ V}, V_{I(B)} = 0$		11	18		11	18	mA
ICCL	V _{CC} = 5.5 V,	V _I = 4.5 V		20	38		20	38	mA

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L R _L	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω , T _A = MIN to MAX¶					
	` '	, , ,	SN54AS86A		SN74AS86A				
			MIN	MAX	MIN	MAX			
t _{PLH}	A or B	V	2	8.5	2	7.5			
^t PHL	(other input low)	Y	2	8	2	6.5	ns		
t _{PLH}	A or B	V	1	8	1	6.5	ns		
^t PHL	(other input high)	Ť	1	9	1	7	115		

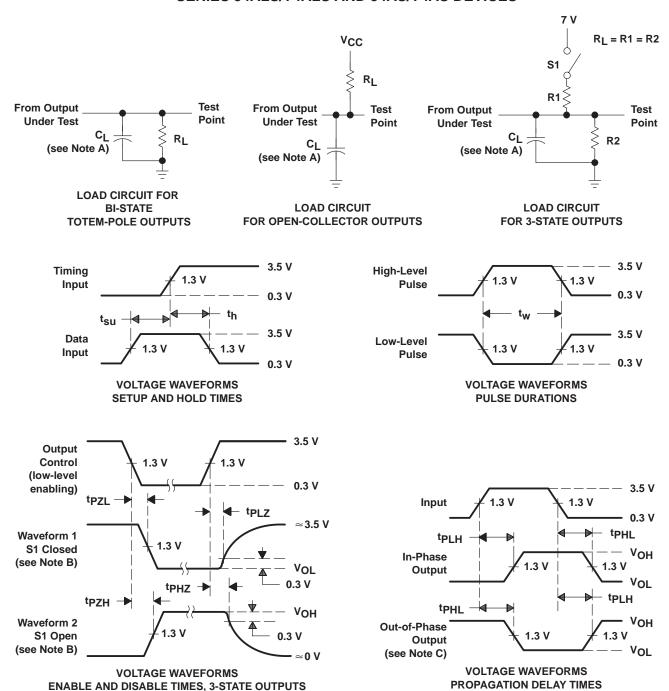
[¶]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[§] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
- D. All input pulses have the following characteristics: PRR \leq 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
- E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



5-Sep-2011

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-88621012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-8862101CA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Call TI	
5962-8862101DA	ACTIVE	CFP	W	14	1	TBD	Call TI	Call TI	
5962-9757201Q2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-9757201QCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Call TI	
SN54ALS86J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SN74ALS86D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS86DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS86DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS86DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS86DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS86DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS86N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74ALS86N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	
SN74ALS86NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74ALS86NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS86NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS86NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS86AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS86ADE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS86ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	



www.ti.com 5-Sep-2011

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74AS86AN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74AS86ANE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SNJ54ALS86FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54ALS86J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SNJ54ALS86W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
SNJ54AS86AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54AS86AJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL. Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54ALS86, SN54AS86A, SN74ALS86, SN74AS86A:

Catalog: SN74ALS86, SN74AS86A



5-Sep-2011

• Military: SN54ALS86, SN54AS86A

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

www.ti.com 29-Jul-2009

TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS86DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74ALS86NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

www.ti.com 29-Jul-2009



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS86DR	SOIC	D	14	2500	346.0	346.0	33.0
SN74ALS86NSR	SO	NS	14	2000	346.0	346.0	33.0

14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB



FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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