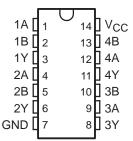
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- **Qualified for Automotive Applications**
- Inputs Are TTL-Voltage Compatible
- **EPIC™** (Enhanced-Performance Implanted **CMOS) Process**
- Latch-Up Performance Exceeds 250 mA Per **JESD 17**
- **ESD Protection Exceeds 2000 V Per** MIL-STD-883. Method 3015: Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)

#### **DOR PW PACKAGE** (TOP VIEW)



#### description

The SN74AHCT00Q performs the Boolean function  $Y = \overline{A \bullet B}$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

#### ORDERING INFORMATION<sup>†</sup>

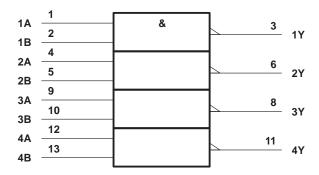
TA	PACK	\GE <sup>‡</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING		
-40°C to 125°C	SOIC - D	Tape and reel	SN74AHCT00QDRQ1	AHCT00Q		
-40°C to 125°C	TSSOP - PW	Tape and reel	SN74AHCT00QPWRQ1	HB00Q		

<sup>†</sup> For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.

#### **FUNCTION TABLE** (each gate)

INP	UTS	OUTPUT
Α	В	Υ
Н	Н	L
L	X	Н
Х	L	Н

## logic symbol†



<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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<sup>‡</sup> Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.

## SN74AHCT00Q-Q1 QUADRUPLE 2-INPUT POSITIVE-NAND GATE

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### logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	$-0.5$ V to 7 V
Output voltage range, VO (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through V <sub>CC</sub> or GND	±50 mA
Package thermal impedance, $\hat{\theta}_{JA}$ (see Note 2): D package	86°C/W
PW package	113°C/W
Storage temperature range, T <sub>stq</sub>	65°C to 150°C

<sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	V
VIH	High-level input voltage	2		V
V <sub>IL</sub>	Low-level input voltage		0.8	V
VI	Input voltage	0	5.5	V
VO	Output voltage	0	VCC	V
ЮН	High-level output current		-8	mA
loL	Low-level output current		8	mA
Δt/Δν	Input transition rise or fall rate		20	ns/V
TA	Operating free-air temperature	-40	125	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEGT COMPLETIONS	.,	T,	չ = 25°C	;	BAINI	BAAV	UNIT	
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	MIN	MAX		
V	$I_{OH} = -50 \mu A$	451/	4.4	4.5		4.4		.,	
VOH	I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8		V	
V	$I_{OL} = 50 \mu A$	4.5 V	4.5.1/			0.1		0.1	V
VOL	I <sub>OL</sub> = 8 mA				0.36		0.44	V	
IĮ	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V			±0.1		±1	μΑ	
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			2		20	μΑ	
ΔI <sub>CC</sub> †	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			1.35		1.5	mA	
Ci	$V_I = V_{CC}$ or GND	5 V		2	10			pF	

<sup>†</sup> This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or VCC.

# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	то	LOAD	T <sub>A</sub> = 25°C				MAY	
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE		TYP	MAX	MIN	MAX	UNIT
<sup>t</sup> PLH	A or B	Υ	C <sub>L</sub> = 15 pF		5	6.9	1	8	
t <sub>PHL</sub>					5	6.9	1	8	ns
<sup>t</sup> PLH	A or D	Y	C <sub>L</sub> = 50 pF		5.5	7.9	1	9	
<sup>t</sup> PHL	A or B				5.5	7.9	1	9	ns

## noise characteristics, $V_{CC} = 5 \text{ V}$ , $C_L = 50 \text{ pF}$ , $T_A = 25^{\circ}\text{C}$ (see Note 4)

	PARAMETER	MIN	TYP	MAX	UNIT
V <sub>OL(P)</sub>	Quiet output, maximum dynamic VOL		0.4	8.0	V
V <sub>OL(V)</sub>	Quiet output, minimum dynamic V <sub>OL</sub>		-0.4	-0.8	V
VOH(V)	Quiet output, minimum dynamic VOH		4.5		V
V <sub>IH(D)</sub>	High-level dynamic input voltage	2			V
V <sub>IL(D)</sub>	Low-level dynamic input voltage			8.0	V

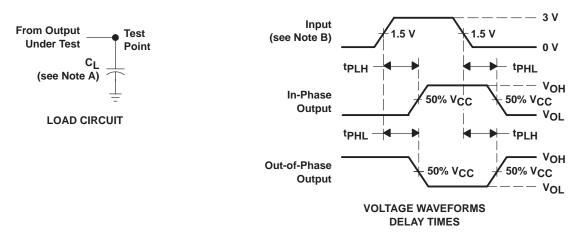
NOTE 4: Characteristics are for surface-mount packages only.

## operating characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST CC	NDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	No load,	f = 1 MHz	10.5	pF

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### PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_f = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ .
- C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms







12-Oct-2011

#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN74AHCT00QDRG4Q1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHCT00QDRQ1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHCT00QPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHCT00QPWRQ1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## D (R-PDSO-G14)

## PLASTIC SMALL OUTLINE



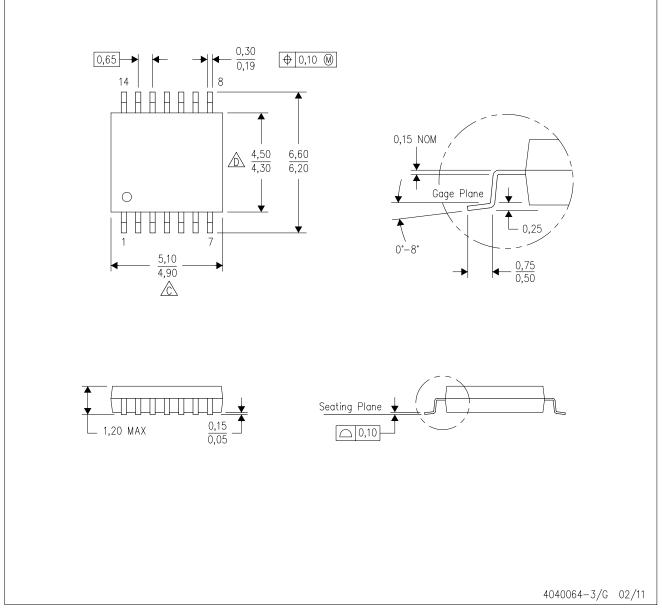
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



PW (R-PDSO-G14)

## PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
  - Sody length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



## PW (R-PDSO-G14)

## PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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