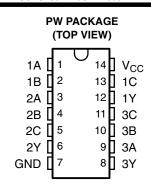
SN74LV11A-Q1 TRIPLE 3-INPUT POSITIVE-AND GATE

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- Qualified for Automotive Applications
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- 2-V to 5.5-V V_{CC} Operation
- Typical V_{OLP} (Output Ground Bounce)
 <0.8 V at V_{CC}= 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 >2.3 V at V_{CC} = 3.3 V, T_A = 25°C
- Support Mixed-Mode Voltage Operation on All Ports
- I_{off} Supports Partial-Power-Down Mode Operation



description/ordering information

This triple 3-input positive-AND gate is designed for 2-V to 5.5-V V_{CC} operation.

The SN74LV11A performs the Boolean function $Y = A \bullet B \bullet C$ or $Y = \overline{A + B + C}$ in positive logic.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION[†]

T _A	PACK	AGE‡	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 105°C	TSSOP - PW	Tape and reel	SN74LV11ATPWRQ1	LV11AT

[†] For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

FUNCTION TABLE (each gate)

	INPUTS	OUTPUT	
Α	В	С	Υ
Н	Н	Н	Н
L	X	Χ	L
Х	L	Χ	L
Х	Х	L	L

logic diagram, each gate (positive logic)





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



[‡] Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	–0.5 V to 7 V
Input voltage range, V _I (see Note 1)	–0.5 V to 7 V
Output voltage range applied in high or low state, V _O (see Notes 1 and 2)	\dots -0.5 V to V _{CC} + 0.5 V
Voltage range applied to any output in the power-off state, V _O (see Note 1)	–0.5 V to 7 V
Input clamp current, I _{IK} (V _I < 0)	–20 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V _{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3)	113°C/W
Storage temperature range, T _{stq}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 5.5 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT		
V_{CC}	Supply voltage		2	5.5	V		
		V _{CC} = 2 V	1.5				
.,	I Bala Jawa I Sanashara Nama	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	$V_{CC} \times 0.7$] ,,		
V_{IH}	High-level input voltage	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	$V_{CC} \times 0.7$		٧		
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$V_{CC} \times 0.7$				
		V _{CC} = 2 V		0.5			
V	Law law line who alterna	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	\	V _{CC} ×0.3			
V _{IL}	Low-level input voltage	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	\	V _{CC} ×0.3			
		\	/ _{CC} ×0.3				
VI	Input voltage		0	5.5	V		
Vo	Output voltage		0	V _{CC}	V		
		V _{CC} = 2 V		-50	μΑ		
	I Bulb Jamed Andrew Annual Andrew	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		-2			
loh	High-level output current	V _{CC} = 3 V to 3.6 V		-6	mA		
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		-12]		
		V _{CC} = 2 V		50	μΑ		
	Landard adapt annual	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	2				
l _{OL}	Low-level output current	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$		6	mA		
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		12			
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		200			
Δt/Δν	Input transition rise or fall rate	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$		100	ns/V		
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$			20			
T _A	Operating free-air temperature		-40	105	°C		

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



SCES468D - JULY 2003 - REVISED JANUARY 2008

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc}	MIN	TYP	MAX	UNIT
	$I_{OH} = -50 \mu\text{A}$	2 V to 5.5 V	V _{CC} -0.1			
V	$I_{OH} = -2 \text{ mA}$	2.3 V	2			V
V _{OH}	$I_{OH} = -6 \text{ mA}$	3 V	2.48			V
	$I_{OH} = -12 \text{ mA}$	4.5 V	3.8			
	$I_{OL} = 50 \mu A$	2 V to 5.5 V			0.1	
.,	I _{OL} = 2 mA	2.3 V			0.4	٧
V _{OL}	I _{OL} = 6 mA	3 V			0.44	V
	I _{OL} = 12 mA	4.5 V			0.55	
I _I	V _I = 5.5 V or GND	0 to 5.5 V			±1	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			20	μΑ
l _{off}	V_1 or $V_0 = 0$ to 5.5 V	0 V			5	μΑ
C _i	$V_I = V_{CC}$ or GND	3.3 V		1.9		pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V \pm 0.2 V (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	то	LOAD	T,	գ = 25°C	;	MINI	MAY	LINUT
PARAMETER	AMETER (INPUT) (OUTPUT)		CAPACITANCE	MIN	TYP	MAX	MIN	MAX	UNIT
t _{pd}	A, B, or C	Y	C _L = 50 pF		9.9	17.5	1	21	ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	LOAD	T,	₄ = 25°C	;	MINI	MAY	LINUT
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	UNIT
t _{pd}	A, B, or C	Υ	C _L = 50 pF		7.2	12.3	1	14	ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

DADAMETED	FROM TO LOAD		T,	₄ = 25°C	;	MIN	MAX	UNIT	
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	IVIIIN	WAX	UNII
t _{pd}	A, B, or C	Υ	C _L = 50 pF		5.4	7.9	1	9	ns

SN74LV11A-Q1 TRIPLE 3-INPUT POSITIVE-AND GATE

SCES468D - JULY 2003 - REVISED JANUARY 2008

noise characteristics, V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C (see Note 5)

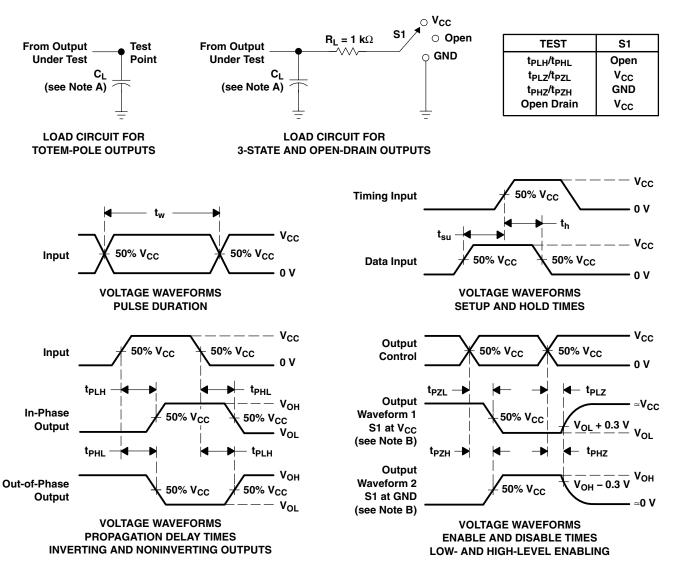
	PARAMETER	MIN	TYP	MAX	UNIT
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}		0.2	0.8	٧
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}		0	-0.8	٧
V _{OH(V)}	Quiet output, minimum dynamic V _{OH}		3.2		٧
V _{IH(D)}	High-level dynamic input voltage	2.31			٧
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST CO	V _{CC}	TYP	UNIT	
	Power dissination conscitance	$C_1 = 50 \text{ pF},$	f = 10 MHz	3.3 V	13.9	pF
Opd	Power dissipation capacitance	C _L = 50 pr,	f = 10 MHz	5 V	15.4	þΓ

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_f \leq 3$ ns. $t_f \leq 3$ ns.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms



12-Oct-2011

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74LV11ATPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV11ATPWRQ1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74LV11A-Q1:

Catalog: SN74LV11A

Enhanced Product: SN74LV11A-EP





12-Oct-2011

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Enhanced Product Supports Defense, Aerospace and Medical Applications

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
 - Sody length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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