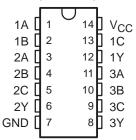
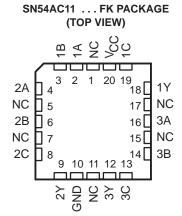
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- 2-V to 6-V V<sub>CC</sub> Operation
- Inputs Accept Voltages to 6 V

SN54AC11 . . . J OR W PACKAGE SN74AC11 . . . D, DB, N, NS, OR PW PACKAGE (TOP VIEW)



### Max t<sub>pd</sub> of 7.5 ns at 5 V



NC - No internal connection

### description/ordering information

The 'AC11 devices contain three independent 3-input AND gates. These devices perform the Boolean function  $Y = A \cdot B \cdot C$  or  $Y = \overline{A} + \overline{B} + \overline{C}$  in positive logic.

#### **ORDERING INFORMATION**

TA	PACKAGE	<u></u> =†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP – N	Tube	SN74AC11N	SN74AC11N
–40°C to 85°C	0010 D	Tube	SN74AC11D	1044
	SOIC - D	Tape and reel	SN74AC11DR	AC11
	SOP - NS	Tape and reel	SN74AC11NSR	AC11
	SSOP – DB	Tape and reel	SN74AC11DBR	AC11
	TOCOD DW	Tube	SN74AC11PW	AC44
	TSSOP – PW	Tape and reel	SN74AC11PWR	AC11
	CDIP – J	Tube	SNJ54AC11J	SNJ54AC11J
−55°C to 125°C	CFP – W	Tube	SNJ54AC11W	SNJ54AC11W
	LCCC - FK	Tube	SNJ54AC11FK	SNJ54AC11FK

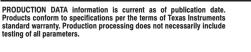
<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

# FUNCTION TABLE (each gate)

	INPUTS		OUTPUT
Α	В	Y	
Н	Н	Н	Н
L	X	Χ	L
Х	L	Χ	L
Х	X	L	L



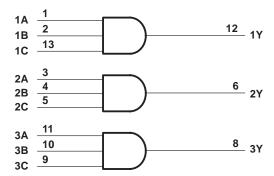
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



### SN54AC11, SN74AC11 TRIPLE 3-INPUT POSITIVE-AND GATES

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#### logic diagram, each gate (positive logic)



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>		–0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)		
Output voltage range, V <sub>O</sub> (see Note 1)		
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ).		±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CO}$	c)	±20 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$		±50 mA
Continuous current through V <sub>CC</sub> or GND		±200 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 2)	: D package	86°C/W
	DB package	96°C/W
	N package	80°C/W
	NS package	76°C/W
	PW package	113°C/W
Storage temperature range, T <sub>stg</sub>		–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 3)

			SN54	AC11	SN74	AC11	
			MIN	MAX	MIN	MAX	UNIT
VCC	Supply voltage		2	6	2	6	V
		V <sub>CC</sub> = 3 V	2.1		2.1		
٧ <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 4.5 V	3.15		3.15		V
		$V_{CC} = 5.5 \text{ V}$	3.85		3.85		
		V <sub>CC</sub> = 3 V		0.9		0.9	
٧ <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 4.5 V		1.35		1.35	V
		V <sub>CC</sub> = 5.5 V		1.65		1.65	
VI	Input voltage		0	VCC	0	VCC	V
٧o	Output voltage		0	VCC	0	Vcc	V
		V <sub>CC</sub> = 3 V		-12		-12	
lOH	High-level output current	V <sub>CC</sub> = 4.5 V		-24		-24	mA
		V <sub>CC</sub> = 5.5 V		-24		-24	
		V <sub>CC</sub> = 3 V		12		12	
lOL	Low-level output current	V <sub>CC</sub> = 4.5 V		24		24	mA
		V <sub>CC</sub> = 5.5 V		24		24	
Δt/Δν	Input transition rise or fall rate			8		8	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEGT COMPITIONS	.,	Т	A = 25°C	;	SN54/	AC11	SN74/	AC11	
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
		3 V	2.9	2.99		2.9		2.9		
	I <sub>OH</sub> = -50 μA	4.5 V	4.4	4.49		4.4		4.4		
		5.5 V	5.4	5.49		5.4		5.4		
V	I <sub>OH</sub> = -12 mA	3 V	2.56			2.4		2.46		
VOH	04.554	4.5 V	3.86			3.7		3.76		V
	$I_{OH} = -24 \text{ mA}$	5.5 V	4.86			4.7		4.76		
	$I_{OH} = -50 \text{ mA}^{\dagger}$	5.5 V				3.85				
	$I_{OH} = -75 \text{ mA}^{\dagger}$	5.5 V						3.85		
		3 V		0.002	0.1		0.1		0.1	
	I <sub>OL</sub> = 50 μA	4.5 V		0.001	0.1		0.1		0.1	
		5.5 V		0.001	0.1		0.1		0.1	
V	I <sub>OL</sub> = 12 mA	3 V			0.36		0.5		0.44	
V <sub>OL</sub>		4.5 V			0.36		0.5		0.44	V
	$I_{OL} = 24 \text{ mA}$	5.5 V			0.36		0.5		0.44	
	$I_{OL} = 50 \text{ mA}^{\dagger}$	5.5 V					1.65			
	I <sub>OL</sub> = 75 mA†	5.5 V							1.65	
IJ	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.1		±1		±1	μΑ
ICC	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			2		40		20	μΑ
Ci	VI = V <sub>CC</sub> or GND	5 V		2.6						pF

<sup>†</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.



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# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

	FROM	то	T <sub>A</sub> = 25°C			SN54AC11		SN74/		
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
t <sub>PLH</sub>	A D C	V	1.5	5.5	9.5	1	11	1	10	
<sup>t</sup> PHL	A, B, or C	Y	1.5	5.5	8.5	1	10.5	1	9.5	ns

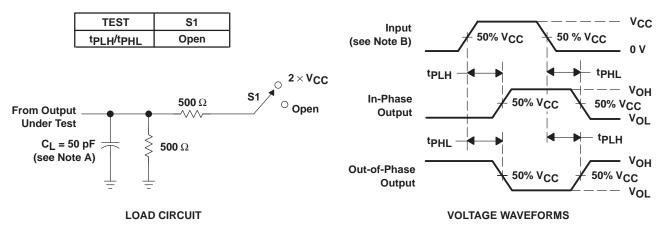
# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	то	T <sub>A</sub> = 25°C			SN54	AC11	SN74/		
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
t <sub>PLH</sub>	A B 22 C	V	1.5	4	8	1	8.5	1	8.5	
tPHL	A, B, or C	Υ	1.5	4	7	1	8	1	7.5	ns

### operating characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	$C_L = 50 \text{ pF}, \qquad \qquad f = 1 \text{ MHz}$	20	pF

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns.  $t_f \leq 2.5$  ns.
- C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms





5-Sep-2011

#### **PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
5962-87611012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-8761101CA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Call TI	
5962-8761101DA	ACTIVE	CFP	W	14	1	TBD	Call TI	Call TI	
SN74AC11D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC11DBLE	OBSOLETE	SSOP	DB	14		TBD	Call TI	Call TI	
SN74AC11DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC11DBRE4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC11DBRG4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC11DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC11DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC11DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC11DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC11DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC11N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74AC11NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74AC11NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC11NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC11NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC11PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	





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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN74AC11PWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC11PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC11PWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	
SN74AC11PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC11PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AC11PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SNJ54AC11FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54AC11J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SNJ54AC11W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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5-Sep-2011

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#### OTHER QUALIFIED VERSIONS OF SN54AC11, SN74AC11:

Catalog: SN74AC11

Automotive: SN74AC11-Q1, SN74AC11-Q1

Enhanced Product: SN74AC11-EP, SN74AC11-EP

Military: SN54AC11

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product Supports Defense, Aerospace and Medical Applications
- Military QML certified for Military and Defense Applications

### **PACKAGE MATERIALS INFORMATION**

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### TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC11DBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74AC11DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AC11NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AC11PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

www.ti.com 30-Jul-2010



\*All dimensions are nominal

7 III dilitorio di o Tiorima.								
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
SN74AC11DBR	SSOP	DB	14	2000	346.0	346.0	33.0	
SN74AC11DR	SOIC	D	14	2500	346.0	346.0	33.0	
SN74AC11NSR	SO	NS	14	2000	346.0	346.0	33.0	
SN74AC11PWR	TSSOP	PW	14	2000	346.0	346.0	29.0	

### 14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

# W (R-GDFP-F14)

### CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB



### FK (S-CQCC-N\*\*)

### LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



### N (R-PDIP-T\*\*)

### PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



### D (R-PDSO-G14)

### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



# D (R-PDSO-G14)

## PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G14)

### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
  - Sody length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



# PW (R-PDSO-G14)

### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



### **MECHANICAL DATA**

### NS (R-PDSO-G\*\*)

# 14-PINS SHOWN

#### PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



### DB (R-PDSO-G\*\*)

### PLASTIC SMALL-OUTLINE

#### **28 PINS SHOWN**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

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