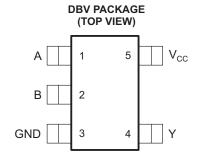
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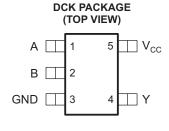
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FEATURES

- Available in Texas Instruments NanoStar[™] and NanoFree[™] Packages
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 5.3 ns at 3.3 V
- Low Power Consumption, 10-μA Max I_{CC}
- ±24-mA Output Drive at 3.3 V

- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)







See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

The SN74LVC1G132 contains one 2-input NAND gate with Schmitt-trigger inputs designed for 1.65-V to 5.5-V V_{CC} operation and performs the Boolean function $Y = \overline{A} \bullet \overline{B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

Because of Schmitt action, this device has different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.

This device can be triggered from the slowest of input ramps and still give clean jitter-free output signals.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

NanoStar[™] and NanoFree[™] package technology is a major breakthrough in IC packaging concepts, using the die as the package.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽²⁾	
	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP		SN74LVC1G132YEPR		
–40°C to 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)		SN74LVC1G132YZPR	D5_	
-40 C 10 03 C	SOT (SOT-23) – DBV	Reel of 3000	SN74LVC1G132DBVR	- C3B	
	301 (301-23) – DBV	Reel of 250	SN74LVC1G132DBVT	C3B_	
	SOT (SC-70) – DCK	Reel of 3000	SN74LVC1G132DCKR	- D5	
	301 (30-70) – DOK	Reel of 250	SN74LVC1G132DCKT	D3_	

⁽¹⁾ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

⁽²⁾ DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site. YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

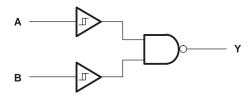
NanoStar, NanoFree are trademarks of Texas Instruments.



FUNCTION TABLE

INF	PUTS	OUTPUT				
Α	В	Y				
L	L	Н				
L	Н	Н				
Н	L	Н				
Н	Н	L				

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.5	V
VI	Input voltage range (2)		-0.5	6.5	V
Vo	Voltage range applied to any output in the high-impedance or power-off state (2)		-0.5	6.5	V
Vo	Voltage range applied to any output in the high or low state (2)(3)		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current			±50	mA
	Continuous current through V _{CC} or GND			±100	mA
		DBV package		206	
θ_{JA}	Package thermal impedance ⁽⁴⁾	DCK package		252	°C/W
		YEP/YZP package		132	
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

⁽²⁾ The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

⁽³⁾ The value of V_{CC} is provided in the recommended operating conditions table.

⁽⁴⁾ The package thermal impedance is calculated in accordance with JESD 51-7.

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Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT	
V	Complementary	Operating	1.65 5.5			
V _{CC}	Supply voltage	Data retention only	1.5		V	
V_{I}	Input voltage		0	5.5	V	
Vo	Output voltage		0	V_{CC}	V	
		V _{CC} = 1.65 V		-4		
		V _{CC} = 2.3 V		-8	mA	
I_{OH}	High-level output current	V 2V		-16		
		V _{CC} = 3 V		-24		
		$V_{CC} = 4.5 \text{ V}$		-32		
		V _{CC} = 1.65 V		4		
		$V_{CC} = 2.3 \text{ V}$		8		
I_{OL}	Low-level output current	V 2V		16	mA	
		V _{CC} = 3 V		24		
		V _{CC} = 4.5 V		32		
T _A	Operating free-air temperature		-40	85	°C	

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

SN74LVC1G132 SINGLE 2-INPUT NAND GATE WITH SCHMITT-TRIGGER INPUTS

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Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

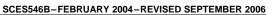
PARAMETER	TEST CONDITIONS	V _{cc}	MIN TYP(1) MAX	UNIT
		1.65 V	0.79 1.16	
V_{T+}		2.3 V	1.11 1.56	
Positive-going input threshold		3 V	1.5 1.87	V
voltage		4.5 V	2.16 2.74	
		5.5 V	2.61 3.33	
		1.65 V	0.39 0.62	
V_{T-}		2.3 V	0.58 0.87	
Negative-going input threshold		3 V	0.84 1.14	V
voltage		4.5 V	1.41 1.79	
		5.5 V	1.87 2.29	
		1.65 V	0.37 0.62	
ΔV_{T}		2.3 V	0.48 0.77	
Hysteresis		3 V	0.56 0.87	V
$(V_{T+} - V_{T-})$		4.5 V	0.71 1.04	
		5.5 V	0.71 1.11	
	$I_{OH} = -100 \mu\text{A}$	1.65 V to 5.5 V	V _{CC} - 0.1	
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2	
	$I_{OH} = -8 \text{ mA}$	2.3 V	1.9	.,
V_{OH}	I _{OH} = -16 mA	0.17	2.4	V
	I _{OH} = -24 mA	3 V	2.3	
	I _{OH} = -32 mA	4.5 V	3.8	
	I _{OL} = 100 μA	1.65 V to 5.5 V	0.1	
	I _{OL} = 4 mA	1.65 V	0.45	
	I _{OL} = 8 mA	2.3 V	0.3	.,
V_{OL}	I _{OL} = 16 mA	0.17	0.4	V
	I _{OL} = 24 mA	3 V	0.55	
	I _{OL} = 32 mA	4.5 V	0.55	
I _I A or B inputs	V _I = 5.5 V or GND	1.65 V to 5.5 V	±1	μΑ
I _{off}	V_I or $V_O = 5.5 \text{ V}$	0	±10	μΑ
I _{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	1.65 V to 5.5 V	10	μΑ
Δl _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 5.5 V	500	μΑ
C _i	V _I = V _{CC} or GND	3.3 V	3.5	pF

⁽¹⁾ All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 15 \text{ pF}$ (unless otherwise noted) (see Figure 1)

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ±0.15 V		V_{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ±0.3 V		V _{CC} = 5 V ±0.5 V		UNIT	
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
	t _{pd}	A or B	Υ	4	16	2.5	7	2	5.3	1.5	4.4	ns	





Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ or 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ±0.15 V		V _{CC} = 2.5 V ±0.2 V		V _{CC} = 3.3 V ±0.3 V		V _{CC} = 5 V ±0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	ı
t _{pd}	A or B	Y	4	16	3	7.5	2	6	2	5	ns

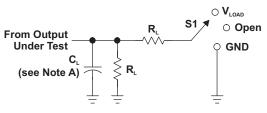
Operating Characteristics

 $T_A = 25^{\circ}C$

	PARAMETER	TEST	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	V _{CC} = 5 V	UNIT
	TANAMETER	CONDITIONS	TYP	TYP	TYP	TYP	Oitii
C_{pd}	Power dissipation capacitance	f = 10 MHz	17	18	18	20	pF



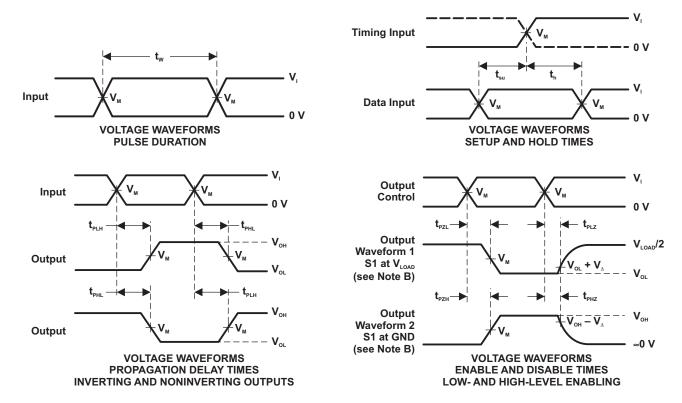
PARAMETER MEASUREMENT INFORMATION



TEST	S1
t _{PLH} /t _{PHL}	Open
t_{PLZ}/t_{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

LOAD CIRCUIT

.,	INPUTS			V		-	.,
V _{cc}	V,	t,/t,	V _M	V _{LOAD}	C _L	R _L	V _Δ
1.8 V ± 0.15 V	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	15 pF	1 M Ω	0.15 V
$2.5 \text{ V} \pm 0.2 \text{ V}$	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	15 pF	1 M Ω	0.15 V
$3.3~V~\pm~0.3~V$	3 V	≤2.5 ns	1.5 V	6 V	15 pF	1 M Ω	0.3 V
5 V ± 0.5 V	V _{cc}	≤2.5 ns	V _{cc} /2	2 × V _{cc}	15 pF	1 M Ω	0.3 V



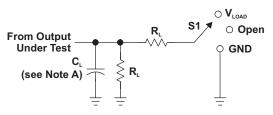
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_o = 50 Ω .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and \dot{t}_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



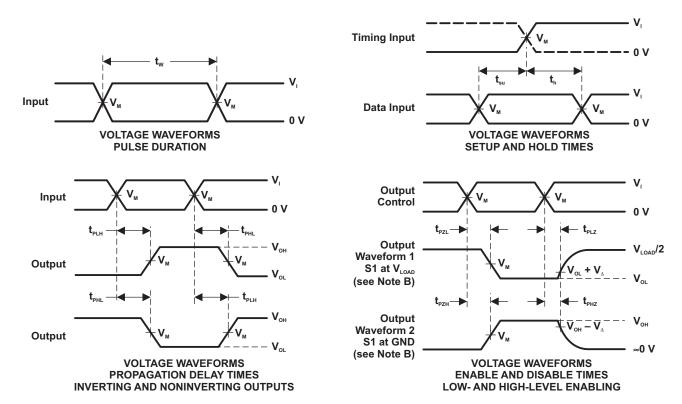
PARAMETER MEASUREMENT INFORMATION



TEST	S1
t _{PLH} /t _{PHL}	Open
t_{PLZ}/t_{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

LOAD CIRCUIT

V	INPUTS		V	V		1	V	
V _{cc}	V,	t,/t,	V _M	V _{LOAD}	C _L	$R_{\scriptscriptstyle L}$	V _A	
1.8 V ± 0.15 V	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	30 pF	1 k Ω	0.15 V	
2.5 V ± 0.2 V	V_{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	30 pF	500 Ω	0.15 V	
$3.3~V~\pm~0.3~V$	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V	
5 V ± 0.5 V	V_{cc}	≤2.5 ns	V _{cc} /2	2 × V _{cc}	50 pF	500 Ω	0.3 V	



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_o = 50 Ω .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and \dot{t}_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms



30-Jul-2011

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
74LVC1G132DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74LVC1G132DBVTE4	ACTIVE	SOT-23	DBV	5		TBD	Call TI	Call TI	
74LVC1G132DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74LVC1G132DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74LVC1G132DCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74LVC1G132DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G132DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G132DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G132DBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G132DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G132DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G132DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



PACKAGE OPTION ADDENDUM

30-Jul-2011

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL. Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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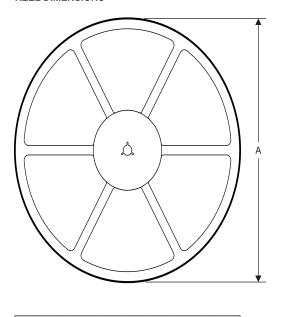
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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G132DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G132DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G132DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3

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*All dimensions are nominal

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G132DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74LVC1G132DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74LVC1G132DCKR	SC70	DCK	5	3000	180.0	180.0	18.0

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-178 Variation AA.



DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AA.



DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



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