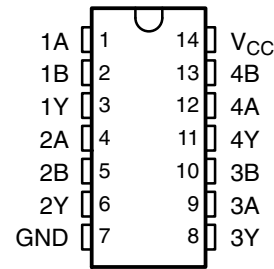


SN74ALVC00-Q1 QUADRUPLE 2-INPUT POSITIVE-NAND GATE

SCES490C – SEPTEMBER 2003 – REVISED JANUARY 2008

- Qualified for Automotive Applications
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Operates From 1.65 V to 3.6 V
- Max t_{pd} of 3 ns at 3.3 V
- ± 24 -mA Output Drive at 3.3 V
- Latch-Up Performance Exceeds 250 mA Per JESD 17

D OR PW PACKAGE
(TOP VIEW)



description/ordering information

The SN74ALVC00 quadruple 2-input positive-NAND gate is designed for 1.65-V to 3.6-V V_{CC} operation.

The device performs the Boolean function $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

ORDERING INFORMATION†

| T_A | PACKAGE‡ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|------------|---------------|-----------------------|------------------|
| | SOIC – D | Tape and reel | | |
| –40°C to 85°C | TSSOP – PW | Tape and reel | SN74ALVC00IDRQ1 | ALVC00I |
| | | | SN74ALVC00IPWRQ1 | VA00I |

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

‡ Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTION TABLE
(each gate)

| INPUTS | | OUTPUT Y |
|--------|---|-------------|
| A | B | |
| H | H | L |
| L | X | H |
| X | L | H |

logic diagram, each gate (positive logic)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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SN74ALVC00-Q1

QUADRUPLE 2-INPUT POSITIVE-NAND GATE

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | |
|--|----------------------------|
| Supply voltage range, V_{CC} | -0.5 V to 4.6 V |
| Input voltage range, V_I (see Note 1) | -0.5 V to 4.6 V |
| Output voltage range, V_O (see Notes 1 and 2) | -0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$) | -50 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | -50 mA |
| Continuous output current, I_O | ± 50 mA |
| Continuous current through V_{CC} or GND | ± 100 mA |
| Package thermal impedance, θ_{JA} (see Note 3): D package | 86°C/W |
| PW package | 113°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

2. This value is limited to 4.6 V maximum.

3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

| | | MIN | MAX | UNIT |
|---------------------|------------------------------------|-----------------------------|----------------------|------|
| V_{CC} | Supply voltage | 1.65 | 3.6 | V |
| V_{IH} | High-level input voltage | $V_{CC} = 1.65$ V to 1.95 V | $0.65 \times V_{CC}$ | V |
| | | $V_{CC} = 2.3$ V to 2.7 V | 1.7 | |
| | | $V_{CC} = 2.7$ V to 3.6 V | 2 | |
| V_{IL} | Low-level input voltage | $V_{CC} = 1.65$ V to 1.95 V | $0.35 \times V_{CC}$ | V |
| | | $V_{CC} = 2.3$ V to 2.7 V | 0.7 | |
| | | $V_{CC} = 2.7$ V to 3.6 V | 0.8 | |
| V_I | Input voltage | 0 | 3.6 | V |
| V_O | Output voltage | 0 | V_{CC} | V |
| I_{OH} | High-level output current | $V_{CC} = 1.65$ V | -4 | mA |
| | | $V_{CC} = 2.3$ V | -12 | |
| | | $V_{CC} = 2.7$ V | -12 | |
| | | $V_{CC} = 3$ V | -24 | |
| I_{OL} | Low-level output current | $V_{CC} = 1.65$ V | 4 | mA |
| | | $V_{CC} = 2.3$ V | 12 | |
| | | $V_{CC} = 2.7$ V | 12 | |
| | | $V_{CC} = 3$ V | 24 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 5 | ns/V |
| T_A | Operating free-air temperature | -40 | 85 | °C |

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP† | MAX | UNIT |
|--------------------------|--|-----------------|----------------------|------|------|------|
| V _{OH} | I _{OH} = -100 μA | 1.65 V to 3.6 V | V _{CC} -0.2 | | | V |
| | I _{OH} = -4 mA | 1.65 V | 1.2 | | | |
| | I _{OH} = -6 mA | 2.3 V | 2 | | | |
| | I _{OH} = -12 mA | 2.3 V | 1.7 | | | |
| | | 2.7 V | 2.2 | | | |
| | | 3 V | 2.4 | | | |
| I _{OH} = -24 mA | 3 V | 2 | | | | |
| V _{OL} | I _{OL} = 100 μA | 1.65 V to 3.6 V | | | 0.2 | V |
| | I _{OL} = 4 mA | 1.65 V | | | 0.45 | |
| | I _{OL} = 6 mA | 2.3 V | | | 0.4 | |
| | I _{OL} = 12 mA | 2.3 V | | | 0.7 | |
| | | 2.7 V | | | 0.4 | |
| | I _{OL} = 24 mA | 3 V | | | 0.55 | |
| I _I | V _I = V _{CC} or GND | 3.6 V | | | ±5 | μA |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 3.6 V | | | 10 | μA |
| ΔI _{CC} | One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND | 3 V to 3.6 V | | | 750 | μA |
| C _i | V _I = V _{CC} or GND | 3.3 V | | 4.5 | | pF |

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 1.8 V ± 0.15 V | | V _{CC} = 2.5 V ± 0.2 V | | V _{CC} = 2.7 V | | V _{CC} = 3.3 V ± 0.3 V | | UNIT |
|-----------------|--------------|-------------|----------------------------------|-----|---------------------------------|-----|-------------------------|-----|---------------------------------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{pd} | A or B | Y | 1 | 4.4 | 1 | 2.8 | 3.2 | | 0.5 | 3 | ns |

operating characteristics, T_A = 25°C

| PARAMETER | TEST CONDITIONS | V _{CC} = 1.8 V | V _{CC} = 2.5 V | V _{CC} = 3.3 V | UNIT |
|--|--------------------------------|-------------------------|-------------------------|-------------------------|------|
| | | TYP | TYP | TYP | |
| C _{pd} Power dissipation capacitance per gate | C _L = 0, f = 10 MHz | 20 | 21 | 23 | pF |

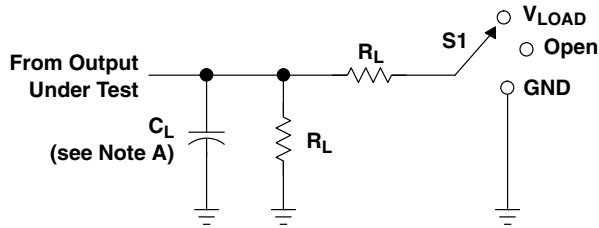


SN74ALVC00-Q1

QUADRUPLE 2-INPUT POSITIVE-NAND GATE

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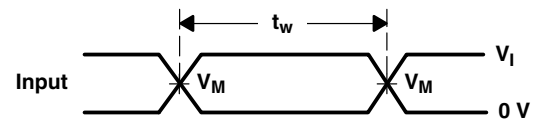
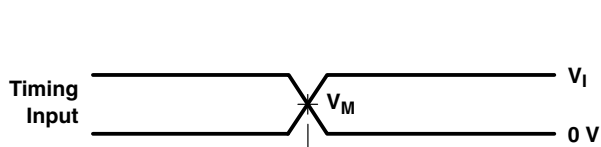
PARAMETER MEASUREMENT INFORMATION



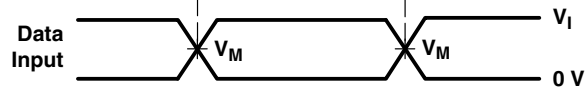
| TEST | S1 |
|-------------------|------------|
| t_{pd} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

LOAD CIRCUIT

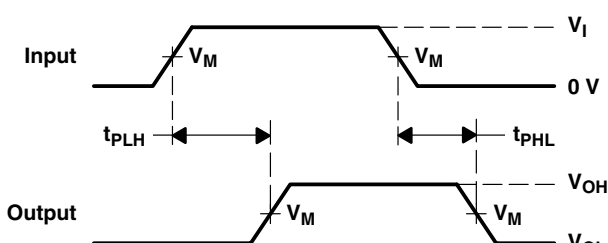
| V_{CC} | INPUT | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|--------------------|----------|-----------------------|------------|-------------------|-------|--------------|--------------|
| | V_I | t_r/t_f | | | | | |
| $1.8 V \pm 0.15 V$ | V_{CC} | $\leq 2 \text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k Ω | 0.15 V |
| $2.5 \pm 0.2 V$ | V_{CC} | $\leq 2 \text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 2.7 V | 2.7 V | $\leq 2.5 \text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| $3.3 V \pm 0.3 V$ | 2.7 V | $\leq 2.5 \text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |



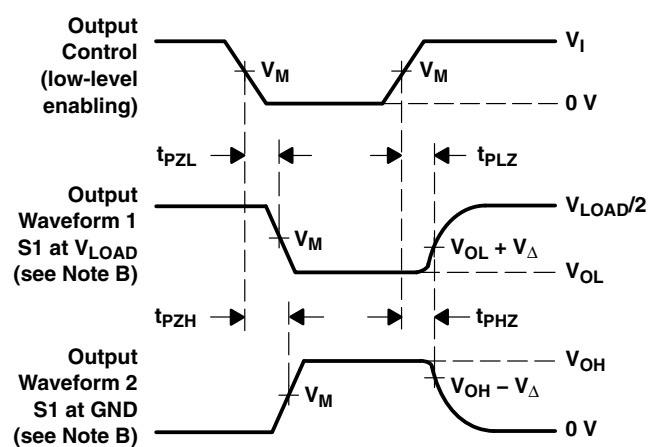
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|--------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN74ALVC00IDRG4Q1 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALVC00IDRQ1 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALVC00IPWRG4Q1 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALVC00IPWRQ1 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74ALVC00-Q1 :

- Catalog: [SN74ALVC00](#)
- Enhanced Product: [SN74ALVC00-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

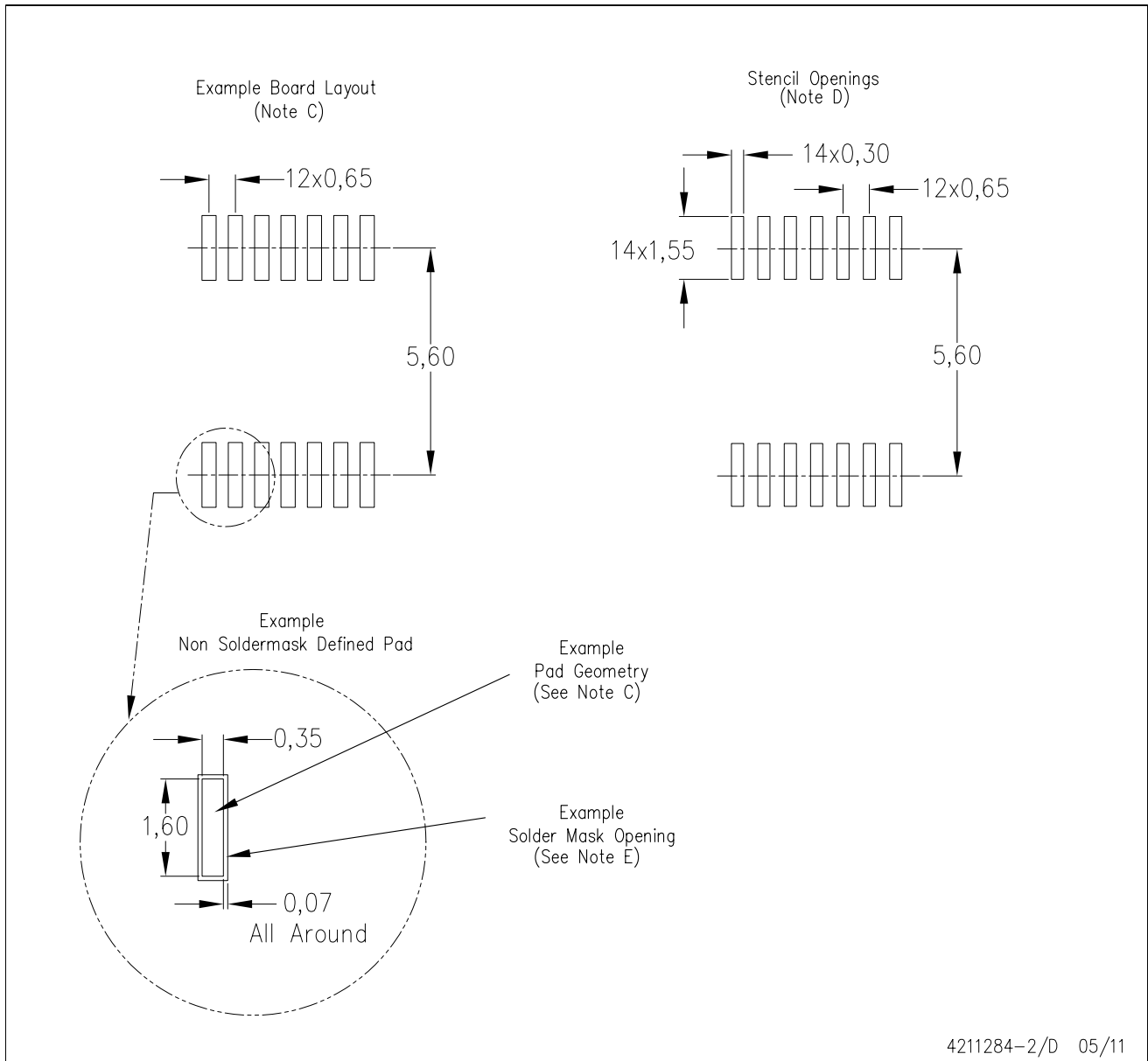


4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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