SCLS534C - AUGUST 2003 - REVISED APRIL 2008

Qualified for Automotive Applications

 ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)

- 2-V to 5.5-V V<sub>CC</sub> Operation
- Typical V<sub>OLP</sub> (Output Ground Bounce)
  <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Typical V<sub>OHV</sub> (Output V<sub>OH</sub> Undershoot)
  >2.3 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Support Mixed-Mode Voltage Operation on All Ports

### description/ordering information

The SN74LV86A is a quadruple 2-input exclusive-OR gate designed for 2-V to 5.5-V  $V_{CC}$  operation.

This device contains four independent 2-input exclusive-OR gates. It performs the Boolean function  $Y = A \oplus B$  or  $Y = \overline{AB} + A\overline{B}$  in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

#### **ORDERING INFORMATION<sup>†</sup>**

TA	T <sub>A</sub> PACKAGE <sup>‡</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING	
–40°C to 105°C	TSSOP – PW	Tape and reel	SN74LV86ATPWRQ1	LV86AT	

<sup>†</sup> For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.

<sup>‡</sup>Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.

**FUNCTION TABLE** 

	(each g	ate)
INP	UTS	OUTPUT
Α	В	Y
L	L	L
L	Н	Н
Н	L	Н
Н	Н	L



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

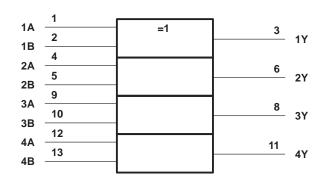
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



P	PW PACKAGE (TOP VIEW)									
1A [	1	υ	14							
1B [	2		13	] V <sub>CC</sub> ] 4B						
1Y [	3		12	4A						
2A [	4		11	] 4Y						
2B [	5		10	] 3B						
2Y [	6		9	] 3A						
GND [	7		8	] 3Y						
	_			,						

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## logic symbol<sup>†</sup>



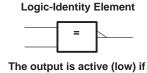
<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



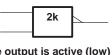
These are five equivalent exclusive-OR symbols valid for an 'LV86A gate in positive logic; negation can be shown at any two ports.



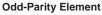
all inputs stand at the same

logic level (i.e., A = B).

**Even-Parity Element** 



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.





The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>‡</sup>

Supply voltage range, V <sub>CC</sub> Input voltage range, V <sub>I</sub> (see Note 1) Voltage range applied to any output in the high-impedance	
or power-off state, $V_{\Omega}$ (see Note 1)	–0.5 V to 7 V
Output voltage range, Vo (see Notes 1 and 2)0.8	
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$	±25 mA
Continuous current through V <sub>CC</sub> or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3)	
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 5.5 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51-7.



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## recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		2	5.5	V	
		$V_{CC} = 2 V$	1.5			
	Libely Level Consistent for the sec	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	$V_{CC} \times 0.7$			
VIH	High-level input voltage	$V_{CC} = 3 V \text{ to } 3.6 V$	$V_{CC} \times 0.7$		V	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$V_{CC} \times 0.7$			
		$V_{CC} = 2 V$		0.5		
.,		V <sub>CC</sub> = 2.3 V to 2.7 V		$V_{CC} \times 0.3$		
VIL	Low-level input voltage	$V_{CC} = 3 \vee to 3.6 \vee$		$V_{CC} \times 0.3$	V	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		$V_{CC} \times 0.3$		
VI	Input voltage	-	0	5.5	V	
VO	Output voltage		0	V <sub>CC</sub>	V	
		$V_{CC} = 2 V$		-50	μΑ	
	High-level output current	$V_{CC}$ = 2.3 V to 2.7 V		-2	mA	
юн		V <sub>CC</sub> = 3 V to 3.6 V		-6		
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		-12		
		V <sub>CC</sub> = 2 V		50	μΑ	
		V <sub>CC</sub> = 2.3 V to 2.7 V		2		
IOL	Low-level output current	V <sub>CC</sub> = 3 V to 3.6 V		6	mA	
		$V_{CC} = 4.5 V \text{ to } 5.5 V$		12		
		V <sub>CC</sub> = 2.3 V to 2.7 V	0	200		
$\Delta t / \Delta v$	Input transition rise or fall rate	V <sub>CC</sub> = 3 V to 3.6 V	0	100	ns/V	
		V <sub>CC</sub> = 4.5 V to 5.5 V	0	20		
TA	Operating free-air temperature		-40	105	°C	

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	Vcc	MIN	TYP	MAX	UNIT
	I <sub>OH</sub> = -50 μA	2 V to 5.5 V	V <sub>CC</sub> -0.1			
V <sub>OH</sub>	$I_{OH} = -2 \text{ mA}$	2.3 V	2			
	$I_{OH} = -6 \text{ mA}$	3 V	2.48			V
	$I_{OH} = -12 \text{ mA}$	4.5 V	3.8			
	I <sub>OL</sub> = 50 μA	2 V to 5.5 V			0.1	
	I <sub>OL</sub> = 2 mA	2.3 V			0.4	
VOL	I <sub>OL</sub> = 6 mA	3 V			0.44	V
	I <sub>OL</sub> = 12 mA	4.5 V			0.55	
lj –	$V_{I} = 5.5 V \text{ or GND}$	0 to 5.5 V			±1	μA
ICC	$V_{I} = V_{CC} \text{ or GND},$ IO =	= 0 5.5 V			20	μΑ
l <sub>off</sub>	$V_{I}$ or $V_{O} = 0$ to 5.5 V	0			5	μΑ
Ci	$V_I = V_{CC}$ or GND	3.3 V		1.4		pF



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switching characteristics over recommended operating free-air temperature range,  $V_{CC}$  = 2.5 V  $\pm$  0.2 V (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	то	LOAD	Τ <sub>4</sub>	λ = 25°C	;			
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	UNIT
<sup>t</sup> pd	A or B	Y	C <sub>L</sub> = 50 pF		10.5	22.6	1	26.5	ns

# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

	FROM	то	LOAD	Τ,	ς = 25°C	;			
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	UNIT
<sup>t</sup> pd	A or B	Y	C <sub>L</sub> = 50 pF		7.4	14.5	1	16.5	ns

# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

	FROM	то	LOAD	Τį	λ = 25°C	;			
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	UNIT
<sup>t</sup> pd	A or B	Y	C <sub>L</sub> = 50 pF		5.3	8.8	1	10	ns

## noise characteristics, $V_{CC}$ = 3.3 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

	PARAMETER	MIN	TYP	MAX	UNIT
VOL(P)	Quiet output, maximum dynamic V <sub>OL</sub>		0.2	0.8	V
VOL(V)	Quiet output, minimum dynamic V <sub>OL</sub>		-0.1	-0.8	V
VOH(V)	Quiet output, minimum dynamic V <sub>OH</sub>		3.1		V
VIH(D)	High-level dynamic input voltage	2.31			V
V <sub>IL(D)</sub>	Low-level dynamic input voltage			0.99	V

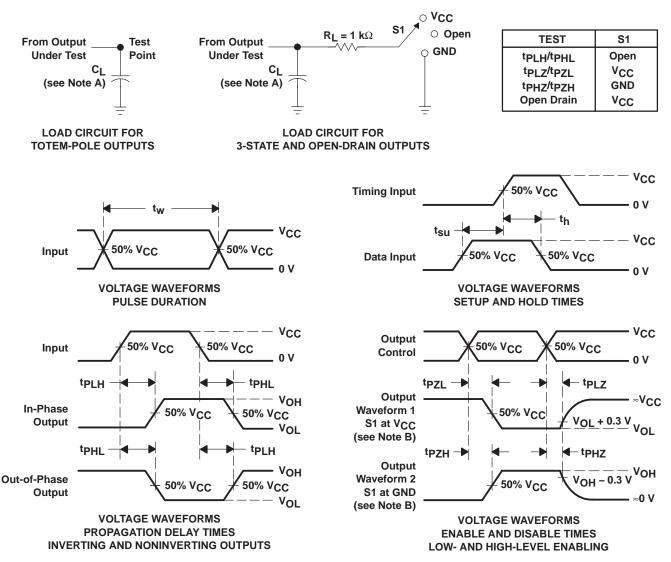
NOTE 5: Characteristics are for surface-mount packages only.

## operating characteristics, T<sub>A</sub> = 25°C

	PARAMETER	TEST CO	V <sub>CC</sub>	TYP	UNIT	
	Dower dissinction consciones	C <sub>I</sub> = 50 pF,	£ 10 MU-	3.3 V	8.4	~ <b>F</b>
Cpd	Power dissipation capacitance	CL = 50 pF,	f = 10 MHz	5 V	8.8	pF



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## PARAMETER MEASUREMENT INFORMATION

NOTES: A. C<sub>I</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \le 1$  MHz,  $Z_{O} = 50 \Omega$ ,  $t_{f} \le 3$  ns,  $t_{f} \le 3$  ns.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E.  $t_{PI7}$  and  $t_{PH7}$  are the same as  $t_{dis}$ .
- F.  $t_{P7I}$  and  $t_{P7H}$  are the same as  $t_{en}$ .
- G. tpHL and tpLH are the same as tpd.

### Figure 1. Load Circuit and Voltage Waveforms





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### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN74LV86ATPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV86ATPWRQ1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### OTHER QUALIFIED VERSIONS OF SN74LV86A-Q1 :

Catalog: SN74LV86A

Enhanced Product: SN74LV86A-EP

# PACKAGE OPTION ADDENDUM



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12-Oct-2011

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Enhanced Product Supports Defense, Aerospace and Medical Applications

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



A. An integration of the information o

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153



# LAND PATTERN DATA



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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