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- Qualified for Automotive Applications
- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 40-µA Max I_{CC}
- Typical t_{pd} = 14 ns
- ±4-mA Output Drive at 5 V
- Low Input Current of 1 μA Max
- Operation From Very Slow Input Transitions

- Temperature-Compensated Threshold Levels
- High Noise Immunity
- Same Pinouts as 'HC00

D OR PW PACKAGE (TOP VIEW) 14 VCC 1A [1B **1**2 13 🛮 4B 1Y [12 AA 2A 11 T 4Y 2B 🛮 5 10 3B 9 🛮 3A 2Y [**GND** 8U 3Y

description/ordering information

Each circuit functions as a NAND gate, but because of the Schmitt action, it has different input threshold levels for positive- and negative-going signals. The SN74HC132 performs the Boolean function $Y = \overline{A} \bullet \overline{B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

This circuit is temperature compensated and can be triggered from the slowest of input ramps and still give clean jitter-free output signals.

ORDERING INFORMATION[†]

T _A	PACKA	GE‡	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	SOIC - D	Reel of 2500	SN74HC132QDRQ1	HC132Q1
-40 C to 125 C		Reel of 2000	SN74HC132QPWRQ1	HC132Q1

[†] For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.

FUNCTION TABLE (each gate)

INP	JTS	OUTPUT
Α	В	Υ
Н	Н	L
L	X	Н
X	L	Н



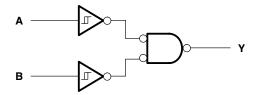
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



[‡] Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 7 V
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{CC}) (see Note 1)	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC}) (see Note 1)	±20 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±25 mA
Continuous current through V _{CC} or GND	±50 mA
Package thermal impedance, θ _{JA} (see Note 2): D package	86°C/W
PW package	113°C/W
Storage temperature range, T _{stg}	. −65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2	5	6	V
		V _{CC} = 2 V	1.5			
V_{IH}	High-level input voltage	$V_{CC} = 4.5 \text{ V}$	3.15	3.15		V
		V _{CC} = 6 V	4.2			
		V _{CC} = 2 V			0.5	
V_{IL}	Low-level input voltage	$V_{CC} = 4.5 \text{ V}$			1.35	V
	V _{CC} = 6 V			1.8		
VI	Input voltage		0		V_{CC}	V
Vo	Output voltage		0		V_{CC}	V
T _A	Operating free-air temperature		-40		125	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEGT COMPLETE	NIO	v _{cc}	Т	_A = 25°C	;	NAIN!	MAY	
PARAMETER	TEST CONDITION	TEST CONDITIONS					MIN	MAX	UNIT
			2 V	0.7	1.2	1.5	0.7	1.5	
V_{T+}			4.5 V	1.55	2.5	3.15	1.55	3.15	V
			6 V	2.1	3.3	4.2	2.1	4.2	
			2 V	0.3	0.6	1	0.3	1	
V_{T-}			4.5 V	0.9	1.6	2.45	0.9	2.45	V
		6 V	1.2	2	3.2	1.2	3.2		
			2 V	0.2	0.6	1.2	0.2	1.2	
$V_{T+} - V_{T-}$		4.5 V	0.4	0.9	2.1	0.4	2.1	V	
		6 V	0.5	1.3	2.5	0.5	2.5		
	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	2 V	1.9	1.998		1.9		
			4.5 V	4.4	4.499		4.4		
V _{OH}			6 V	5.9	5.999		5.9		V
		$I_{OH} = -4 \text{ mA}$	4.5 V	3.98	4.3		3.7		
		$I_{OH} = -5.2 \text{ mA}$	6 V	5.48	5.8		5.2		
			2 V		0.002	0.1		0.1	
		$I_{OL} = 20 \mu A$	4.5 V		0.001	0.1		0.1	v
V_{OL}	$V_{I} = V_{IH}$ or V_{IL}		6 V		0.001	0.1		0.1	
		I _{OL} = 4 mA	4.5 V		0.17	0.26		0.4	
		I _{OL} = 5.2 mA	6 V		0.15	0.26		0.4	
l _l	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000	nA
I _{CC}	$V_I = V_{CC}$ or 0,	I _O = 0	6 V			2		40	μΑ
C _i			2 V to 6 V		3	10		10	pF

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	то	\ , \	T _A = 25°C			54151		LINUT
PARAMETER	(INPUT)	(OUTPUT)	V _{CC}	MIN	TYP	MAX	MIN	MAX	UNIT
			2 V		60	120		186	
t _{pd}	A or B	Υ	4.5 V		18	25		37	ns
·			6 V		14	21		32	
			2 V		28	75		110	
t _t		Any	4.5 V		8	15		22	ns
			6 V		6	13		19	

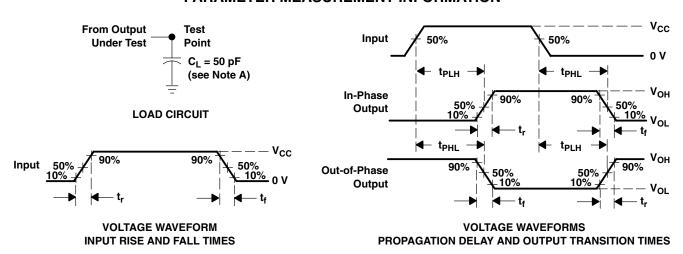
operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per gate	No load	20	pF



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PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and test-fixture capacitance.

- B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z_{O} = 50 Ω , t_{r} = 6 ns, t_{f} = 6 ns.
- C. The outputs are measured one at a time with one input transition per measurement.
- D. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms



19-Oct-2011

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74HC132QDRG4Q1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC132QDRQ1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC132QPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC132QPWRQ1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74HC132-Q1:





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Military: SN54HC132

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
 - Sody length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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