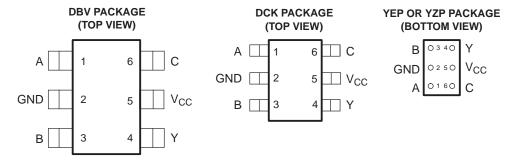
www.ti.com

SCES439D-APRIL 2003-REVISED JULY 2006

#### **FEATURES**

- Available in the Texas Instruments NanoStar <sup>™</sup> and NanoFree<sup>™</sup> Packages
- Supports 5-V V<sub>CC</sub> Operation
- Inputs Accept Voltages to 5.5 V
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

#### **DESCRIPTION/ORDERING INFORMATION**

The SN74LVC1G386 performs the Boolean function  $Y = A \oplus B \oplus C$  in positive logic.

NanoStar<sup>™</sup> and NanoFree<sup>™</sup> package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING(2)
	NanoStar™ - WCSP (DSBGA) 0.23-mm Large Bump - YEP	Tana and roal	SN74LVC1G386YEPR	Co
-40°C to 85°C	NanoFree <sup>™</sup> – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Tape and reel	SN74LVC1G386YZPR	C8_
	SOT (SOT-23) - DBV	Tape and reel	SN74LVC1G386DBVR	CC6_
	SOT (SC-70) - DCK	Tape and reel	SN74LVC1G386DCKR	C8_

<sup>(1)</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar, NanoFree are trademarks of Texas Instruments.

<sup>(2)</sup> DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site. YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, ● = Pb-free).



#### **FUNCTION TABLE**

	INPUTS		OUTPUT
Α	В	С	Υ
L	L	L	L
L	L	Н	Н
L	Н	L	Н
L	Н	Н	L
Н	L	L	Н
Н	L	Н	L
Н	Н	L	L
Н	Н	Н	Н

#### **LOGIC DIAGRAM (POSITIVE LOGIC)**



## **Absolute Maximum Ratings**(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage range		-0.5	6.5	V
VI	Input voltage range (2)		-0.5	6.5	V
Vo	Voltage range applied to any output in the high-imp	pedance or power-off state (2)	-0.5	6.5	V
Vo	Voltage range applied to any output in the high or	low state <sup>(2)(3)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50	mA
I <sub>OK</sub>	Output clamp current V <sub>O</sub> < 0			<b>-</b> 50	mA
Io	Continuous output current			±50	mA
	Continuous current through V <sub>CC</sub> or GND			±100	mA
		DBV package		165	
$\theta_{JA}$	Package thermal impedance (4)	DCK package		259	°C/W
	YEP/YZP package			123	
T <sub>stg</sub>	Storage temperature range			150	°C

<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

 <sup>(2)</sup> The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 (3) The value of V<sub>CC</sub> is provided in the recommended operating conditions table.
 (4) The package thermal impedance is calculated in accordance with JESD 51-7.



SCES439D-APRIL 2003-REVISED JULY 2006

# Recommended Operating Conditions<sup>(1)</sup>

			MIN	MAX	UNIT
W	Cumply yeltogo	Operating	1.65	5.5	V
$V_{CC}$	Supply voltage	Data retention only	1.5		V
		V <sub>CC</sub> = 1.65 V to 1.95 V	$0.65 \times V_{CC}$		
V	High level input voltage	$V_{CC}$ = 2.3 V to 2.7 V	1.7		V
$V_{IH}$	High-level input voltage	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	2		V
		V <sub>CC</sub> = 4.5 V to 5.5 V	$0.7 \times V_{CC}$		
		V <sub>CC</sub> = 1.65 V to 1.95 V		$0.35 \times V_{CC}$	
V	Low level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	V
$V_{IL}$	Low-level input voltage	V <sub>CC</sub> = 3 V to 3.6 V		0.8	V
		V <sub>CC</sub> = 4.5 V to 5.5 V		$0.3 \times V_{CC}$	
VI	Input voltage		0	5.5	V
Vo	Output voltage		0	V <sub>CC</sub>	V
		V <sub>CC</sub> = 1.65 V		-4	
		V <sub>CC</sub> = 2.3 V		-8	
$I_{OH}$	High-level output current	vel output current $V_{CC} = 3 \text{ V}$		-16	mA
				-24	
		V <sub>CC</sub> = 4.5 V		-32	
		V <sub>CC</sub> = 1.65 V		4	
		V <sub>CC</sub> = 2.3 V		8	
$I_{OL}$	Low-level output current	V 2.V		16	mA
		V <sub>CC</sub> = 3 V		24	
		V <sub>CC</sub> = 4.5 V	32		
		$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}, 2.5 \text{ V} \pm 0.2 \text{ V}$		20	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		ns/V	
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		5	
T <sub>A</sub>	Operating free-air temperature	,	-40	85	°C

<sup>(1)</sup> All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



#### **Electrical Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>cc</sub>	MIN TYP(1) MAX	UNIT	
	$I_{OH} = -100 \mu A$	1.65 V to 5.5 V	V <sub>CC</sub> - 0.1		
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2		
V <sub>OH</sub>	$I_{OH} = -8 \text{ mA}$	2.3 V	1.9	V	
VOH	$I_{OH} = -16 \text{ mA}$	3 V	2.4	V	
	$I_{OH} = -24 \text{ mA}$	3 V	2.3		
	$I_{OH} = -32 \text{ mA}$	4.5 V	3.8		
	$I_{OL} = 100  \mu A$	1.65 V to 5.5 V	0.1		
	$I_{OL} = 4 \text{ mA}$	1.65 V	0.45		
V	$I_{OL} = 8 \text{ mA}$	2.3 V	0.3	V	
V <sub>OL</sub>	$I_{OL} = 16 \text{ mA}$	3 V 0.5		-	
	$I_{OL} = 24 \text{ mA}$				
	$I_{OL} = 32 \text{ mA}$	4.5 V	0.55		
I <sub>I</sub> All inputs	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V	±5	μΑ	
I <sub>off</sub>	$V_I$ or $V_O = 5.5 \text{ V}$	0	±10	μΑ	
Icc	$V_I = 5.5 \text{ V or GND}, \qquad I_O = 0$	1.65 V to 5.5 V	10	μΑ	
$\Delta I_{CC}$	One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND	3 V to 5.5 V	500	μΑ	
C <sub>i</sub>	$V_I = V_{CC}$ or GND	3.3 V	3.5	pF	

<sup>(1)</sup> All typical values are at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C.

## **Switching Characteristics**

over recommended operating free-air temperature range,  $C_L$  = 15 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO (OUTPUT)	V <sub>CC</sub> = ± 0.	1.8 V 15 V	V <sub>CC</sub> = ± 0.		V <sub>CC</sub> = ± 0.		۷ <sub>CC</sub> = ± 0.		UNIT
	(INPUT)	(001F01)	MIN	MIN MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A, B, or C	Y	3	9.4	1.3	5	0.8	4.5	0.5	3.5	ns

### **Switching Characteristics**

over recommended operating free-air temperature range,  $C_L = 30 \text{ pF}$  or 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = ± 0.	1.8 V 15 V	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		UNIT				
	(INPUT)	(0011 01)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A, B, or C	Y	3.5	12	1.8	5.5	1.3	5	1	4	ns

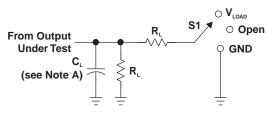
### **Operating Characteristics**

 $T_A = 25^{\circ}C$ 

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V		V <sub>CC</sub> = 5 V	UNIT
			TYP	TYP	TYP	TYP	
$C_{pd}$	Power dissipation capacitance	f = 10 MHz	17.5	18	19	22	pF



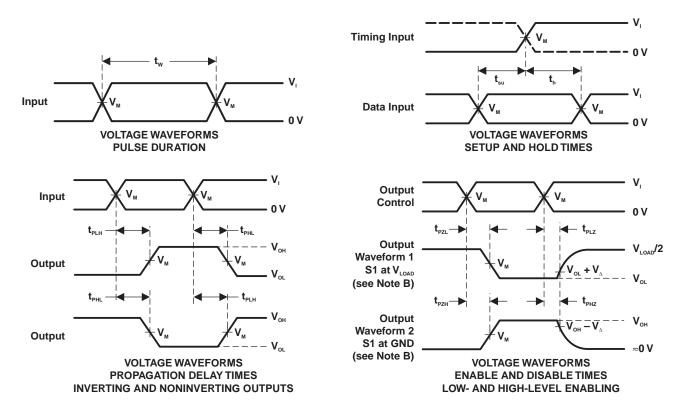
#### PARAMETER MEASUREMENT INFORMATION



TEST	S1
t <sub>PZL</sub> (see Notes E and F)	V <sub>LOAD</sub>
t <sub>PLZ</sub> (see Notes E and G)	$V_{\scriptscriptstyle LOAD}$
t <sub>PHZ</sub> /t <sub>PZH</sub>	V <sub>LOAD</sub>

LOAD CIRCUIT

.,	INI	PUTS		.,		_	.,
V <sub>cc</sub>	V,	t,/t,	V <sub>M</sub>	V <sub>LOAD</sub>	C <sub>∟</sub>	R <sub>∟</sub>	V <sub>Δ</sub>
$1.8~\textrm{V}\pm0.15~\textrm{V}$	V <sub>cc</sub>	≤2 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	15 pF	<b>1 M</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	V <sub>cc</sub>	≤2 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	15 pF	<b>1 M</b> Ω	0.15 V
3.3 V $\pm$ 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	15 pF	<b>1 Μ</b> Ω	0.3 V
5 V $\pm$ 0.5 V	V <sub>cc</sub>	≤2.5 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	15 pF	<b>1 Μ</b> Ω	0.3 V



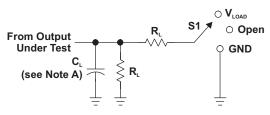
NOTES: A. C, includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators have the following characteristics: PRR ≤ 10 MHz, Z₀ = 50 Ω.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. Because this device has open-drain outputs,  $t_{Pl7}$  and  $t_{P7l}$  are the same as  $t_{PD}$ .
- F.  $t_{PZL}$  is measured at  $V_{M}$ .
- G.  $t_{PLZ}$  is measured at  $V_{OL} + V_{\Delta}$ .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



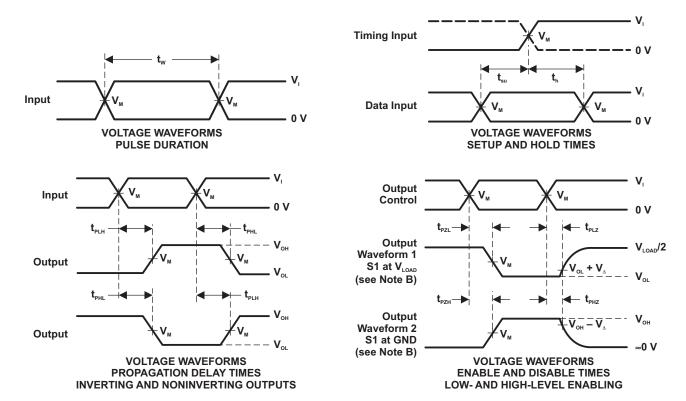
#### PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{\scriptscriptstyle PLH}/t_{\scriptscriptstyle PHL}$	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	<b>V</b> <sub>LOAD</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

LOAD CIRCUIT

V	INPUTS		V	V		1	V
V <sub>cc</sub>	V,	t,/t,	V <sub>M</sub>	<b>V</b> <sub>LOAD</sub>	C <sub>L</sub>	$R_{\scriptscriptstyle L}$	V <sub>A</sub>
1.8 V ± 0.15 V	V <sub>cc</sub>	≤2 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V ± 0.2 V	$V_{cc}$	≤2 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	30 pF	500 Ω	0.15 V
$3.3~V~\pm~0.3~V$	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	$V_{cc}$	≤2.5 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	50 pF	<b>500</b> Ω	0.3 V



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>o</sub> = 50  $\Omega$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{\text{PLZ}}$  and  $\dot{t}_{\text{PHZ}}$  are the same as  $t_{\text{dis}}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms





3-Mar-2012

#### **PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
74LVC1G386DBVRE4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74LVC1G386DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74LVC1G386DCKRE4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74LVC1G386DCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G386DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G386DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G386DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G386DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G386YZPR	ACTIVE	DSBGA	YZP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



## **PACKAGE OPTION ADDENDUM**

3-Mar-2012

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

# PACKAGE MATERIALS INFORMATION

www.ti.com 2-Mar-2012

## TAPE AND REEL INFORMATION

#### **REEL DIMENSIONS**



#### **TAPE DIMENSIONS**



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### TAPE AND REEL INFORMATION

#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G386DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G386DCKR	SC70	DCK	6	3000	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3
SN74LVC1G386DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G386DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G386YZPR	DSBGA	YZP	6	3000	180.0	8.4	1.02	1.52	0.63	4.0	8.0	Q1

www.ti.com 2-Mar-2012



\*All dimensions are nominal

7 til difficilolorio dio ficilimai							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G386DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74LVC1G386DCKR	SC70	DCK	6	3000	202.0	201.0	28.0
SN74LVC1G386DRYR	SON	DRY	6	5000	180.0	180.0	30.0
SN74LVC1G386DSFR	SON	DSF	6	5000	180.0	180.0	30.0
SN74LVC1G386YZPR	DSBGA	YZP	6	3000	220.0	220.0	34.0

# DBV (R-PDSO-G6)

# PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- Falls within JEDEC MO-178 Variation AB, except minimum lead width.



# DBV (R-PDSO-G6)

# PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



# DCK (R-PDSO-G6)

# PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AB.





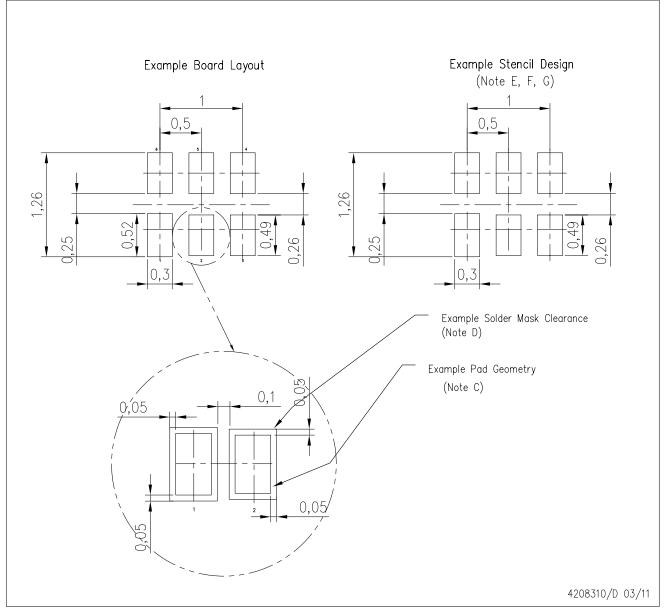
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. SON (Small Outline No-Lead) package configuration.
- The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
- E. This package complies to JEDEC MO-287 variation UFAD.
- $frac{f}{K}$  See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.



# DRY (S-PUSON-N6)

### PLASTIC SMALL OUTLINE NO-LEAD



- NOTES: A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
  - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
  - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.





NOTES: All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.

- B. This drawing is subject to change without notice.
  C. SON (Small Outline No-Lead) package configuration.
  D. This package complies to JEDEC MO-287 variation X2AAF.





# PLASTIC SMALL OUTLINE NO-LEAD



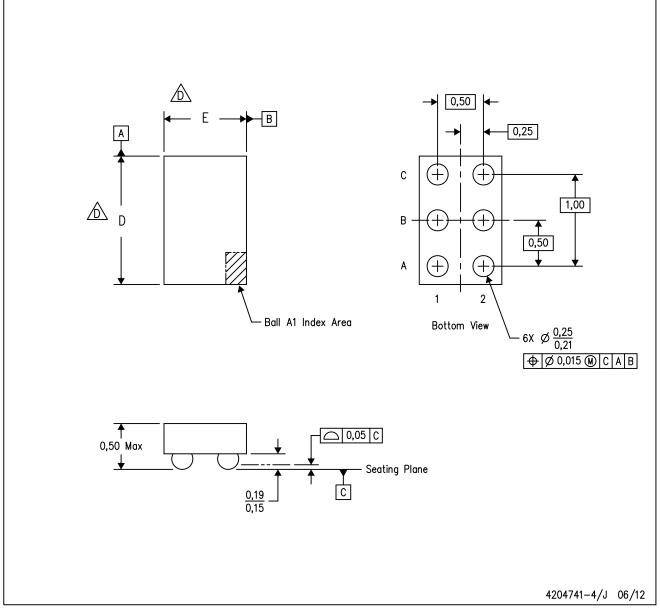
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
- E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
- H. Component placement force should be minimized to prevent excessive paste block deformation.



YZP (R-XBGA-N6)

DIE-SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.
- The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
- E. This package is a Pb-free solder ball design. Refer to the 6 YEP package (drawing 4204725) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.



#### **IMPORTANT NOTICE**

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

Applications

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

www.ti.com/automotive
www.ti.com/communications
www.ti.com/computers
www.ti.com/consumer-apps
www.ti.com/energy
www.ti.com/industrial
www.ti.com/medical
www.ti.com/security
www.ti.com/space-avionics-defense
www.ti.com/video

Wireless Connectivity <u>www.ti.com/wirelessconnectivity</u>

OMAP Mobile Processors www.ti.com/omap

**Products** 

TI E2E Community Home Page

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2012, Texas Instruments Incorporated

e2e.ti.com