

CD54HC7266, CD74HC7266

Data sheet acquired from Harris Semiconductor SCHS219D

August 1997 - Revised September 2003

High-Speed CMOS Logic Quad 2-Input EXCLUSIVE NOR Gate

Features

- Four Independent EXCLUSIVE NOR Gates
- · Buffered Inputs and Outputs
- · Logical Comparators
- · Parity Generators and Checkers
- · Adders/Subtracters
- Fanout (Over Temperature Range)
 - Standard Outputs........... 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range ... -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: N_{IL} = 30%, N_{IH} = 30%of V_{CC} at V_{CC} = 5V

Description

The 'HC7266 contains four independent Exclusive NOR gates in one package. They provide the system designer with a means for implementation of the EXCLUSIVE NOR function.

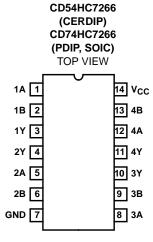
This device is functionally the same as the TTL226. They differ in that the 'HC7266 has active high and low outputs whereas the 226 has open collector outputs.

Ordering Information

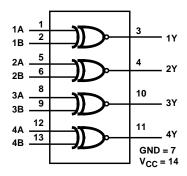
PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC7266F3A	-55 to 125	14 Ld CERDIP
CD74HC7266E	-55 to 125	14 Ld PDIP
CD74HC7266M	-55 to 125	14 Ld SOIC
CD74HC7266MT	-55 to 125	14 Ld SOIC
CD74HC7266M96	-55 to 125	14 Ld SOIC

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

Pinout



Functional Diagram

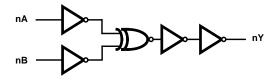


TRUTH TABLE

INP	INPUTS						
nA	nA nB						
L	L	Н					
L	Н	L					
Н	L	L					
Н	Н	Н					

H = High Voltage Level, L = Low Voltage Level

Logic Symbol



CD54HC7266, CD74HC7266

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} -0.5V to 7V DC Input Diode Current, I_{IK} DC Output Diode Current, I_{OK} DC Output Source or Sink Current per Output Pin, IO

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (oC/W)
E (PDIP) Package	80
M (SOIC) Package	86
Maximum Junction Temperature	
Maximum Storage Temperature Range	65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300 ⁰ C
(SOIC - Lead Tips Only)	

Operating Conditions

Temperature Range (T _A)
Supply Voltage Range, V _{CC}
HC Types2V to 6V
HCT Types
DC Input or Output Voltage, V _I , V _O 0V to V _{CC}
Input Rise and Fall Time
2V
4.5V 500ns (Max)
6V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

		TES CONDI		v _{cc}		25°C		-40°C T	O 85°C	-55°C T	O 125°C															
PARAMETER	SYMBOL	V _I (V)	I _O (mA)	(S)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS														
HC TYPES																										
High Level Input	V _{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V														
Voltage				4.5	3.15	-	-	3.15	-	3.15	-	V														
				6	4.2	-	-	4.2	-	4.2	-	V														
Low Level Input	V _{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V														
Voltage				4.5	-	-	1.35	-	1.35	-	1.35	V														
				6	-	-	1.8	-	1.8	-	1.8	V														
High Level Output	V _{OH}	V _{IH} or V _{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V														
Voltage CMOS Loads																	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
																		-0.02	6	5.9	-	-	5.9	-	5.9	-
High Level Output	1		-4	4.5	3.98	-	-	3.84	-	3.7	-	V														
Voltage TTL Loads			-5.2	6	5.48	-	-	5.34	-	5.2	-	V														
Low Level Output	V _{OL}	V _{IH} or V _{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V														
Voltage CMOS Loads			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V														
			0.02	6	-	-	0.1	-	0.1	-	0.1	V														
Low Level Output	1		4	4.5	-	-	0.26	-	0.33	-	0.4	V														
Voltage TTL Loads			5.2	6	-	-	0.26	-	0.33	-	0.4	V														

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DC Electrical Specifications (Continued)

		TEST CONDITIONS		-		v _{cc}		25°C	25°C		-40°C TO 85°C		-55°C TO 125°C	
PARAMETER	SYMBOL	V _I (V)	I _O (mA)	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS		
Input Leakage Current	II	V _{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	μА		
Quiescent Device Current	lcc	V _{CC} or GND	0	6	-	-	2	-	20	-	40	μА		

Switching Specifications Input t_p , $t_f = 6ns$

		TEST		25	°C	-40°C TO 85°C	-55°C TO 125°C	
PARAMETER	SYMBOL	CONDITIONS	V _{CC} (V)	TYP	MAX	MAX	MAX	UNITS
HC TYPES								
Propagation Delay	t _{PLH} , t _{PHL}	C _L = 50pF	2	ı	115	145	150	ns
			4.5	-	23	29	35	ns
			6	-	30	25	30	ns
Propagation Delay Time, Any Input	t _{PLH} , t _{PHL}	C _L = 15pF	5	9	-	-	-	ns
Output Transition Times	t _{TLH} , t _{THL}	C _L = 50pF	2	-	75	95	110	ns
(Figure 1)			4.5	-	15	19	22	ns
			6	-	13	16	19	ns
Input Capacitance	C _{IN}	-	-	-	10	10	10	pF
Power Dissipation Capacitance	C _{PD} (Note 2)	C _L = 15pF	5	33	-	-	-	pF

NOTE:

Test Circuit and Waveform

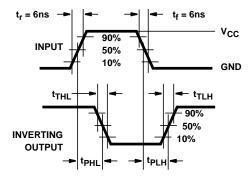


FIGURE 1. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

^{2.} C_{PD} is used to determine the dynamic power consumption per gate, $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.





5-Sep-2011

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
8404302CA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Call TI	
CD54HC7266F3A	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
CD74HC7266E	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HC7266EE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HC7266M	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC7266M96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC7266M96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC7266M96G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC7266ME4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC7266MG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC7266MT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC7266MTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC7266MTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



PACKAGE OPTION ADDENDUM

5-Sep-2011

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF CD54HC7266, CD74HC7266:

Military: CD54HC7266

NOTE: Qualified Version Definitions:

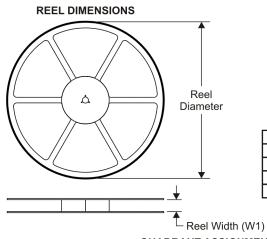
Catalog - TI's standard catalog product

Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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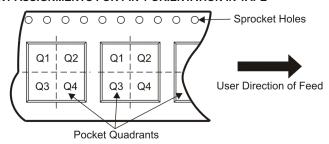
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

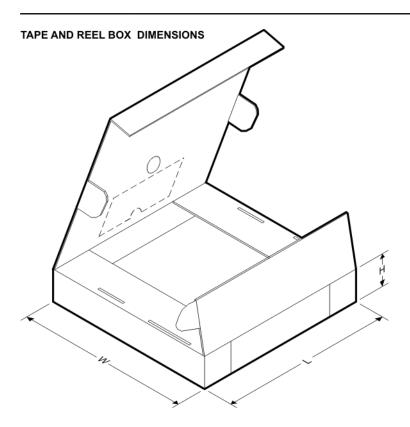
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC7266M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HC7266MT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC7266M96	SOIC	D	14	2500	346.0	346.0	33.0
CD74HC7266MT	SOIC	D	14	250	346.0	346.0	33.0

14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

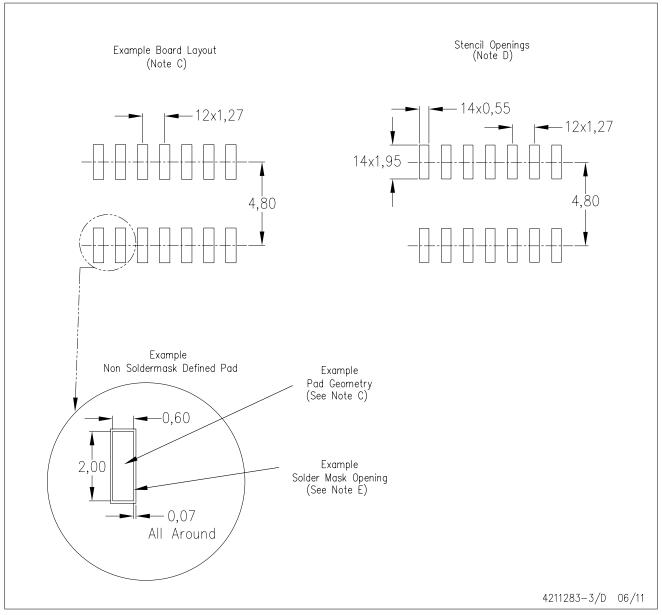


- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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