

Typical V_{OLP} (Output Ground Bounce) <0.8 V

Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at

Max t_{pd} of 4.6 ns at 3.3 V

at V_{CC} = 3.3 V, T_A = 25°C

 $V_{CC} = 3.3 V, T_A = 25^{\circ}C$

FEATURES

- Controlled Baseline
 - One Assembly/Test Site, One Fabrication Site
- Extended Temperature Performance of -40°C to 125°C and -55°C to 125°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree (1)
- Operates From 2 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- (1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

DESCRIPTION/ORDERING INFORMATION

The SN74LVC86A quadruple 2-input exclusive-OR gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The device performs the Boolean function $Y = A \oplus B$ or $Y = \overline{AB} + A\overline{B}$ in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

ORDERING INFORMATION⁽¹⁾

| T _A | PACK | AGE ⁽²⁾ | ORDERABLE PART NUMBER | TOP-SIDE MARKING | | |
|----------------|-----------------------|--------------------|-----------------------|------------------|--|--|
| -40°C to 125°C | SOIC – D | Reel of 2500 | SN74LVC86AQDREP | LVC86AE | | |
| -40 C 10 125 C | TSSOP – PW | Reel of 2000 | SN74LVC86AQPWREP | LVC86AE | | |
| –55°C to 125°C | SOIC – D Reel of 2500 | | SN74LVC86AMDREP | LVC86AM | | |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

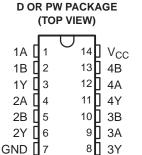
FUNCTION TABLE

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

| (EACH GATE) | | | | | | | | |
|-------------|-----|--------|--|--|--|--|--|--|
| INP | UTS | OUTPUT | | | | | | |
| Α | В | Y | | | | | | |
| L | L | L | | | | | | |
| L | Н | Н | | | | | | |
| н | L | Н | | | | | | |
| Н | Н | L | | | | | | |



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

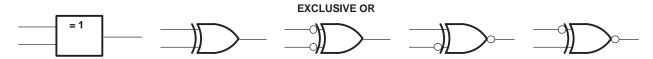


SN74LVC86A-EP QUADRUPLE 2-INPUT EXCLUSIVE-OR GATE

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EXCLUSIVE-OR LOGIC

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



These five equivalent exclusive-OR symbols are valid for an SN74LVC86A gate in positive logic; negation may be shown at any two ports.

LOGIC-IDENTITY ELEMENT

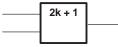
The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

EVEN-PARITY ELEMENT

2k

The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|------------------|--|----------------------|------|-----------------------|------|
| V _{CC} | Supply voltage range | | -0.5 | 6.5 | V |
| VI | Input voltage range ⁽²⁾ | -0.5 | 6.5 | V | |
| Vo | Output voltage range ⁽²⁾⁽³⁾ | | -0.5 | V _{CC} + 0.5 | V |
| I _{IK} | Input clamp current | V _I < 0 V | | -50 | mA |
| I _{OK} | Output clamp current | V _O < 0 V | | -50 | mA |
| I _O | Continuous output current | | | ±50 | mA |
| | Continuous current through V_{CC} or GND | | | ±100 | mA |
| 0 | Deckare thermal impedance ⁽⁴⁾ | D package | | 86 | °C/W |
| θ_{JA} | Package thermal impedance ⁽⁴⁾ | PW package | | 113 | °C/W |
| T _{stg} | Storage temperature range | | -65 | 150 | °C |

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings (1) only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed. (2)

The value of V_{CC} is provided in the recommended operating conditions table. (3)

The package thermal impedance is calculated in accordance with JESD 51-7. (4)

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Recommended Operating Conditions⁽¹⁾

| | | | MIN | MAX | UNIT |
|-----------------|------------------------------------|----------------------------------|-----|----------|------|
| V | Supply veltage | Operating | 2 | 3.6 | V |
| V _{CC} | Supply voltage | Data retention only | 1.5 | | v |
| V _{IH} | High-level input voltage | V _{CC} = 2.7 V to 3.6 V | 2 | | V |
| V _{IL} | Low-level input voltage | V_{CC} = 2.7 V to 3.6 V | | 0.8 | V |
| VI | Input voltage | | 0 | 5.5 | V |
| Vo | Output voltage | | 0 | V_{CC} | V |
| | Ligh lovel output ourrent | V _{CC} = 2.7 V | | -12 | mA |
| I _{OH} | High-level output current | $V_{CC} = 3 V$ | | -24 | IIIA |
| | | V _{CC} = 2.7 V | | 12 | |
| I _{OL} | Low-level output current | V _{CC} = 3 V | | 24 | mA |
| Δt/Δv | Input transition rise or fall rate | · · · · · | | 9 | ns/V |
| т | | Q suffix | -40 | 125 | °C |
| T _A | Operating free-air temperature | M suffix | -55 | 125 | °C |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{cc} | MIN TYP ⁽¹⁾ | MAX | UNIT |
|------------------|--|-----------------|------------------------|------|------|
| | $I_{OH} = -100 \ \mu A$ | 2.7 V to 3.6 V | $V_{CC} - 0.2$ | | |
| M | 10 | 2.7 V | 2.2 | | V |
| V _{ОН} | $I_{OH} = -12 \text{ mA}$ | 3 V | 2.4 | | v |
| _ | $I_{OH} = -24 \text{ mA}$ | 3 V | 2.2 | | |
| | I _{OL} = 100 μA | 2.7 V to 3.6 V | | 0.2 | |
| V _{OL} | I _{OL} = 12 mA | 2.7 V | | 0.4 | V |
| | $I_{OL} = 24 \text{ mA}$ | 3 V | | 0.55 | |
| l _l | $V_1 = 5.5 \text{ V or GND}$ | 3.6 V | | ±5 | μA |
| I _{CC} | $V_{I} = V_{CC} \text{ or } GND, I_{O} = 0$ | 3.6 V | | 10 | μA |
| ΔI _{CC} | One input at V _{CC} $-$ 0.6 V, Other inputs at V _{CC} or GND | 2.7 V to 3.6 V | | 500 | μA |
| C _i | $V_{I} = V_{CC} \text{ or } GND$ | 3.3 V | 5 | | pF |

(1) All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}C$.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| PARAMETER | PARAMETER FROM (INPUT) | TO (OUTPUT) | V _{CC} = | 2.7 V | V _{CC} = 1 ± 0.3 | UNIT | |
|-----------------|---------------------------|----------------|-------------------|-------|------------------------------|------|----|
| | (INFOT) | (001F01) | MIN | MAX | MIN | MAX | |
| t _{pd} | А | Y | | 5.6 | 1 | 4.6 | ns |

Operating Characteristics

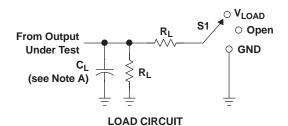
 $T_A = 25^{\circ}C$

| | PARAMETER | TEST | V _{CC} = 2.5 V | V _{CC} = 3.3 V | UNIT |
|-----------------|--|------------|-------------------------|-------------------------|------|
| | | CONDITIONS | TYP | TYP | 0 |
| C _{pd} | Power dissipation capacitance per gate | f = 10 MHz | 7.5 | 8.5 | pF |

SN74LVC86A-EP QUADRUPLE 2-INPUT EXCLUSIVE-OR GATE SCAS752B-DECEMBER 2003-REVISED JULY 2007

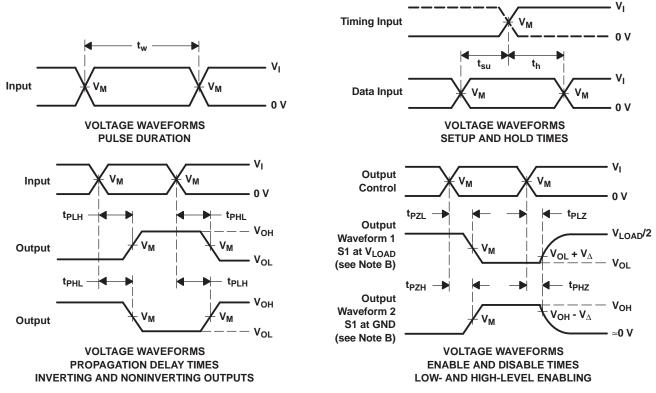


PARAMETER MEASUREMENT INFORMATION



| TEST | S1 |
|------------------------------------|-------------------|
| t _{PLH} /t _{PHL} | Open |
| t _{PLZ} /t _{PZL} | V _{LOAD} |
| t _{PHZ} /t _{PZH} | GND |

| N. | INPUTS | | N | | • | | N |
|-------------------|--------|--------------------------------|-------|-------------------|-------|--------------|--------------|
| V _{CC} | VI | t _r /t _f | VM | V _{LOAD} | CL | RL | V_{Δ} |
| 2.7 V | 2.7 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| 3.3 V \pm 0.3 V | 2.7 V | ≤ 2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. $t_{PLZ} \, \text{and} \, t_{PHZ} \, \text{are the same as} \, t_{dis}.$
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|-----------------|--------------------|------|----------------|----------------------------|------------------|------------------------------|
| SN74LVC86AMDREP | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC86AQDREP | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC86AQPWREP | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| V62/04670-01XE | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| V62/04670-01YE | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| V62/04670-02XE | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74LVC86A-EP :

- Catalog: SN74LVC86A
- Automotive: SN74LVC86A-Q1
- Military: SN54LVC86A

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military QML certified for Military and Defense Applications

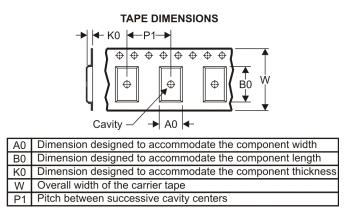
PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



| *All dimensions are nominal | All dimensions are nominal | | | | | | | | | | | |
|-----------------------------|----------------------------|--------------------|----|------|--------------------------|--------------------------|------------|------------|------------|------------|-----------|------------------|
| Device | Package Type | Package Drawing | | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
| SN74LVC86AMDREP | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LVC86AQDREP | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LVC86AQPWREP | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

30-Jul-2010



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC86AMDREP | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74LVC86AQDREP | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74LVC86AQPWREP | TSSOP | PW | 14 | 2000 | 346.0 | 346.0 | 29.0 |

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



A. An integration of the information o

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153



LAND PATTERN DATA



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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