

Data sheet acquired from Harris Semiconductor SCHS125C

# CD54HC02, CD74HC02, CD54HCT02

# High-Speed CMOS Logic Quad Two-Input NOR Gate

March 1998 - Revised September 2003

#### **Features**

- · Buffered Inputs
- Typical Propagation Delay: 7ns at V<sub>CC</sub> = 5V,
   C<sub>L</sub> = 15pF, T<sub>A</sub> = 25°C
- Fanout (Over Temperature Range)
- Wide Operating Temperature Range ...-55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL}$  = 30%,  $N_{IH}$  = 30% of  $V_{CC}$  at  $V_{CC}$  = 5V
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,
     V<sub>IL</sub>= 0.8V (Max), V<sub>IH</sub> = 2V (Min)
  - CMOS Input Compatibility, I<sub>I</sub>  $\leq$  1 $\mu$ A at V<sub>OL</sub>, V<sub>OH</sub>

# Description

The 'HC02 and 'HCT02 logic gates utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The HCT logic family is functionally pin compatible with the standard LS logic family.

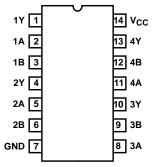
#### **Ordering Information**

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC02F3A	-55 to 125	14 Ld CERDIP
CD54HCT02F3A	-55 to 125	14 Ld CERDIP
CD74HC02E	-55 to 125	14 Ld PDIP
CD74HC02M	-55 to 125	14 Ld SOIC
CD74HC02MT	-55 to 125	14 Ld SOIC
CD74HC02M96	-55 to 125	14 Ld SOIC
CD74HCT02E	-55 to 125	14 Ld PDIP
CD74HCT02M	-55 to 125	14 Ld SOIC
CD74HCT02MT	-55 to 125	14 Ld SOIC
CD74HCT02M96	-55 to 125	14 Ld SOIC

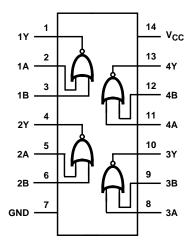
NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

# **Pinout**





# Functional Diagram

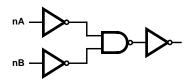


**TRUTH TABLE** 

INP	OUTPUT		
nA	nB	nY	
L	L	Н	
L	Н	L	
Н	L	L	
Н	Н	L	

H = High Voltage Level, L = Low Voltage Level

# Logic Diagram



#### CD54HC02, CD74HC02, CD54HCT02, CD74HCT02

# **Absolute Maximum Ratings**

# DC Supply Voltage, V $_{CC}$ ...-0.5V to 7V DC Input Diode Current, I $_{IK}$ For V $_{I}$ < -0.5V or V $_{I}$ > V $_{CC}$ + 0.5V ...±20mA DC Output Diode Current, I $_{OK}$ For V $_{O}$ < -0.5V or V $_{O}$ > V $_{CC}$ + 0.5V ...±20mA DC Output Source or Sink Current per Output Pin, I $_{O}$ For V $_{O}$ > -0.5V or V $_{O}$ < V $_{CC}$ + 0.5V ...±25mA DC V $_{CC}$ or Ground Current, I $_{CC}$ or I $_{GND}$ ...±50mA

#### **Thermal Information**

Thermal Resistance (Typical, Note 1)	$\theta_{JA}$ (°C/W)
E (PDIP) Package	80
M (SOIC) Package	86
Maximum Junction Temperature (Hermetic Package or Di	
Maximum Junction Temperature (Plastic Package)	150°C
Maximum Storage Temperature Range65	<sup>o</sup> C to 150 <sup>o</sup> C
Maximum Lead Temperature (Soldering 10s)	300°C
(SOIC - Lead Tips Only)	

#### **Operating Conditions**

Temperature Range (T <sub>A</sub> )55°C to 125°C
Supply Voltage Range, V <sub>CC</sub>
HC Types2V to 6V
HCT Types
DC Input or Output Voltage, V <sub>I</sub> , V <sub>O</sub> 0V to V <sub>CC</sub>
Input Rise and Fall Time
2V
4.5V 500ns (Max)
6V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

#### NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

#### **DC Electrical Specifications**

		TE: CONDI		v <sub>cc</sub>		25°C		-40°C 1	O 85°C	-55°C TO 125°C		
PARAMETER	SYMBOL	V <sub>I</sub> (V)	I <sub>O</sub> (mA)	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES												
High Level Input	V <sub>IH</sub>	-	-	2	1.5	-	-	1.5	-	1.5	-	V
Voltage				4.5	3.15	•	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input	V <sub>IL</sub>	-	-	2	-	-	0.5	-	0.5	-	0.5	V
Voltage				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output	VoH	V <sub>IH</sub> or V <sub>IL</sub>	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
Voltage CMOS Loads			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output			-	-	-	-	-	-	-	-	-	V
Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
TTE LOAGS			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	2	-	-	0.1	-	0.1	-	0.1	V
Voltage CMOS Loads			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
CIVIOS LOAGS			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output	7		-	-	-	-	-	-	-	-	-	V
Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
I I L LUaus			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	lı	V <sub>CC</sub> or GND	-	6	-	-	±0.1	-	±1	-	±1	μА
Quiescent Device Current	Icc	V <sub>CC</sub> or GND	0	6	-	-	2	-	20	-	40	μА

# CD54HC02, CD74HC02, CD54HCT02, CD74HCT02

# DC Electrical Specifications (Continued)

		TES CONDI		V <sub>CC</sub>		25°C		-40°C 1	O 85°C	-55°C T	O 125°C	
PARAMETER	SYMBOL	V <sub>I</sub> (V)	I <sub>O</sub> (mA)	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HCT TYPES												
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	Voн	V <sub>IH</sub> or V <sub>IL</sub>	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	lį	V <sub>CC</sub> and GND	0	5.5	-		±0.1	-	±1	-	±1	μΑ
Quiescent Device Current	Icc	V <sub>CC</sub> or GND	0	5.5	-	-	2	-	20	-	40	μΑ
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI <sub>CC</sub> (Note 2)	V <sub>CC</sub> -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μΑ

#### NOTE:

### **HCT Input Loading Table**

INPUT	UNIT LOADS
All	1.5

NOTE: Unit Load is  $\Delta I_{CC}$  limit specified in DC Electrical Table, e.g.,  $360\mu\text{A}$  max at  $25^{\text{O}}\text{C}.$ 

# Switching Specifications Input $t_{r}$ , $t_{f} = 6$ ns

		TEST	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES											
Propagation Delay, Input to Output (Figure 1)	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	90	-	115	-	135	ns
			4.5	-	-	18	-	23	-	27	ns
			6	-	-	15	-	20	-	23	ns
Propagation Delay, Data Input to Output Y	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 15pF	5	-	7	-	-	-	-	-	ns
Transition Times (Figure 1)	t <sub>TLH</sub> , t <sub>THL</sub>	C <sub>L</sub> = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C <sub>IN</sub>	-	-	-	-	10	-	10	-	10	pF

<sup>2.</sup> For dual-supply systems theoretical worst case ( $V_I$  = 2.4V,  $V_{CC}$  = 5.5V) specification is 1.8mA.

# CD54HC02, CD74HC02, CD54HCT, CD74HCT02

#### Switching Specifications Input $t_r$ , $t_f = 6ns$ (Continued)

		TEST	TEST		25°C			-40°C TO 85°C		-55°C TO 125°C		
PARAMETER	SYMBOL	CONDITIONS	V <sub>CC</sub> (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS	
Power Dissipation Capacitance (Notes 3, 4)	C <sub>PD</sub>	-	5	-	26	-	-	-	-	-	pF	
HCT TYPES	HCT TYPES											
Propagation Delay, Input to Output (Figure 2)	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	4.5	-	-	21	-	26	-	32	ns	
Propagation Delay, Data Input to Output Y	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 15pF	5	-	8	-	-	-	-	-	ns	
Transition Times (Figure 2)	t <sub>TLH</sub> , t <sub>THL</sub>	C <sub>L</sub> = 50pF	4.5	-	-	15	-	19	-	22	ns	
Input Capacitance	C <sub>IN</sub>	-	-	-	-	10	-	10	-	10	pF	
Power Dissipation Capacitance (Notes 3, 4)	C <sub>PD</sub>	-	5	=	26	-	-	-	-	-	pF	

#### NOTES:

- 3. C<sub>PD</sub> is used to determine the dynamic power consumption, per gate.
- 4.  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = input frequency,  $C_L$  = output load capacitance,  $V_{CC}$  = supply voltage.

#### Test Circuits and Waveforms

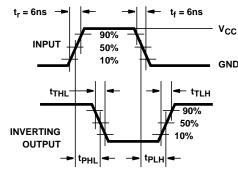


FIGURE 1. HC AND HCU TRANSITION TIMES AND PROPAGA-TION DELAY TIMES, COMBINATION LOGIC

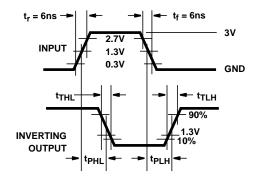


FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

5-Sep-2011

#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
5962-8975101CA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Call TI	
CD54HC02F	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
CD54HC02F3A	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
CD54HCT02F	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
CD54HCT02F3A	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
CD74HC02E	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HC02EE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HC02M	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC02M96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC02M96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC02M96G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC02ME4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC02MG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC02MT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC02MTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC02MTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT02E	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HCT02EE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HCT02M	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT02M96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT02M96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	





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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
CD74HCT02M96G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT02ME4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT02MG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT02MT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT02MTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT02MTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### OTHER QUALIFIED VERSIONS OF CD54HC02, CD54HCT02, CD74HC02, CD74HCT02:

◆ Catalog: CD74HC02, CD74HCT02

• Military: CD54HC02, CD54HCT02

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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# TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC02M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HC02MT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HCT02M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HCT02MT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

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\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC02M96	SOIC	D	14	2500	346.0	346.0	33.0
CD74HC02MT	SOIC	D	14	250	346.0	346.0	33.0
CD74HCT02M96	SOIC	D	14	2500	346.0	346.0	33.0
CD74HCT02MT	SOIC	D	14	250	346.0	346.0	33.0

# 14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

# N (R-PDIP-T\*\*)

# PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



# D (R-PDSO-G14)

# PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



# D (R-PDSO-G14)

# PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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