

## CONFIGURABLE MULTIPLE-FUNCTION GATE

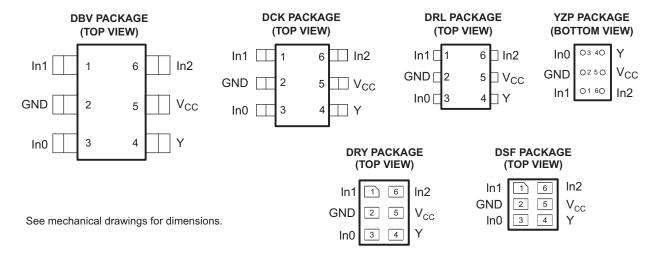
Check for Samples: SN74LVC1G57

#### **FEATURES**

- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V V<sub>CC</sub> Operation
- Inputs Accept Voltages to 5.5 V
- Max t<sub>pd</sub> of 6.3 ns at 3.3 V
- Low Power Consumption, 10-µA Max I<sub>CC</sub>
- ±24-mA Output Drive at 3.3 V
- I<sub>off</sub> Supports Partial-Power-Down Mode

#### Operation

- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)



#### **DESCRIPTION/ORDERING INFORMATION**

This configurable multiple-function gate is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation.

The SN74LVC1G57 features configurable multiple functions. The output state is determined by eight patterns of 3-bit input. The user can choose the logic functions AND, OR, NAND, NOR, XNOR, inverter, and noninverter. All inputs can be connected to  $V_{CC}$  or GND.

This device functions as an independent gate, but because of Schmitt action, it may have different input threshold levels for positive-going  $(V_{T_{+}})$  and negative-going  $(V_{T_{-}})$  signals.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



#### **ORDERING INFORMATION**

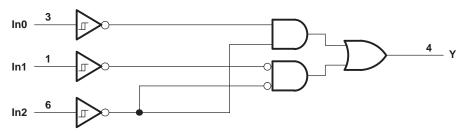
T <sub>A</sub>	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>(2)</sup>
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74LVC1G57YZPR	CL_
	SOT (SOT-23) – DBV	Reel of 3000	SN74LVC1G57DBVR	CA7_
–40°C to 85°C	SOT (SC-70) – DCK	Reel of 3000	SN74LVC1G57DCKR	CL_
	SOT (SOT-563) – DRL	Reel of 4000	SN74LVC1G57DRLR	CL_
	QFN – DRY <sup>(3)</sup>	Reel of 5000	SN74LVC1G57DRYR	CL
	μQFN – DSF <sup>(3)</sup>	Reel of 5000	SN74LVC1G57DSFR	CL

- Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
- DBV/DCK/DRL: The actual top-side marking has one additional character that designates the assembly/test site. YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free). ESD protection exceeds 150-V machine model.

**Table 1. FUNCTION TABLE** 

	INPUTS	OUTPUT	
ln2	ln1	In0	Y
L	L	L	Н
L	L	Н	L
L	Н	L	Н
L	Н	Н	L
Н	L	L	L
Н	L	Н	L
Н	Н	L	Н
Н	Н	Н	Н

Figure 1. LOGIC DIAGRAM (POSITIVE LOGIC)



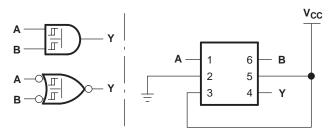
**Table 2. FUNCTION SELECTION TABLE** 

LOGIC FUNCTION	FIGURE NO.
2-input AND	1
2-input AND with both inputs inverted	4
2-input NAND with inverted input	2, 3
2-input OR with inverted input	2, 3
2-input NOR	4
2-input NOR with both inputs inverted	1
2-input XNOR	5

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### LOGIC CONFIGURATIONS



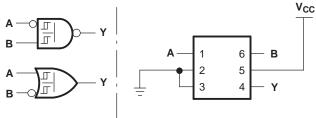
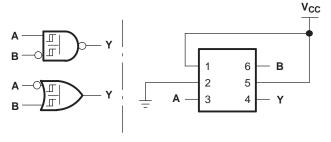


Figure 2. 2-Input AND Gate

Figure 3. 2-Input NAND Gate With Inverted A Input



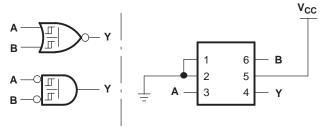


Figure 4. 2-Input NAND Gate With Inverted B Input

Figure 5. 2-Input NOR Gate

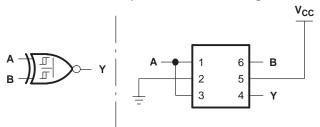


Figure 6. 2-Input XNOR Gate



## Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage range		-0.5	6.5	V
VI	Input voltage range (2)		-0.5	6.5	V
Vo	Voltage range applied to any output in the high-im	npedance or power-off state <sup>(2)</sup>	-0.5	6.5	V
Vo	Voltage range applied to any output in the high or	low state <sup>(2) (3)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		<b>–</b> 50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		<b>–</b> 50	mA
Io	Continuous output current			±50	mA
	Continuous current through V <sub>CC</sub> or GND			±100	mA
		DBV package		165	
^	David and the control in the day (4)	DCK package		259	9000
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DRL package		142	°C/W
		YZP package		123	
T <sub>stg</sub>	Storage temperature range		-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## Recommended Operating Conditions<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Complexed to an	Operating	1.65	5.5	
	Supply voltage	Supply voltage Data retention only			V
VI	Input voltage	·	0	5.5	V
Vo	Output voltage		0	V <sub>CC</sub>	V
V <sub>I</sub>		V <sub>CC</sub> = 1.65 V		-4	
		V <sub>CC</sub> = 2.3 V		-8	
	High-level output current	V 0.V		-16	mA
		V <sub>CC</sub> = 3 V		-24	
		Data retention only  V <sub>CC</sub> = 1.65 V		-32	
		V <sub>CC</sub> = 1.65 V		4	
		V <sub>CC</sub> = 2.3 V		8	
$I_{OL}$	Low-level output current	V 2V		16	
		V <sub>CC</sub> = 3 V		24	
		V <sub>CC</sub> = 4.5 V		32	
T <sub>A</sub>	Operating free-air temperature		-40	85	°C

<sup>(1)</sup> All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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<sup>(2)</sup> The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>(3)</sup> The value of V<sub>CC</sub> is provided in the recommended operating conditions table.

<sup>(4)</sup> The package thermal impedance is calculated in accordance with JESD 51-7.



## **Electrical Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>cc</sub>	MIN TYP <sup>(1)</sup>	MAX	UNI		
		1.65 V	0.79	1.16			
$V_{T+}$		2.3 V	1.11	1.56			
Positive-going input		3 V	1.5	1.87	V		
threshold voltage		4.5 V	2.16	2.74			
		5.5 V	2.61	3.33			
		1.65 V	0.35	0.62			
$V_{T-}$		2.3 V	0.58	0.87			
Negative-going input		3 V	0.84	1.19	V		
threshold voltage		4.5 V	1.41	1.9			
		5.5 V	1.87	2.29			
		1.65 V	0.3	0.62			
		2.3 V	0.4	0.8			
$\Delta V_T$ Hysteresis ( $V_{T+} - V_{T-}$ )		3 V	0.53	0.87	V		
11y3(e1e3i3 (V  + - V  _)		4.5 V	0.71	1.04			
		5.5 V	0.71	1.11	İ		
	I <sub>OH</sub> = -100 μA	1.65 V to 5.5 V	V <sub>CC</sub> - 0.1				
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2				
.,	$I_{OH} = -8 \text{ mA}$	2.3 V	1.9				
$V_{OH}$	I <sub>OH</sub> = -16 mA	2.1/	2.4		V		
	I <sub>OH</sub> = -24 mA	3 V	2.3				
	I <sub>OH</sub> = -32 mA	4.5 V	3.8				
	I <sub>OL</sub> = 100 μA	1.65 V to 5.5 V		0.1			
	I <sub>OL</sub> = 4 mA	1.65 V		0.45			
	I <sub>OL</sub> = 8 mA	2.3 V		0.3			
$V_{OL}$	I <sub>OL</sub> = 16 mA	2.1/		0.4	V		
	I <sub>OL</sub> = 24 mA	3 V		0.55			
	I <sub>OL</sub> = 32 mA	4.5 V		0.55			
l <sub>l</sub>	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V		±1	μA		
l <sub>off</sub>	$V_I$ or $V_O = 5.5 \text{ V}$	0		±10	μΑ		
I <sub>CC</sub>	$V_1 = 5.5 \text{ V or GND, } I_0 = 0$	1.65 V to 5.5 V		10	μΑ		
ΔI <sub>CC</sub>	One input at $V_{CC} - 0.6 V$ , Other inputs at $V_{CC}$ or GND	3 V to 5.5 V		500	μA		
C <sub>i</sub>	$V_I = V_{CC}$ or GND	3.3 V	3.5		рF		

<sup>(1)</sup> All typical values are at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C.



## **Switching Characteristics**

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = ± 0.7			2.5 V .2 V		3.3 V .3 V	V <sub>CC</sub> : ± 0.		UNIT
	(INFOT)	(001F01)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	Any In	Υ	3.2	14.4	2	8.3	1.5	6.3	1.1	5.1	ns

## **Operating Characteristics**

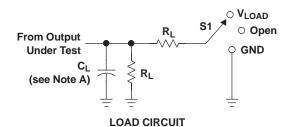
 $T_A = 25^{\circ}C$ 

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V TYP	V <sub>CC</sub> = 2.5 V TYP	V <sub>CC</sub> = 3.3 V TYP	V <sub>CC</sub> = 5 V TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz	20	20	21	22	pF

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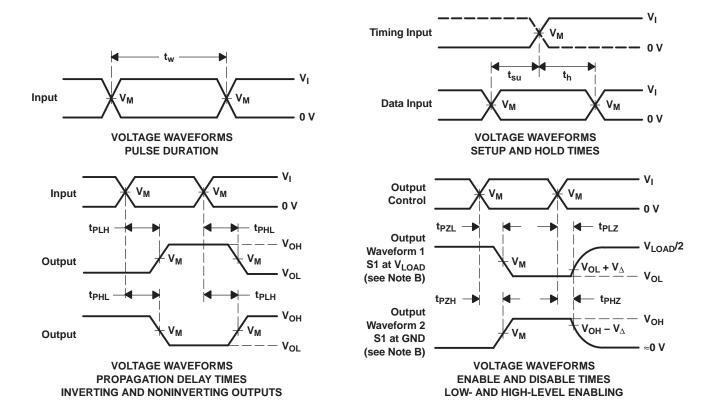


#### PARAMETER MEASUREMENT INFORMATION



TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	V <sub>LOAD</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

.,	INPUTS		.,	V	0		.,
V <sub>CC</sub>	VI	t <sub>r</sub> /t <sub>f</sub>	V <sub>M</sub>	V <sub>LOAD</sub>	C <sub>L</sub> R <sub>L</sub>		$V_{\Delta}$
1.8 V ± 0.15 V	V <sub>CC</sub>	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	$V_{CC}$	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	500 Ω	0.15 V
3.3 V $\pm$ 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V <sub>CC</sub>	≤2.5 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	50 pF	500 Ω	0.3 V



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
- F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
- G. t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>.
- H. All parameters and waveforms are not applicable to all devices.

Figure 7. Load Circuit and Voltage Waveforms

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### SCES414M - NOVEMBER 2002 - REVISED OCTOBER 2011



## **REVISION HISTORY**

Cł	hanges from Revision L (January 2007) to Revision M	Page
•	Added DRY and DSF packages to datasheet.	1
•	Added additional package options to the ORDERING INFORMATION table.	2



3-Mar-2012

#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN74LVC1G57DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G57DBVRE4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G57DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G57DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G57DCKRE4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G57DCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G57DRLR	ACTIVE	SOT	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G57DRLRG4	ACTIVE	SOT	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G57DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G57DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G57YZPR	ACTIVE	DSBGA	YZP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



### PACKAGE OPTION ADDENDUM

3-Mar-2012

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

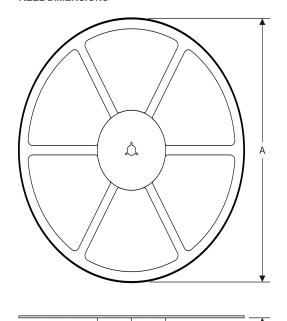
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

# PACKAGE MATERIALS INFORMATION

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## TAPE AND REEL INFORMATION

#### **REEL DIMENSIONS**



#### **TAPE DIMENSIONS**



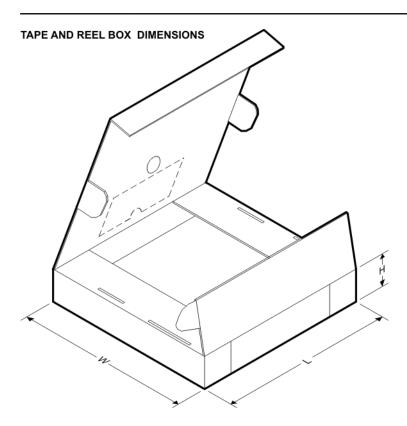
A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### TAPE AND REEL INFORMATION

\*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G57DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G57DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G57DCKR	SC70	DCK	6	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1G57DRLR	SOT	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1G57DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G57DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G57YZPR	DSBGA	YZP	6	3000	180.0	8.4	1.02	1.52	0.63	4.0	8.0	Q1

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\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G57DBVR	SOT-23	DBV	6	3000	203.0	203.0	35.0
SN74LVC1G57DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1G57DCKR	SC70	DCK	6	3000	205.0	200.0	33.0
SN74LVC1G57DRLR	SOT	DRL	6	4000	202.0	201.0	28.0
SN74LVC1G57DRYR	SON	DRY	6	5000	180.0	180.0	30.0
SN74LVC1G57DSFR	SON	DSF	6	5000	180.0	180.0	30.0
SN74LVC1G57YZPR	DSBGA	YZP	6	3000	220.0	220.0	34.0

# DBV (R-PDSO-G6)

# PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- Falls within JEDEC MO-178 Variation AB, except minimum lead width.



# DBV (R-PDSO-G6)

# PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



# DCK (R-PDSO-G6)

# PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AB.



# DCK (R-PDSO-G6)

# PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



# DRL (R-PDSO-N6)

# PLASTIC SMALL OUTLINE



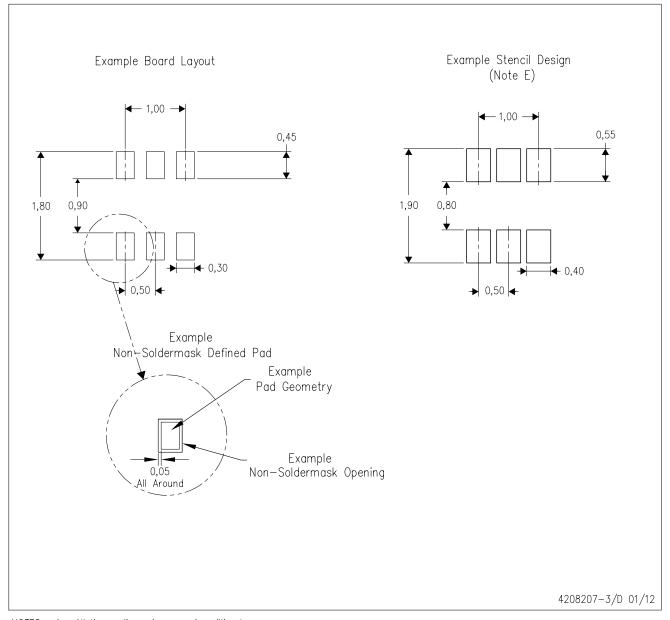
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs.

  Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
- D. JEDEC package registration is pending.



# DRL (R-PDSO-N6)

#### PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Side aperture dimensions over—print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.





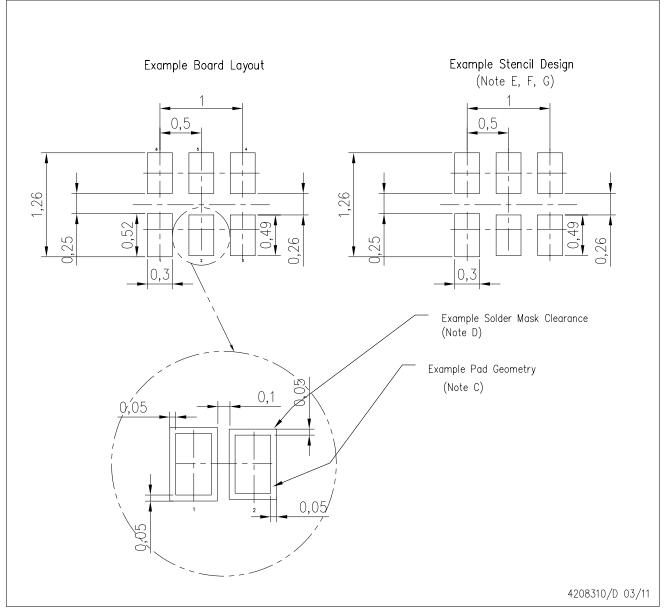
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. SON (Small Outline No-Lead) package configuration.
- The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
- E. This package complies to JEDEC MO-287 variation UFAD.
- $frac{f}{K}$  See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.



# DRY (S-PUSON-N6)

### PLASTIC SMALL OUTLINE NO-LEAD



- NOTES: A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
  - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
  - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.





NOTES: All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.

- B. This drawing is subject to change without notice.
  C. SON (Small Outline No-Lead) package configuration.
  D. This package complies to JEDEC MO-287 variation X2AAF.





# PLASTIC SMALL OUTLINE NO-LEAD

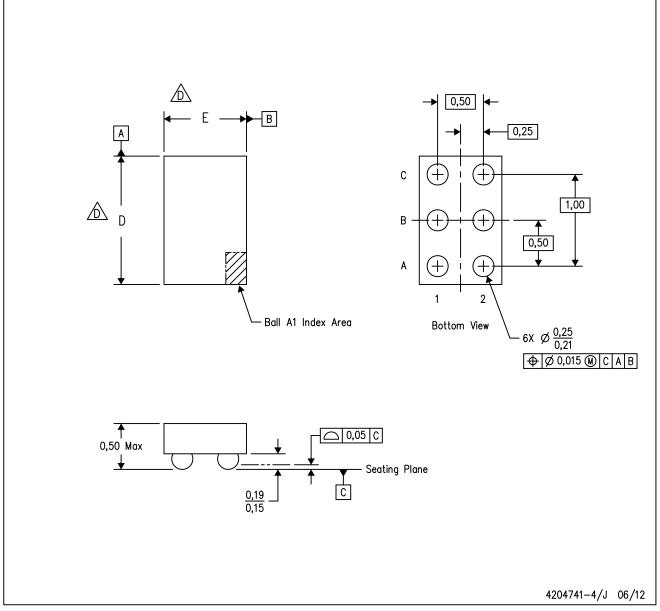


- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
- E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
- H. Component placement force should be minimized to prevent excessive paste block deformation.



YZP (R-XBGA-N6)

DIE-SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.
- The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
- E. This package is a Pb-free solder ball design. Refer to the 6 YEP package (drawing 4204725) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.



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