

54ACT11030, 74ACT11030 8-INPUT POSITIVE-NAND GATES

SCLS050 – MARCH 1987 – REVISED APRIL 1993

- Inputs Are TTL-Voltage Compatible
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

These devices contain a single 8-input NAND gate and perform the following Boolean functions in positive logic:

$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H} \text{ or}$$

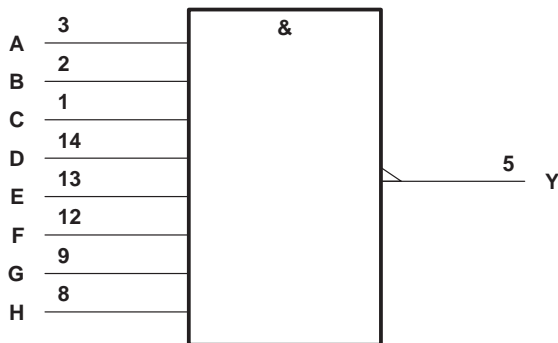
$$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$$

The 54ACT11030 is characterized for operation over the full military temperature range of -55°C to 125°C . The 74ACT11030 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

| INPUTS A THRU H | OUTPUT Y |
|----------------------|-------------|
| All inputs H | L |
| One or more inputs L | H |

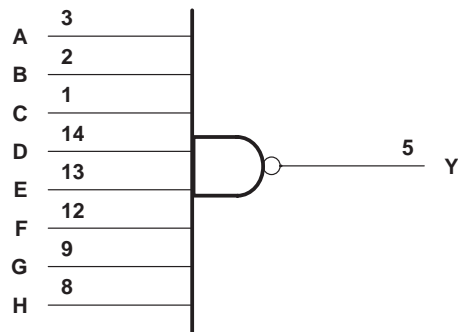
logic symbol†



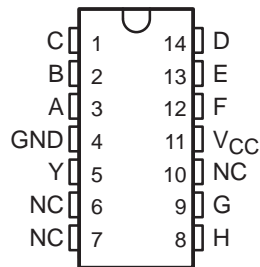
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the D, J, and N packages.

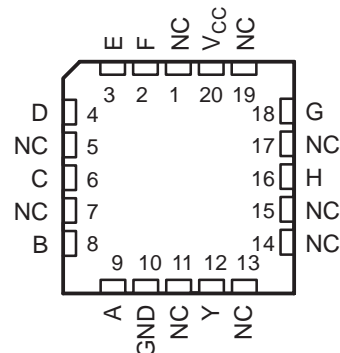
logic diagram (positive logic)



54ACT11030 ... J PACKAGE
74ACT11030 ... D OR N PACKAGE
(TOP VIEW)



54ACT11030 ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

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SCLS050 – MARCH 1987 – REVISED APRIL 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------------------|
| Supply voltage range, V_{CC} | -0.5 V to 6 V |
| Input voltage range, V_I (see Note 1) | -0.5 V to $V_{CC} + 0.5$ V |
| Output voltage range, V_O (see Note 1) | -0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) | ± 20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) | ± 50 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ± 50 mA |
| Continuous current through V_{CC} or GND | ± 100 mA |
| Storage temperature range | -65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

| | 54ACT11030 | | 74ACT11030 | | UNIT |
|--|------------|----------|------------|----------|------|
| | MIN | MAX | MIN | MAX | |
| V_{CC} Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| V_{IH} High-level input voltage | 2 | | 2 | | V |
| V_{IL} Low-level input voltage | | 0.8 | | 0.8 | V |
| V_I Input voltage | 0 | V_{CC} | 0 | V_{CC} | V |
| V_O Output voltage | 0 | V_{CC} | 0 | V_{CC} | V |
| I_{OH} High-level output current | | -24 | | -24 | mA |
| I_{OL} Low-level output current | | 24 | | 24 | mA |
| $\Delta t/\Delta v$ Input transition rise or fall rate | 0 | 10 | 0 | 10 | ns/V |
| T_A Operating free-air temperature | -55 | 125 | -40 | 85 | °C |

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SCLS050 – MARCH 1987 – REVISED APRIL 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | 54ACT11030 | | 74ACT11030 | | UNIT |
|---------------------------------------|---|-----------------|-----------------------|-----|------|------------|------|------------|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | I _{OH} = -50 μA | 4.5 V | 4.4 | | | 4.4 | | 4.4 | V | |
| | | 5.5 V | 5.4 | | | 5.4 | | 5.4 | | |
| | I _{OH} = -24 mA | 4.5 V | 3.94 | | | 3.7 | | 3.8 | | |
| | | 5.5 V | 4.94 | | | 4.7 | | 4.8 | | |
| | I _{OH} = -50 mA [†] | 5.5 V | | | | 3.85 | | | | |
| I _{OH} = -75 mA [†] | 5.5 V | | | | | | 3.85 | | | |
| V _{OL} | I _{OL} = 50 μA | 4.5 V | | | | 0.1 | | 0.1 | V | |
| | | 5.5 V | | | | 0.1 | | 0.1 | | |
| | I _{OL} = 24 mA | 4.5 V | | | | 0.36 | | 0.44 | | |
| | | 5.5 V | | | | 0.36 | | 0.44 | | |
| | I _{OL} = 50 mA [†] | 5.5 V | | | | | 1.65 | | | |
| I _{OL} = 75 mA [†] | 5.5 V | | | | | | 1.65 | | | |
| I _I | V _I = V _{CC} or GND | 5.5 V | | | ±0.1 | | ±1 | ±1 | μA | |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 5.5 V | | | 4 | | 80 | 40 | μA | |
| ΔI _{CC} [‡] | One input at 3.4 V, Other inputs at V _{CC} or GND | 5.5 V | | | 0.9 | | 1 | 1 | mA | |
| C _i | V _I = V _{CC} or GND | 5 V | | 3.5 | | | | | pF | |

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | T _A = 25°C | | | 54ACT11030 | | 74ACT11030 | | UNIT |
|------------------|--------------|-------------|-----------------------|-----|-----|------------|-----|------------|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t _{PLH} | A thru H | Y | 1.5 | 5.4 | 8.1 | 1.5 | 8.8 | 1.5 | 8.5 | ns |
| t _{PHL} | | | 1.5 | 5.9 | 7.8 | 1.5 | 9.3 | 1.5 | 8.7 | |

operating characteristics, V_{CC} = 5 V, T_A = 25°C

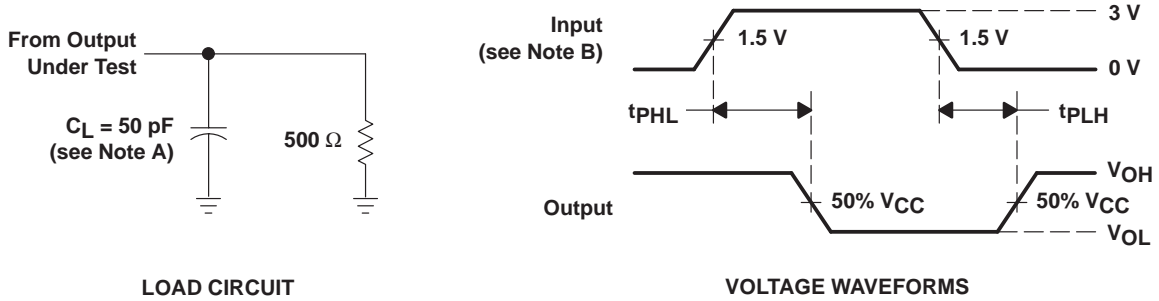
| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|--|-----------------------------------|-----|------|
| C _{pd} Power dissipation capacitance per gate | C _L = 50 pF, f = 1 MHz | 41 | pF |



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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| 74ACT11030DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| 74ACT11030DR | SOIC | D | 14 | 2500 | 346.0 | 346.0 | 33.0 |

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