- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication
- **Extended Temperature Performance of** -55°C to 125°C
- **Enhanced Diminishing Manufacturing** Sources (DMS) Support
- **Enhanced Product Change Notification**
- Qualification Pedigree[†]
- **EPIC™** (Enhanced-Performance Implanted **CMOS) Process**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life.

Operating Range 2-V to 5.5-V V_{CC}

2Y | 6

GND []

ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)

D OR PW PACKAGE (TOP VIEW) 1А Г 14 🛮 V_{CC} 1B **∏** 2 13**∏** 4B 1Y 🛮 3 12 4A 2A 🛮 4 11 4Y 10**∏** 3B 2B 🛮 5

9 | 3A

8 3Y

description

The SN74AHC00 performs the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

ORDERING INFORMATION

TA	PACK	AGE [‡]	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOIC - D	Tape and reel	SN74AHC00MDREP	AHC00MEP
-55 0 10 125 0	TSSOP – PW	Tape and reel	SN74AHC00MPWREP	HA00MEP

[‡] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each gate)

INP	UTS	OUTPUT
Α	В	Υ
Н	Н	L
L	X	Н
Х	L	Н

logic diagram, each gate (positive logic)





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC}	0.5 V to 7 V
Input voltage range, V _I (see Note 1)	–0.5 V to 7 V
Output voltage range, VO (see Note 1)	0.5 V to V _{CC} + 0.5 V
Input clamp current, $I_{ K }(V_{ C } < 0)$	–20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V _{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	86°C/W
PW package	113°C/W
Storage temperature range, T _{stq}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT	
VCC	Supply voltage		2	5.5	V	
	V _{CC} = 2 V		1.5			
V_{IH}	High-level input voltage	V _{CC} = 3 V	2.1		V	
		$V_{CC} = 5.5 V$	3.85			
		V _{CC} = 2 V		0.5		
V_{IL}	Low-level input voltage	V _{CC} = 3 V		0.9	V	
		$V_{CC} = 5.5 V$		1.65		
٧ _I	Input voltage		0	5.5	V	
٧o	Output voltage		0	VCC	V	
		V _{CC} = 2 V		-50	μΑ	
IOH	High-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		-4	A	
		$V_{CC} = 5 V \pm 0.5 V$		-8	mA	
		V _{CC} = 2 V		50	μΑ	
loL	Low-level output current $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$			4	A	
		$V_{CC} = 5 V \pm 0.5 V$		8	mA	
A+/A>-	Input transition rise or fall rate $ \frac{\text{V}_{CC} = 3.3 \text{ V}}{\text{V}_{CC} = 5 \text{ V} \pm} $			100	ns/V	
Δt/Δv				20	115/ V	
TA	Operating free-air temperature		-55	125	°C	

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

^{2.} The package thermal impedance is calculated in accordance with JESD 51-7.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	Vaa	T,	ղ = 25°C	;	MIN	MAX	UNIT
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	IVIIIN	WAX	ONIT
		2 V	1.9	2		1.9		
VOH	I _{OH} = -50 μA	3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		V
	I _{OH} = -4 mA	3 V	2.58			2.48		
	I _{OH} = -8 mA	4.5 V	3.94			3.8		
		2 V			0.1		0.1	
	I _{OL} = 50 μA	3 V			0.1		0.1	
V _{OL}		4.5 V			0.1		0.1	V
	I _{OL} = 4 mA	3 V			0.36		0.5	
	I _{OL} = 8 mA	4.5 V			0.36		0.5	
Ι _Ι	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1	μΑ
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			2		20	μΑ
Ci	V _I = V _{CC} or GND	5 V		2	10			pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	LOAD	T,	λ = 25°C	;	MIN	MAX	UNIT
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	IVIIIV	WAX	ON
^t PLH	A or B	V	C _L = 15 pF		5.5	7.9	1	9.5	no
t _{PHL}	AUID	Ť			5.5	7.9	1	9.5	ns
^t PLH	A or B	V	C: - 50 pF		8	11.4	1	13	20
t _{PHL}	AUID	ſ	C _L = 50 pF		8	11.4	1	13	ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	LOAD	T _A = 25°C			MIN	MAX	UNIT
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	IVIIIN	WAX	UNIT
t _{PLH}	A or B	Y	C _L = 15 pF		3.7	5.5	1	6.5	ns
t _{PHL}	AOIB				3.7	5.5	1	6.5	1115
t _{PLH}	A or B	V	C _L = 50 pF		5.2	7.5	1	8.5	
t _{PHL}	AUB	ī			5.2	7.5	1	8.5	ns

noise characteristics, $V_{CC} = 5 \text{ V}$, $C_L = 50 \text{ pF}$, $T_A = 25^{\circ}\text{C}$ (see Note 4)

	PARAMETER	MIN	TYP	MAX	UNIT
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}		0.3	0.8	V
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}		-0.3	-0.8	V
V _{OH(V)}	Quiet output, minimum dynamic VOH		4.6		V
V _{IH(D)}	High-level dynamic input voltage	3.5			V
V _{IL(D)}	Low-level dynamic input voltage			1.5	V

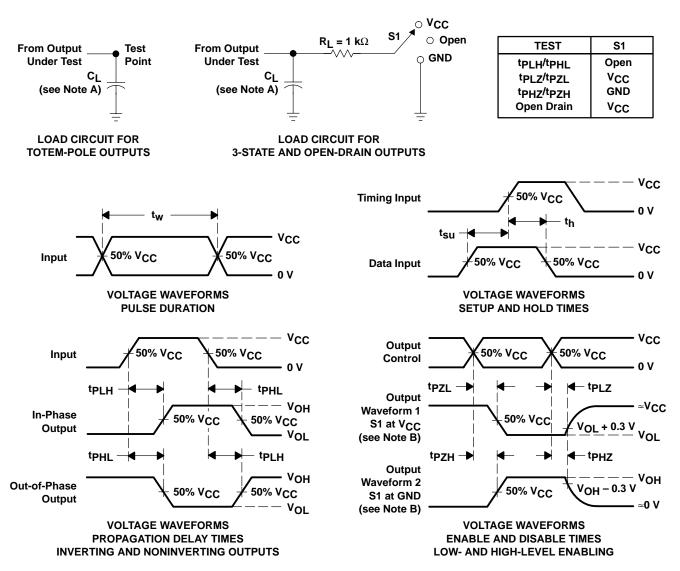
NOTE 4: Characteristics are for surface-mount packages only.



operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST C	ONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	No load,	f = 1 MHz	9.5	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z_O = 50 Ω , $t_f \leq$ 3 ns, $t_f \leq$ 3 ns.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms







.com 18-Sep-2008

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74AHC00MDREP	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC00MPWREP	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/03604-01XE	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/03604-01YE	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74AHC00-EP:

Catalog: SN74AHC00
Automotive: SN74AHC00-C

Automotive: SN74AHC00-Q1Military: SN54AHC00

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC00MDREP	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC00MPWREP	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC00MDREP	SOIC	D	14	2500	333.2	345.9	28.6
SN74AHC00MPWREP	TSSOP	PW	14	2000	346.0	346.0	29.0

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
 - Sody length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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