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SCES2240 - APRIL 1999 - REVISED MARCH 2012

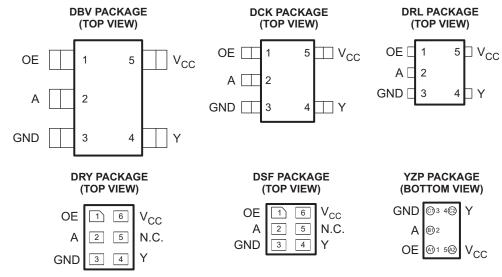
SINGLE BUS BUFFER GATE WITH 3-STATE OUTPUT

Check for Samples: SN74LVC1G126

FEATURES

- Available in the Texas Instruments NanoFree™ **Package**
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 3.7 ns at 3.3 V
- Low Power Consumption, 10-µA Max I_{CC}
- ±24-mA Output Drive at 3.3 V
- I_{off} Supports Partial-Power-Down Mode Operation

- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



N.C. - No internal connection

See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

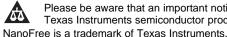
This single bus buffer gate is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G126 is a single line driver with a 3-state output. The output is disabled when the output-enable (OE) input is low.

NanoFree[™] package technology is a major breakthrough in IC packaging concepts, using the die as the package.

To ensure the high-impedance state during power up or power down. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



ORDERING INFORMATION

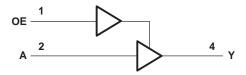
T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING (2)
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb- free)	Reel of 3000	SN74LVC1G126YZPR	CN_
	SON - DRY	Reel of 5000	SN74LVC1G126DRYR	CN
	μQFN – DSF	Reel of 5000	SN74LVC1G126DSFR	CN
–40°C to 85°C	SOT (SOT-23) – DBV	Reel of 3000	SN74LVC1G126DBVR	- C26
	301 (301-23) – DBV	Reel of 250	SN74LVC1G126DBVT	C20_
	SOT (SC-70) – DCK	Reel of 3000	SN74LVC1G126DCKR	CN
	SOT (SC-70) - DCK	Reel of 250	SN74LVC1G126DCKT	CN_
	SOT (SOT-553) – DRL	Reel of 4000	SN74LVC1G126DRLR	CN_

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
- (2) DBV/DCK/DRLY: The actual top-side marking has one additional character that designates the assembly/test site. YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, = Pb-free).

FUNCTION TABLE

INP	OUTPUT	
OE	Α	Υ
Н	Н	Н
Н	L	L
L	Χ	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



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ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	6.5	V
VI	Input voltage range ⁽²⁾	Input voltage range ⁽²⁾			V
Vo	Voltage range applied to any output in the	high-impedance or power-off state (2)	-0.5	6.5	V
Vo	Voltage range applied to any output in the high or low state ⁽²⁾ (3)		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V ₁ < 0		-50	mA
lok	Output clamp current	V _O < 0		-50	mA
lo	Continuous output current		±50	mA	
	Continuous current through V _{CC} or GND			±100	mA
		DBV package		206	
		DCK package		252	
θ_{JA}	Package thermal impedance (4)	DRL package		142	°C/W
		DRY package		234	
		YZP package		132	
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

⁽²⁾ The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

³⁾ The value of V_{CC} is provided in the recommended operating conditions table.

⁽⁴⁾ The package thermal impedance is calculated in accordance with JESD 51-7.



RECOMMENDED OPERATING CONDITIONS(1)

			MIN	MAX	UNIT	
.,	Complexion	Operating	1.65	5.5	V	
V_{CC}	Supply voltage	Data retention only	1.5		v	
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}			
.,	Liber level beaut value	V _{CC} = 2.3 V to 2.7 V	1.7		V	
V_{IH}	High-level input voltage	V _{CC} = 3 V to 3.6 V	2		V	
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}			
		V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}		
.,	Lave lavel in motoraliana	V _{CC} = 2.3 V to 2.7 V		0.7		
V_{IL}	Low-level input voltage	V _{CC} = 3 V to 3.6 V		0.8	V	
		V _{CC} = 4.5 V to 5.5 V		0.3 × V _{CC}		
VI	Input voltage		0	5.5	V	
Vo	Output voltage		0	V _{CC}	V	
		V _{CC} = 1.65 V		-4		
		V _{CC} = 2.3 V		-8		
I_{OH}	High-level output current			-16	mA	
		V _{CC} = 3 V		-24		
		V _{CC} = 4.5 V		-32		
		V _{CC} = 1.65 V		4		
		V _{CC} = 2.3 V		8		
I_{OL}	Low-level output current			16	mA	
		V _{CC} = 3 V		24		
		V _{CC} = 4.5 V		32		
		$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}, 2.5 \text{ V} \pm 0.2 \text{ V}$		20		
Δt/Δν	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10		
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		5		
T _A	Operating free-air temperature		-40	85	°C	

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{cc}	MIN	TYP ⁽¹⁾ MAX	UNIT		
	$I_{OH} = -100 \mu A$	1.65 V to 5.5 V	V _{CC} - 0.1				
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2				
V	$I_{OH} = -8 \text{ mA}$	2.3 V	1.9	V			
V _{OH}	$I_{OH} = -16 \text{ mA}$	3 V	2.4		V		
	$I_{OH} = -24 \text{ mA}$	3 V	2.3				
	$I_{OH} = -32 \text{ mA}$	4.5 V	3.8				
	$I_{OL} = 100 \ \mu A$	1.65 V to 5.5 V		0.1			
	$I_{OL} = 4 \text{ mA}$	1.65 V		0.45			
V	$I_{OL} = 8 \text{ mA}$	2.3 V		0.3	V		
V _{OL}	$I_{OL} = 16 \text{ mA}$	3 V		0.4	V		
	$I_{OL} = 24 \text{ mA}$	3 V		0.55			
	$I_{OL} = 32 \text{ mA}$	4.5 V		0.55			
I _I A or OE inputs	$V_I = 5.5 \text{ V or GND}$	0 to 5.5 V		±5	μA		
I _{off}	V_I or $V_O = 5.5 \text{ V}$	0		±10	μΑ		
I_{OZ}	$V_{O} = 0 \text{ to } 5.5 \text{ V}$	3.6 V		10	μA		
I _{CC}	$V_I = 5.5 \text{ V or GND}$ $I_O = 0$	1.65 V to 5.5 V		10	μΑ		
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 5.5 V		500	μΑ		
C _i	$V_I = V_{CC}$ or GND	3.3 V		4	pF		

⁽¹⁾ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SWITCHING CHARACTERISTICs

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = ± 0.1		V _{CC} = ± 0.2		V _{CC} = ± 0.		V _{CC} : ± 0.	= 5 V .5 V	UNIT
	(INPUT)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	Α	Υ	1.7	6.9	0.6	4.6	0.6	3.7	0.5	3.4	ns

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ or 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = ± 0.		V _{CC} = ± 0.2		V _{CC} = ± 0.	3.3 V 3 V	V _{CC} = ± 0.		UNIT
	(INFOT)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	Α	Υ	2.6	8	1.1	5.5	1	4.5	1	4	ns
t _{en}	OE	Υ	2.8	9.4	1.3	6.6	1.2	5.3	1	5	ns
t _{dis}	OE	Υ	1.6	9.8	1	5.5	1	5.5	1	4.2	ns

OPERATING CHARACTERISTICS

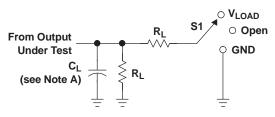
 $T_A = 25^{\circ}C$

	PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	V _{CC} = 5 V TYP	UNIT
_	Power dissipation	Outputs enabled	f = 10 MHz	19	19	19	21	ρF
Cpd	capacitance	Outputs disabled	I = IU IVIAZ	2	2	3	4	рг

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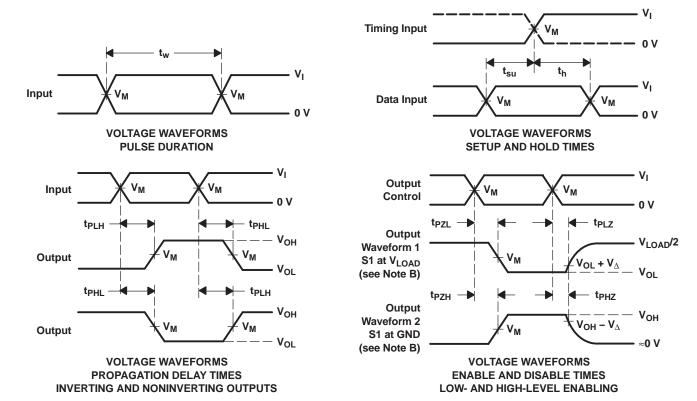
PARAMETER MEASUREMENT INFORMATION



TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

п	0	Δ	ח	CI	R	CI	П	IT

V	INPUTS		V	V			V
V _{CC}	VI	t _r /t _f	V _M	V _{LOAD}	CL	R _L	V_{Δ}
1.8 V \pm 0.15 V	V _{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	15 pF	1 M Ω	0.15 V
2.5 V \pm 0.2 V	V _{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	15 pF	1 M Ω	0.15 V
3.3 V \pm 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	15 pF	1 M Ω	0.3 V
5 V \pm 0.5 V	V _{CC}	≤2.5 ns	V _{CC} /2	2×V _{CC}	15 pF	1 M Ω	0.3 V



NOTES: A. C_L includes probe and jig capacitance.

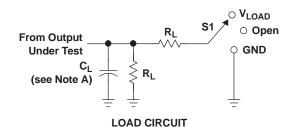
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

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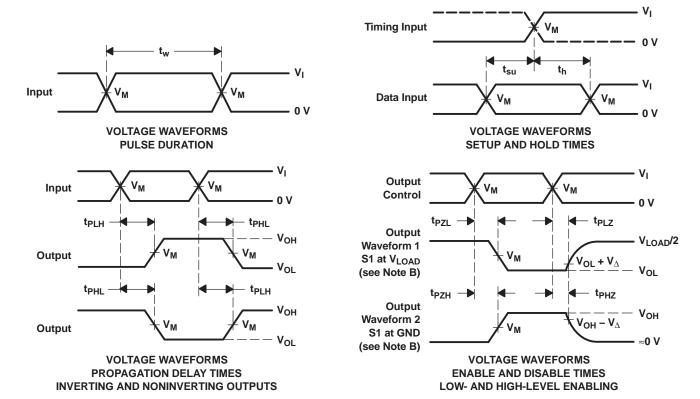


PARAMETER MEASUREMENT INFORMATION (continued)



TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

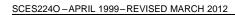
.,	INF	PUTS	.,	.,		-	v
V _{CC}	VI	t _r /t _f	V _M	V _{LOAD}	CL	R _L	$oldsymbol{V}_\Delta$
1.8 V \pm 0.15 V	V _{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	30 pF	1 k Ω	0.15 V
2.5 V \pm 0.2 V	V _{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	30 pF	500 Ω	0.15 V
3.3 V \pm 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V \pm 0.5 V	V _{CC}	≤2.5 ns	V _{CC} /2	2×V _{CC}	50 pF	500 Ω	0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en}.
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

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REVISION HISTORY

Ch	Changes from Revision N (February 2007) to Revision O						
•	Added DSF package option to the datasheet.		1				

1-Jun-2012

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
74LVC1G126DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74LVC1G126DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74LVC1G126DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74LVC1G126DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74LVC1G126DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74LVC1G126DCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74LVC1G126DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74LVC1G126DRLRG4	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74LVC1G126DRYRG4	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74LVC1G132DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G126DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G126DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G126DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G126DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G126DRLR	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G126DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G126DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	



PACKAGE OPTION ADDENDUM

1-.lun-2012

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74LVC1G126YZPR	ACTIVE	DSBGA	YZP	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74LVC1G126:

Automotive: SN74LVC1G126-Q1

Enhanced Product: SN74LVC1G126-EP

NOTE: Qualified Version Definitions:

Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects





1-Jun-2012

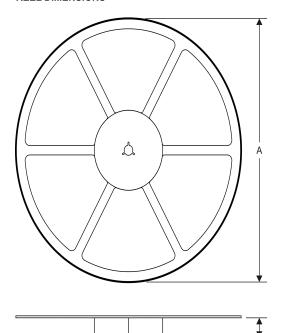
• Enhanced Product - Supports Defense, Aerospace and Medical Applications

PACKAGE MATERIALS INFORMATION

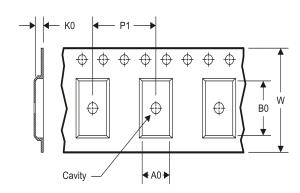
www.ti.com 1-Jun-2012

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

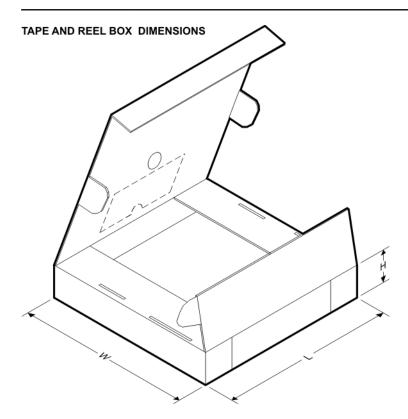
TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G126DBVR	SOT-23	DBV	5	3000	180.0	9.2	3.17	3.23	1.37	4.0	8.0	Q3
SN74LVC1G126DBVR	SOT-23	DBV	5	3000	178.0	9.2	3.3	3.2	1.55	4.0	8.0	Q3
SN74LVC1G126DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G126DBVT	SOT-23	DBV	5	250	180.0	9.2	3.17	3.23	1.37	4.0	8.0	Q3
SN74LVC1G126DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G126DBVT	SOT-23	DBV	5	250	178.0	9.2	3.3	3.2	1.55	4.0	8.0	Q3
SN74LVC1G126DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G126DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G126DCKR	SC70	DCK	5	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1G126DCKT	SC70	DCK	5	250	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1G126DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G126DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G126DRLR	SOT	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1G126DRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
SN74LVC1G126DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G126YZPR	DSBGA	YZP	5	3000	180.0	8.4	1.02	1.52	0.63	4.0	8.0	Q1

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G126DBVR	SOT-23	DBV	5	3000	205.0	200.0	33.0
SN74LVC1G126DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G126DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G126DBVT	SOT-23	DBV	5	250	205.0	200.0	33.0
SN74LVC1G126DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G126DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G126DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G126DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G126DCKR	SC70	DCK	5	3000	205.0	200.0	33.0
SN74LVC1G126DCKT	SC70	DCK	5	250	205.0	200.0	33.0
SN74LVC1G126DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G126DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G126DRLR	SOT	DRL	5	4000	202.0	201.0	28.0
SN74LVC1G126DRYR	SON	DRY	6	5000	203.0	203.0	35.0
SN74LVC1G126DSFR	SON	DSF	6	5000	180.0	180.0	30.0
SN74LVC1G126YZPR	DSBGA	YZP	5	3000	220.0	220.0	34.0

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.



DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AA.



DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



DRL (R-PDSO-N5)

PLASTIC SMALL OUTLINE



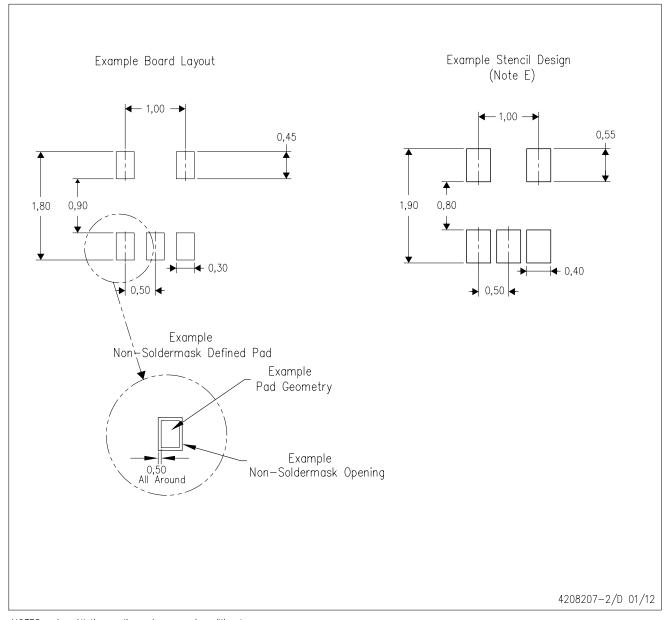
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs.

 Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
- D. JEDEC package registration is pending.



DRL (R-PDSO-N5)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Side aperture dimensions over—print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.





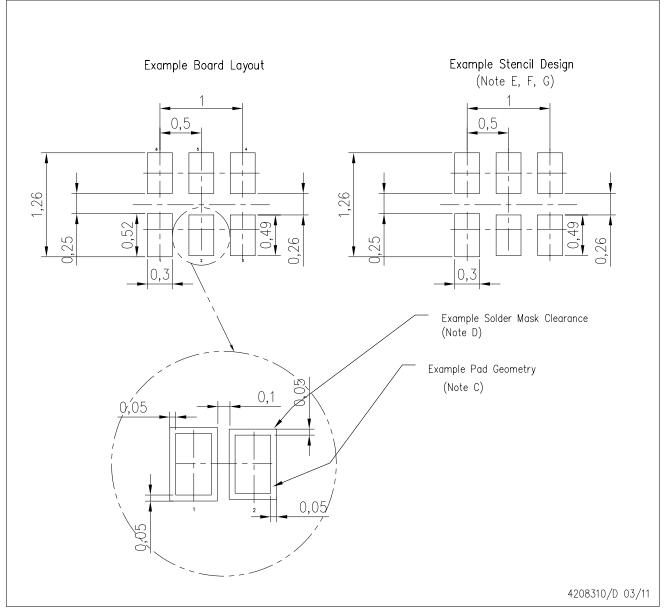
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. SON (Small Outline No-Lead) package configuration.
- The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
- E. This package complies to JEDEC MO-287 variation UFAD.
- $frac{f}{K}$ See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.



DRY (S-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES: A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.





NOTES: All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.

- B. This drawing is subject to change without notice.
 C. SON (Small Outline No-Lead) package configuration.
 D. This package complies to JEDEC MO-287 variation X2AAF.





PLASTIC SMALL OUTLINE NO-LEAD

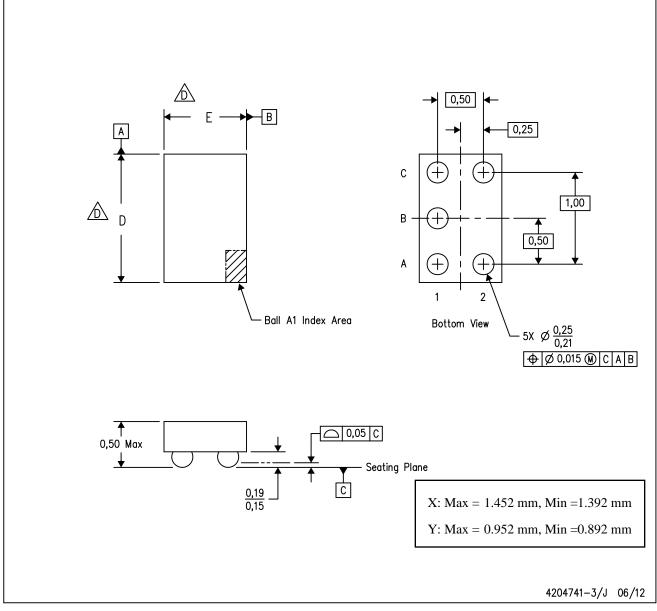


- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
- E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
- H. Component placement force should be minimized to prevent excessive paste block deformation.



YZP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.
- The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
- E. This package is a Pb-free solder ball design. Refer to the 5 YEP package (drawing 4204725) for tin-lead (SnPb).

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