

FEATURES

- Controlled Baseline
 - One Assembly/Test Site, One Fabrication Site
- Extended Temperature Performance of -55°C to 125°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree (1)
- Inputs Are TTL-Voltage Compatible
- Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption
- Balanced Propagation Delays
- ±24-mA Output Drive Current
 - Fanout to 15 F Devices
- (1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

DESCRIPTION/ORDERING INFORMATION

The CD74ACT86-EP is a quadruple 2-input exclusive-OR gate. This device performs the Boolean function $Y = A \oplus B$ or $Y = \overline{AB} + A\overline{B}$ in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

T _A	PACKAG	Е ⁽¹⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOIC – D	Tape and Reel	CD74ACT86MDREP	ACT86MEP

ORDERING INFORMATION

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

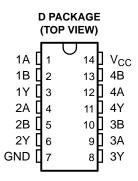
		,			
INP	INPUTS				
Α	В	Y			
L	L	L			
L	Н	н			
Н	L	н			
Н	Н	L			

FUNCTION TABLE (EACH GATE)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

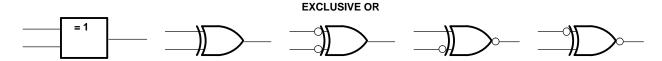
• Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015



SCHS357-MARCH 2006

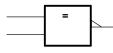
Exclusive-OR Logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

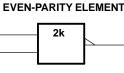


These are five equivalent exclusive-OR symbols valid for an CD74ACT86-EP gate in positive logic; negation may be shown at any two ports.

LOGIC-IDENTITY ELEMENT

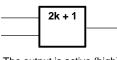


The output is active (low) if all inputs stand at the same logic level (i.e., A = B).



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6	V
I _{IK}	Input clamp current ⁽²⁾	$V_{I} < 0 \text{ or } V_{I} > V_{CC}$		±20	mA
I _{OK}	Output clamp current ⁽²⁾	$V_{O} < 0 \text{ or } V_{O} > V_{CC}$		±50	mA
I _O	Continuous output current	$V_{O} = 0$ to V_{CC}		±50	mA
	Continuous current through V _{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance ⁽³⁾			86	°C/W
T _{stg}	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

		T _A =	25°C	–55°C to 125°C		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
VI	Input voltage	0	V _{CC}	0	V_{CC}	V
Vo	Output voltage	0	V _{CC}	0	V_{CC}	V
I _{OH}	High-level output current		-24		-24	mA
I _{OL}	Low-level output current		24		24	mA
$\Delta t / \Delta v$	Input transition rise or fall rate		10		10	ns/V

 All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST C	TEST CONDITIONS			T _A = 25°C		–55°C to 125°C	
			V _{cc}	MIN	MAX	MIN	MAX	
		I _{OH} = -50 μA	4.5 V	4.4		4.4		
V_{OH} $V_I = V_{IH} \text{ or } V_{IL}$	$V_I = V_{IH} \text{ or } V_{IL}$	I _{OH} = -24 mA	4.5 V	3.94		3.7		V
		$I_{OH} = -50 \text{ mA}^{(1)}$	5.5 V	3.85		3.85		
		I _{OL} = 50 μA	4.5 V		0.1		0.1	
V _{OL}	$V_I = V_{IH} \text{ or } V_{IL}$	I _{OL} = 24 mA	4.5 V		0.36		0.5	V
		I _{OL} = 50 mA ⁽¹⁾	5.5 V		1.65		1.65	
I _I	$V_{I} = V_{CC}$ or GND		5.5 V		±0.1		±1	μΑ
I _{CC}	$V_I = V_{CC}$ or GND,	I _O = 0	5.5 V		4		80	μA
$\Delta I_{CC}^{(2)}$	$V_{I} = V_{CC} - 2.1 V$		4.5 V to 5.5 V		2.4		3	mA
C _i					10		10	pF

(1) Test one output at a time, not exceeding 1-s duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

(2) Additional quiescent supply current per input pin, TTL inputs high, 1 unit load

ACT INPUT LOAD TABLE⁽¹⁾

INPUT	UNIT LOAD
All	0.48

Unit load is ∆I_{CC} limit specified in electrical characteristics table (e.g., 2.4 mA at 25°C).

Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

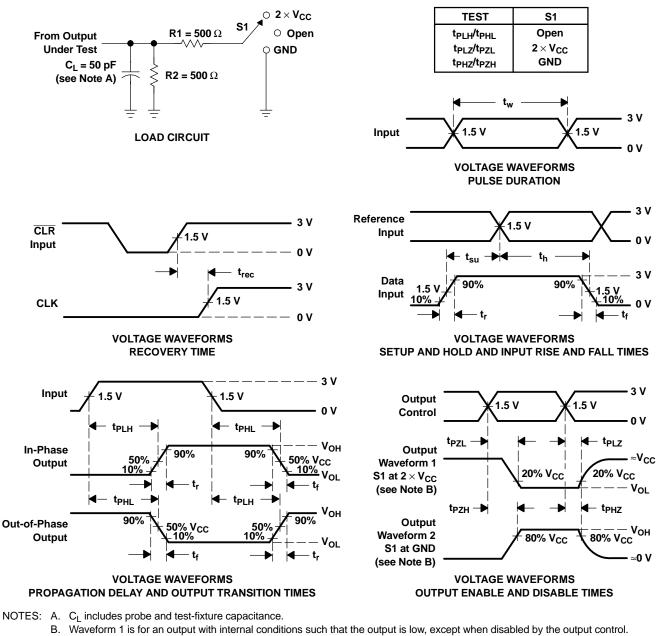
PARAMETER	FROM (INPUT)	TO (OUTPUT)	–55°C 125°		UNIT
	(INFOT)	(601-01)	MIN	MAX	
t _{PLH}	A or B	V	3.7	14.6	20
t _{PHL}	AOIB	Ť	3.7	14.6	ns

Operating Characteristics

 $V_{CC} = 5 \text{ V}, \text{ T}_{A} = 25^{\circ}\text{C}$

	PARAMETER	ТҮР	UNIT
C _{pd}	Power dissipation capacitance	57	pF

CD74ACT86-EP **QUADRUPLE 2-INPUT EXCLUSIVE-OR GATE** SCHS357-MARCH 2006



PARAMETER MEASUREMENT INFORMATION

Texas

STRUMENTS www.ti.com

- - Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control. C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z_O = 50 Ω , t_r = 3 ns, t_f = 3 ns.
 - Phase relationships between waveforms are arbitrary.
 - D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
 - E. The outputs are measured one at a time, with one input transition per measurement.
 - F. t_{PLH} and t_{PHL} are the same as t_{pd}.
 - G. t_{PZL} and t_{PZH} are the same as t_{en}.
 - H. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - I. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Qty Eco Plan ⁽²⁾ Lead/ Ball Finish		MSL Peak Temp ⁽³⁾	Samples (Requires Login)
CD74ACT86MDREP	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Add to cart
V62/06620-01XE	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Add to cart

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF CD74ACT86-EP :

Catalog: CD74ACT86





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9-May-2012

• Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal	
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Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74ACT86MDREP	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1



PACKAGE MATERIALS INFORMATION

5-Aug-2008



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74ACT86MDREP	SOIC	D	14	2500	346.0	346.0	33.0

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.





NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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