D OR PW PACKAGE (TOP VIEW)

1A

1B 🛛 2

1Y 🛛 3

2A 4

2B 🛛 5

2Y **6** 

GND 7

14 Vcc

13 4B

12 4A

11 **1** 4Y

10 3B

9 🛛 3A

8 3Y

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- Controlled Baseline
  One Assembly/Test Site, One Fabrication Site
- Extended Temperature Performance of -55°C to 125°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree<sup>†</sup>
- EPIC<sup>™</sup> (Enhanced-Performance Implanted CMOS) Process
- Operating Range 2-V to 5.5-V V<sub>CC</sub>
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)

<sup>†</sup> Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

#### description/ordering information

The SN74AHC32 is a quadruple 2-input positive-OR gate. This device performs the Boolean function  $Y = \overline{\overline{A} \cdot \overline{B}}$  or Y = A + B in positive logic.

#### **ORDERING INFORMATION**

TA	PACK	AGE <sup>‡</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
55°C to 125°C	SOIC – D	Tape and reel	SN74AHC32MDREP	AHC32MEP
–55°C to 125°C	TSSOP – PW	Tape and reel	SN74AHC32MPWREP	AHC32EP

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**FUNCTION TABLE** 

	(each g	jate)
INP	UTS	OUTPUT
Α	В	Y
н	Х	н
х	Н	н
L	L	L



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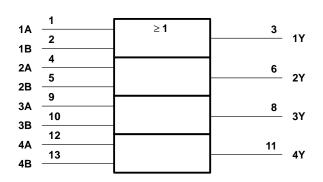
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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#### logic symbol<sup>†</sup>



<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>‡</sup>

Supply voltage range, $V_{CC}$ Input voltage range, $V_I$ (see Note 1) Output voltage range, $V_O$ (see Note 1) Input clamp current, $I_{IK}$ ( $V_I < 0$ ) Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) Continuous current through $V_{CC}$ or GND Package thermal impedance, $\theta_{JA}$ (see Note 2): D package	$\begin{array}{c} -0.5 \ V \ to \ 7 \ V \\ p \ V_{CC} + 0.5 \ V \\ \dots \ -20 \ mA \\ \dots \ \pm 20 \ mA \\ \dots \ \pm 25 \ mA \\ \dots \ \pm 50 \ mA \\ \dots \ 86^{\circ}C/W \end{array}$
PW package	
Storage temperature range, T <sub>stg</sub> e	

<sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.



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#### recommended operating conditions (see Note 3)

			MIN	MAX	UNIT	
VCC	Supply voltage		2	5.5	V	
		$V_{CC} = 2 V$	1.5			
VIH	High-level input voltage	$V_{CC} = 3 V$	2.1		V	
		V <sub>CC</sub> = 5.5 V	3.85			
		$V_{CC} = 2 V$		0.5		
VIL	Low-level input voltage	$V_{CC} = 3 V$		0.9	V	
		V <sub>CC</sub> = 5.5 V		1.65		
VI	Input voltage		0	5.5	V	
٧ <sub>0</sub>	Output voltage		0	VCC	V	
		$V_{CC} = 2 V$		-50	μA	
ЮН	High-level output current	$V_{CC}$ = 3.3 V ± 0.3 V		-4	A	
		$V_{CC}$ = 5 V ± 0.5 V		-8	mA	
		$V_{CC} = 2 V$		50	μA	
IOL	Low-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		4	A	
		$V_{CC}$ = 5 V ± 0.5 V		8	mA	
A+/A.	Input transition rise or fell rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		100	<b>n</b> o///	
Δt/Δv	Input transition rise or fall rate	$V_{CC} = 5 V \pm 0.5 V$		20	ns/V	
Т <sub>А</sub>	Operating free-air temperature		-55	125	°C	

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	Vee	T,	λ = 25°C		MIN	МАХ	UNIT	
PARAMETER	TEST CONDITIONS	vcc	MIN	TYP	MAX	IVITIN	MAX	UNIT	
		2 V	1.9	2		1.9			
	I <sub>OH</sub> = -50 μA	3 V	2.9	3		2.9			
VOH		4.5 V	4.4	4.5		4.4		V	
	$I_{OH} = -4 \text{ mA}$	3 V	2.58			2.48			
	I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8			
		2 V			0.1		0.1	1	
	I <sub>OL</sub> = 50 μA	3 V			0.1		0.1		
VOL		4.5 V			0.1		0.1	V	
	I <sub>OL</sub> = 4 mA	3 V			0.36		0.5		
	I <sub>OL</sub> = 8 mA	4.5 V			0.36		0.5		
lį	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V			±0.1		±1	μΑ	
ICC	$V_{I} = V_{CC} \text{ or GND}, \qquad I_{O} = 0$	5.5 V			2		20	μΑ	
Ci	$V_{I} = V_{CC}$ or GND	5 V		2	10			рF	



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# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO (OUTPUT)	LOAD	T <sub>A</sub> = 25°C			MIN	МАХ	UNIT
	(INPUT)		CAPACITANCE	MIN	TYP	MAX		WAA	
<sup>t</sup> PLH	A or B	Y	C <sub>L</sub> = 15 pF		5.5	7.9	1	9.5	ns
<sup>t</sup> PHL	AUID				5.5	7.9	1	9.5	
<sup>t</sup> PLH	A or B	V	0. 50 pF		8	11.4	1	13	ns
<sup>t</sup> PHL		ſ	C <sub>L</sub> = 50 pF		8	11.4	1	13	

# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	LOAD	Т	ן = 25°C	;	MIN	МАХ	UNIT
FARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX		MAA	UNIT
<sup>t</sup> PLH	A or B	v	Ct = 15 pE		3.8	5.5	1	6.5	20
<sup>t</sup> PHL	AUB	T	C <sub>L</sub> = 15 pF		3.8	5.5	1	6.5	ns
<sup>t</sup> PLH	A or B	V	$C_{\rm r} = 50  \rm pF$		5.3	7.5	1	8.5	20
<sup>t</sup> PHL	AUB	ſ	C <sub>L</sub> = 50 pF		5.3	7.5	1	8.5	ns

# noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

	PARAMETER	MIN	TYP	MAX	UNIT
VOL(P)	Quiet output, maximum dynamic V <sub>OL</sub>		0.3	0.8	V
VOL(V)	Quiet output, minimum dynamic V <sub>OL</sub>		-0.3	-0.8	V
VOH(V)	Quiet output, minimum dynamic V <sub>OH</sub>		4.7		V
VIH(D)	High-level dynamic input voltage	3.5			V
V <sub>IL(D)</sub>	Low-level dynamic input voltage			1.5	V

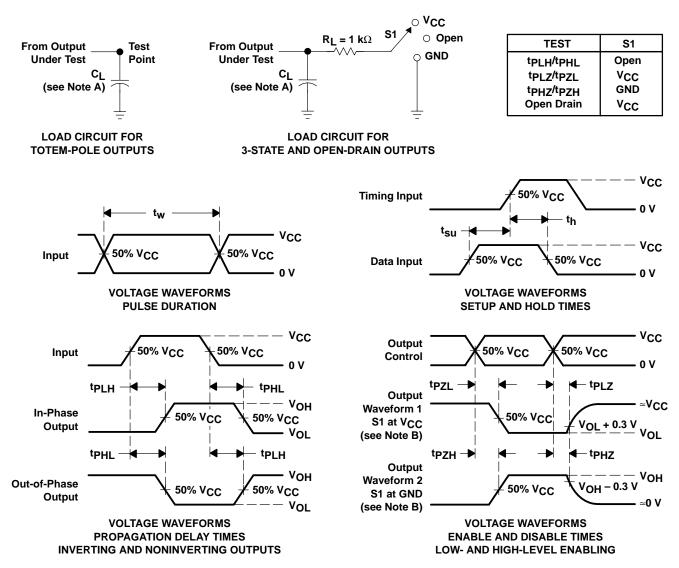
NOTE 4: Characteristics are for surface-mount packages only.

### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

	PARAMETER	TEST C	ONDITIONS	TYP	UNIT
Cpd	Power dissipation capacitance	No load,	f = 1 MHz	14	pF



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PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>f</sub>  $\leq$  3 ns, t<sub>f</sub>  $\leq$  3 ns.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



#### PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74AHC32MDREP	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC32MPWREP	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/03651-01XE	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/03651-01YE	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### OTHER QUALIFIED VERSIONS OF SN74AHC32-EP :

- Catalog: SN74AHC32
- Military: SN54AHC32

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

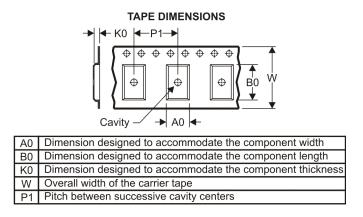
# PACKAGE MATERIALS INFORMATION

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### TAPE AND REEL INFORMATION





### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC32MDREP	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC32MPWREP	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

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# PACKAGE MATERIALS INFORMATION

30-Jul-2010



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC32MDREP	SOIC	D	14	2500	333.2	345.9	28.6
SN74AHC32MPWREP	TSSOP	PW	14	2000	346.0	346.0	29.0

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