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- High Capacitive-Drive Capability
- 'ALS832A Has Typical Delay Time of 4.8 ns (C_L = 50 pF) and Typical Power Dissipation of 4.5 mW Per Gate
- 'AS832B Has Typical Delay Time of 3.2 ns (C_L = 50 pF) and Typical Power Dissipation of Less Than 13 mW Per Gate
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

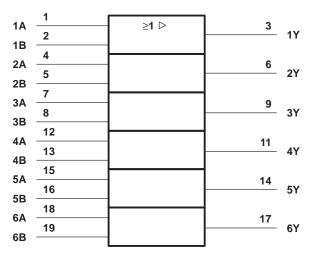
These devices contain six independent 2-input OR drivers. They perform the Boolean functions Y = A + B or $Y = \overline{A \cdot B}$ in positive logic.

The SN54ALS832A and SN54AS832B are characterized for operation over the full military temperature range of -55° C to 125° C. The SN74ALS832A and SN74AS832B are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each driver)

INP	UTS	OUTPUT
А	В	Y
н	Х	Н
X	Н	Н
L	L	L

logic symbol[†]



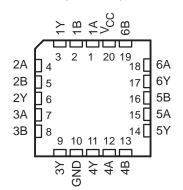
⁺ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

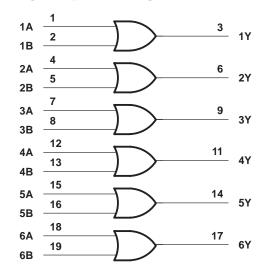


SN54ALS832A, SN54AS832B . . . J PACKAGE SN74ALS832A, SN74AS832B . . . DW OR N PACKAGE (TOP VIEW)

SN54ALS832A, SN54AS832B . . . FK PACKAGE (TOP VIEW)



logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V _{CC}	
Input voltage, V _I	/ V
Operating free-air temperature range, T _A : SN54ALS832A	–55°C to 125°C
SN74ALS832A	0°C to 70°C
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54ALS832A			SN7	UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
IOH	High-level output current			-12			-15	mA
IOL	Low-level output current			12			24	mA
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CO	TEST CONDITIONS				SN7	UNIT		
PARAMETER	TEST CC	JNDITIONS	MIN	typ‡	MAX	MIN	typ‡	MAX	UNIT
VIK	V _{CC} = 4.5 V,	lı = -18 mA			-1.5			-1.5	V
	V_{CC} = 4.5 V to 5.5 V,	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -2	2		V _{CC} -2	2		
VOH		$I_{OH} = -3 \text{ mA}$	2.4	2.4 3.2 2.4 3.2		3.2		v	
VОН	$V_{CC} = 4.5 V$	I _{OH} = -12 mA	2						v
		I _{OH} = -15 mA				2			
VOL		I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
VOL	V _{CC} = 4.5 V	I _{OL} = 24 mA					0.35	0.5	v
l	V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA
ЧΗ	V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μΑ
١ _{١L}	V _{CC} = 5.5 V,	$V_{I} = 0.4 V$			-0.1			-0.1	mA
١O§	V _{CC} = 5.5 V,	V _O = 2.25 V	-20		-112	-30		-112	mA
IССН	V _{CC} = 5.5 V,	V _I = 4.5 V		6	9		6	9	mA
ICCL	V _{CC} = 5.5 V,	$V_{I} = 0$		9.5	16		9.5	16	mA

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

\$ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.



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switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	Ci Ri	V_{CC} = 4.5 V to 5.5 V, C_{L} = 50 pF, R_{L} = 500 Ω, T_{A} = MIN to MAX [†]					
			SN54AL	SN54ALS832A MIN MAX		SN54ALS832A SN74AL		S832A	
			MIN			MAX			
^t PLH	A or B	v	1	13	2	9			
^t PHL		· ·	1	11	1	8	ns		

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage, V _{CC}	
Operating free-air temperature range, T _A : SN54AS832B	-55°C to 125°C
SN74AS832B	0°C to 70°C
Storage temperature range	-65°C to 150°C

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions§

		SN54AS832B			SN	UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
ЮН	High-level output current			-40			-48	mA
IOL	Low-level output current			40			48	mA
TA	Operating free-air temperature	-55		125	0		70	°C

§ These high sink- or source-current devices are not recommended for use above 40 MHz.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST C	TEST CONDITIONS			2B	SN7	UNIT		
PARAMETER	TEST CO					MIN	TYP†	MAX	UNIT
VIK	V _{CC} = 4.5 V,	lı = -18 mA			-1.2			-1.2	V
	V_{CC} = 4.5 V to 5.5 V,	$I_{OH} = -2 \text{ mA}$	V _{CC} -2			V _{CC} -2			
Vou		$I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2		V
VOH	$V_{CC} = 4.5 V$	$I_{OH} = -40 \text{ mA}$	2						v
		$I_{OH} = -48 \text{ mA}$				2			
Ve	V _{CC} = 4.5 V	I _{OL} = 40 mA		0.25	0.5				V
VOL	$v_{CC} = 4.5 v$	I _{OL} = 48 mA					0.35	0.5	v
lį	V _{CC} = 5.5 V,	$V_{I} = 7 V$			0.1			0.1	mA
ΙΗ	V _{CC} = 5.5 V,	VI = 2.7 V			20			20	μA
١	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.5			-0.5	mA
۱ ₀ ‡	V _{CC} = 5.5 V,	V _O = 2.25 V	-50		-200	-50		-200	mA
Іссн	V _{CC} = 5.5 V,	VI = 4.5 V		11	17		11	17	mA
ICCL	V _{CC} = 5.5 V,	$V_{I} = 0$		22	36		22	36	mA

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

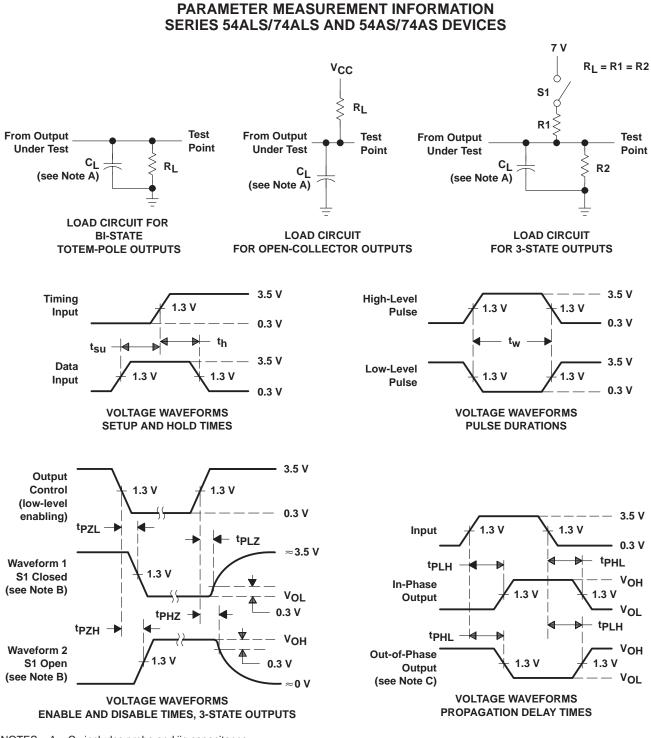
switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CL RL TA	= 50 pF = 500 Ω = MIN t	2, o MAX§		UNIT
			SN54A	S832B	SN74A	S832B	
			MIN	MAX	MIN	MAX	
^t PLH	A or B	V	1	7.5	1	6.3	ns
^t PHL	7010		1	7	1	6.3	115

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



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NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
- D. All input pulses have the following characteristics: PRR \leq 1 MHz, t_{f} = t_{f} = 2 ns, duty cycle = 50\%.
- E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms





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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-88523012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-8852301RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Call TI	
5962-8852301SA	ACTIVE	CFP	W	20	1	TBD	Call TI	Call TI	
84145012A	NRND	LCCC	FK	20	1	TBD	Call TI	Call TI	
8414501RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Call TI	
SN54ALS832AJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SN54AS832BJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SN74ALS832ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS832ADWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS832ADWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS832AN	ACTIVE	PDIP	Ν	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74ALS832ANE4	ACTIVE	PDIP	Ν	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74AS832BDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS832BDWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS832BDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS832BDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS832BDWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS832BDWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS832BN	ACTIVE	PDIP	Ν	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74AS832BNE4	ACTIVE	PDIP	Ν	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SNJ54ALS832AFK	NRND	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54ALS832AJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SNJ54AS832BFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	



Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SNJ54AS832BJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SNJ54AS832BW	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54ALS832A, SN54AS832B, SN74ALS832A, SN74AS832B :

• Catalog: SN74ALS832A, SN74AS832B

• Military: SN54ALS832A, SN54AS832B

NOTE: Qualified Version Definitions:

PACKAGE OPTION ADDENDUM



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• Catalog - TI's standard catalog product

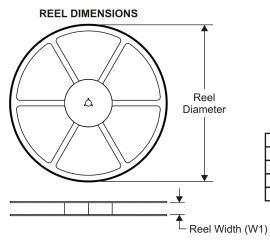
• Military - QML certified for Military and Defense Applications

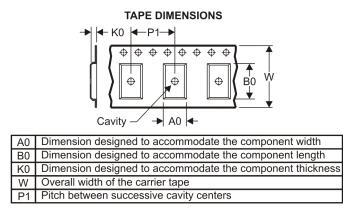
PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



4	All dimensions are nominal												
	Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ſ	SN74AS832BDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

29-Jul-2009



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AS832BDWR	SOIC	DW	20	2000	346.0	346.0	41.0

J (R-GDIP-T**) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20



LEADLESS CERAMIC CHIP CARRIER

FK (S-CQCC-N**) 28 TERMINAL SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. This package can be hermetically sealed with a metal lid.

D. Falls within JEDEC MS-004



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-013 variation AC.



LAND PATTERN DATA



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
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