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- Controlled Baseline
  One Assembly/Test Site, One Fabrication Site
- Extended Temperature Performance of -40°C to 105°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree<sup>†</sup>
- 2-V to 5.5-V V<sub>CC</sub> Operation

<sup>†</sup> Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

#### description/ordering information

Typical V<sub>OLP</sub> (Output Ground Bounce)
 <0.8 V at V<sub>CC</sub>= 3.3 V, T<sub>A</sub> = 25°C

- Typical V<sub>OHV</sub> (Output V<sub>OH</sub> Undershoot)
  >2.3 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Supports Mixed-Mode Voltage Operation on All Ports
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation

PW PACKAGE (TOP VIEW)							
1A 1B 2A 2B 2C 2Y GND	2 3 4	14 13 12 11 10 9 8	] V <sub>CC</sub> ] 1C ] 1Y ] 3C ] 3B ] 3A ] 3Y				

This triple 3-input positive-AND gate is designed for 2-V to 5.5-V  $V_{CC}$  operation.

The SN74LV11A performs the Boolean function  $Y = A \bullet B \bullet C$  or  $Y = \overline{\overline{A} + \overline{B} + \overline{C}}$  in positive logic.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### **ORDERING INFORMATION**

TA	PACK	AGE‡	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 105°C	TSSOP – PW	Tape and reel	SN74LV11ATPWREP	LV11AEP

<sup>‡</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each gate)								
	INPUTS	OUTPUT						
Α	В	С	Y					
Н	Н	Н	Н					
L	Х	Х	L					
Х	L	Х	L					
Х	Х	L	L					



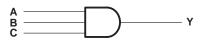
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#### logic diagram, each gate (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub>	–0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	. –0.5 V to 7 V
Output voltage range applied in high or low state, VO (see Notes 1 and 2)0.5 V	/ to V <sub>CC</sub> + 0.5 V
Voltage range applied to any output in the power-off state, VO (see Note 1)	–0.5 V to 7 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$	±25 mA
Continuous current through V <sub>CC</sub> or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3)	113°C/W
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

2. This value is limited to 5.5 V maximum.

3. The package thermal impedance is calculated in accordance with JESD 51-7.



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### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		2	5.5	V
		$V_{CC} = 2 V$	1.5		
	1 Pade Jacob Served configure	$V_{CC}$ = 2.3 V to 2.7 V	V <sub>CC</sub> ×0.7		
VIH	High-level input voltage	$V_{CC} = 3 \vee to 3.6 \vee$	V <sub>CC</sub> ×0.7		V
		$V_{CC}$ = 4.5 V to 5.5 V	V <sub>CC</sub> ×0.7		
		$V_{CC} = 2 V$		0.5	
.,		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		V <sub>CC</sub> ×0.3	.,
VIL	Low-level input voltage	$V_{CC} = 3 \vee to 3.6 \vee$		V <sub>CC</sub> ×0.3	V
		$V_{CC}$ = 4.5 V to 5.5 V		V <sub>CC</sub> ×0.3	
VI	Input voltage		0	5.5	V
VO	Output voltage		0	VCC	V
		V <sub>CC</sub> = 2 V		-50	μA
	1 Park Jacob and an annual	$V_{CC}$ = 2.3 V to 2.7 V	-2		
юн	High-level output current	$V_{CC} = 3 \vee to 3.6 \vee$		-6	
		$V_{CC}$ = 4.5 V to 5.5 V			
		V <sub>CC</sub> = 2 V		50	μA
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	2		
IOL	Low-level output current	V <sub>CC</sub> = 3 V to 3.6 V			mA
		$V_{CC}$ = 4.5 V to 5.5 V		12	
		V <sub>CC</sub> = 2.3 V to 2.7 V		200	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3 V \text{ to } 3.6 V$	100		ns/V
		V <sub>CC</sub> = 4.5 V to 5.5 V		20	
Тд	Operating free-air temperature		-40	105	°C

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
	I <sub>OH</sub> = -50 μA	2 V to 5.5 V	V <sub>CC</sub> -0.1			
	$I_{OH} = -2 \text{ mA}$	2.3 V	2			
Vон	$I_{OH} = -6 \text{ mA}$	3 V	2.48			V
	$I_{OH} = -12 \text{ mA}$	4.5 V	3.8			
	I <sub>OL</sub> = 50 μA	2 V to 5.5 V			0.1	
	I <sub>OL</sub> = 2 mA	2.3 V			0.4 V	
VOL	I <sub>OL</sub> = 6 mA	3 V			0.44	V
	I <sub>OL</sub> = 12 mA	4.5 V			0.55	
lj	$V_{I} = 5.5 V \text{ or GND}$	0 to 5.5 V			±1	μΑ
ICC	$V_{I} = V_{CC} \text{ or } GND,  I_{O} = 0$	5.5 V			20	μΑ
loff	$V_{I}$ or $V_{O} = 0$ to 5.5 V	0 V			5	μΑ
Ci	$V_I = V_{CC}$ or GND	3.3 V		1.9		pF



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switching characteristics over recommended operating free-air temperature range,  $V_{CC}$  = 2.5 V  $\pm$  0.2 V (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	TO LOAD T <sub>A</sub> = 25°		λ = 25°C	;				
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN TYP MAX		MIN	MAX	UNIT	
<sup>t</sup> pd	A, B, or C	Y	CL = 50 pF		9.9	17.5	1	21	ns

# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	TO LOAD T <sub>A</sub> = 25°C		MIN	MAX	UNIT		
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN TYP MAX		WIIN	WAX	UNIT	
<sup>t</sup> pd	A, B, or C	Y	C <sub>L</sub> = 50 pF		7.2	12.3	1	14	ns

# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	то	TO LOAD		T <sub>A</sub> = 25°C				
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN TYP MAX		MIN	MAX	UNIT	
<sup>t</sup> pd	A, B, or C	Y	C <sub>L</sub> = 50 pF		5.4	7.9	1	9	ns

## noise characteristics, $V_{CC}$ = 3.3 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

	PARAMETER	MIN	TYP	MAX	UNIT
V <sub>OL(P)</sub>	Quiet output, maximum dynamic V <sub>OL</sub>		0.2	0.8	V
VOL(V)	Quiet output, minimum dynamic V <sub>OL</sub>		0	-0.8	V
VOH(V)	Quiet output, minimum dynamic V <sub>OH</sub>		3.2		V
VIH(D)	High-level dynamic input voltage	2.31			V
V <sub>IL(D)</sub>	Low-level dynamic input voltage			0.99	V

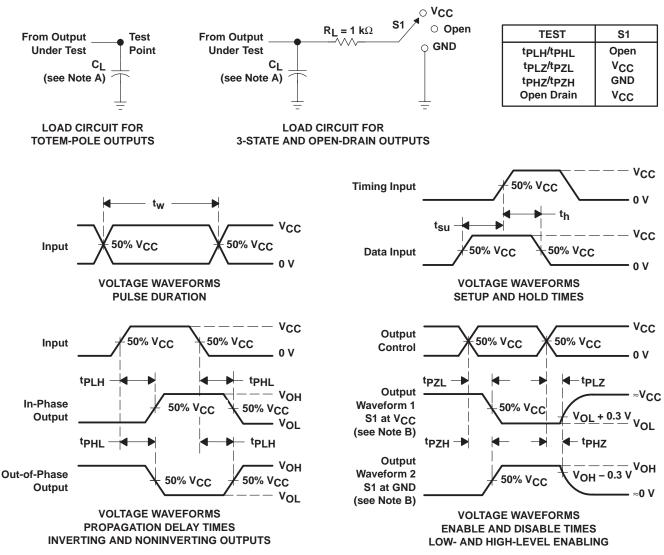
NOTE 5: Characteristics are for surface-mount packages only.

## operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	PARAMETER TEST CONDITIONS		V <sub>CC</sub>	TYP	UNIT
<u> </u>	Down dissipation consoltance	C. 50 mF	£ 10 MU-	3.3 V	13.9	~ <b>Г</b>
Cpd	Power dissipation capacitance	C <sub>L</sub> = 50 pF,	f = 10 MHz	5 V	15.4	pF



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PARAMETER MEASUREMENT INFORMATION

NOTES: A. Cl includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
  Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>f</sub>  $\leq$  3 ns, t<sub>f</sub>  $\leq$  3 ns.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F.  $t_{P7I}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G. tPHL and tPLH are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



### PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins P	ackage Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LV11ATPWREP	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04692-01XE	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. **TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74LV11A-EP :

- Catalog: SN74LV11A
- Automotive: SN74LV11A-Q1

NOTE: Qualified Version Definitions:

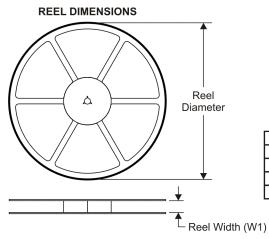
- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects

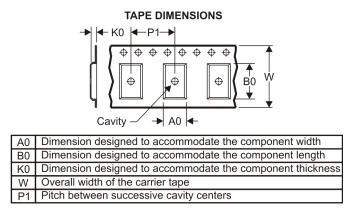
# PACKAGE MATERIALS INFORMATION

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### TAPE AND REEL INFORMATION





### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



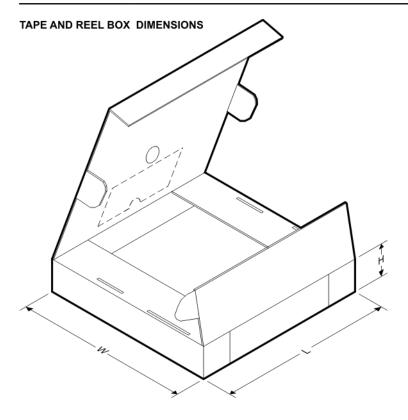
*All dimensions are nominal												
Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV11ATPWREP	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

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# PACKAGE MATERIALS INFORMATION

30-Jul-2010



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV11ATPWREP	TSSOP	PW	14	2000	346.0	346.0	29.0

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



A. An integration of the information o

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153



## LAND PATTERN DATA



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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