

FEATURES

- Available in the Texas Instruments NanoFree[™] Package
- Low Static-Power Consumption $(I_{CC} = 0.9 \ \mu A \ Max)$
- Low Dynamic-Power Consumption $(C_{pd} = 5 \text{ pF Typ at } 3.3 \text{ V})$
- Low Input Capacitance (C₁ = 1.5 pF)
- Low Noise Overshoot and Undershoot <10% of V_{CC}
- Input-Disable Feature Allows Floating Input Conditions
- I_{off} Supports Partial-Power-Down Mode Operation
- **Includes Schmitt-Trigger Inputs**

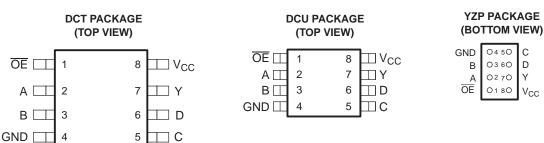
- Wide Operating V_{CC} Range of 0.8 V to 3.6 V **Optimized for 3.3-V Operation**
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- t_{pd} = 7.4 ns Max at 3.3 V •
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

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V_{CC}



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static- and dynamic-power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity (see Figures 1 and 2).

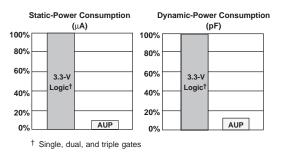


Figure 1. AUP - The Lowest-Power Family

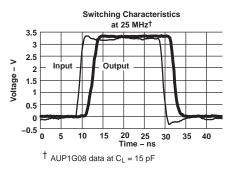


Figure 2. Excellent Signal Integrity

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SCES594C-JULY 2004-REVISED DECEMBER 2007

DESCRIPTION/ORDERING INFORMATION

The SN74AUP1G99 features configurable multiple functions with a 3-state output. This device has the input-disable feature, which allows floating input signals. The inputs and output are disabled when the output-enable (\overline{OE}) input is high. When \overline{OE} is low, the output state is determined by 16 patterns of 4-bit input. The user can choose the logic functions, such as MUX, AND, OR, NAND, NOR, XOR, XNOR, inverter, and buffer. All inputs can be connected to V_{CC} or GND.

This device functions as an independent gate with Schmitt-trigger inputs, which allows for slow input transition and better switching noise immunity at the input.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

NanoStar[™] and NanoFree[™] package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

T _A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽³⁾
−40°C to 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Tape and reel	SN74AUP1G99YZPR	HY_
	SSOP – DCT	Tape and reel	SN74AUP1G99DCTR	H99
	VSSOP – DCU	Tape and reel	SN74AUP1G99DCUR	H99_

ORDERING INFORMATION

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

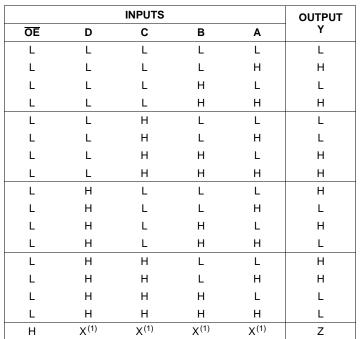
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

(3) DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site. DCU: The actual top-side marking has one additional character that designates the assembly/test site. YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

2

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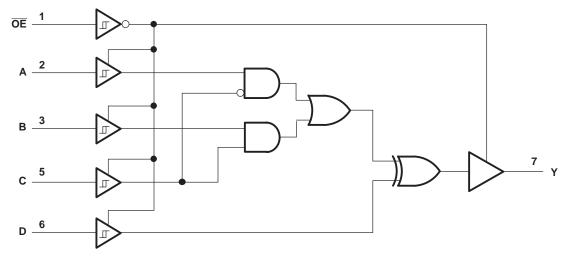
SCES594C-JULY 2004-REVISED DECEMBER 2007



FUNCTION TABLE

(1) Floating inputs allowed.

LOGIC DIAGRAM (POSITIVE LOGIC)



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TRUMENTS

SCES594C-JULY 2004-REVISED DECEMBER 2007



FUNCTION SELECTION TABLE

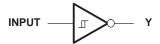
PRIMARY FUNCTION	COMPLEMENTARY FUNCTION	PAGE
3-state buffer		4
3-state inverter		4
3-state 2-to-1 data selector MUX		5
3-state 2-to-1 data selector MUX, inverted out		5
3-state 2-input AND	3-state 2-input NOR, both inputs inverted	5
3-state 2-input AND, 1 input inverted	3-state 2-input NOR, 1 input inverted	5
3-state 2-input AND, both inputs inverted	3-state 2-input NOR	5
3-state 2-input NAND	3-state 2-input OR, both inputs inverted	6
3-state 2-input NAND, 1 input inverted	3-state 2-input OR, 1 input inverted	6
3-state 2-input NAND, both inputs inverted	3-state 2-input OR	6
3-state 2-input XOR		6
3-state 2-input XNOR	3-state 2-input XOR, 1 input inverted	7

3-STATE BUFFER FUNCTIONS AVAILABLE



FUNCTION	OE	Α	В	С	D		
		Input	Х	L	L		
3-state buffer	L	Х	Input	Н	L		
		L	Н	Input	L		
		Н	L	Input	н		
		Н	Х	L	Input		
		Х	L	Н	Input		
		L	L	Х	Input		

3-STATE INVERTER FUNCTIONS AVAILABLE



FUNCTION	ŌĒ	Α	В	С	D
		Input	Х	L	Н
		Х	Input	Н	Н
		L	н	Input	Н
3-state inverter	L	Н	L	Input	L
		Н	Х	L	Input
		Х	н	Н	Input
		Н	Н	Х	Input

4

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NO. OF INPUTS

2

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SN74AUP1G99 LOW-POWER ULTRA-CONFIGURABLE MULTIPLE-FUNCTION GATE WITH 3-STATE OUTPUTS

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Ā/B

Input 1

Input 2

SCES594C-JULY 2004-REVISED DECEMBER 2007

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Input 1

Input 2

С

Input 2

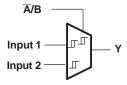
Input 1

D

L

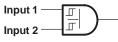
L

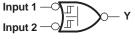
3-STATE MUX FUNCTIONS AVAILABLE



	-				
FUNCTION	OE	Α	В	С	D
3-state 2-to-1, data selector MUX		Input 1	Input 2	Input 1 or Input 2	L
3-state 2-to-1, data selector MUX		Input 2	Input 1	Input 2 or Input 1	L
3-state 2-to-1, data selector MUX, inverted out	L	Input 1	Input 2	Input 1 or Input 2	Н
3-state 2-to-1, data selector MUX, inverted out		Input 2	Input 1	Input 2 or Input 1	Н

3-STATE AND/NOR FUNCTIONS AVAILABLE





Input 2	
AND/NAND FUNCTION	OR/NOR FUNCTION

3-state AND

3-state AND

nput 1 — O	≞୲∕∕∨
nput 2 — 🗸	

OE

L

Α

L

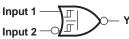
L

nput 2 —	
JNCTION	OR/I

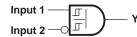
AND	3-state NOR, both	inputs inverted
Input 1 —O	<u></u> т	Input 1
Input 2		Input 2

3-state NOR, both inputs inverted

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NO. OF INPUTS	AND/NAND FUNCTION	OR/NOR FUNCTION	OE	Α	В	С	D
2	3-state AND, with A inverted	3-state NOR, with B inverted		Input 2	L	Input 1	L
2	3-state AND, with A inverted	3-state NOR, with B inverted		Н	Input 1	Input 2	Н





NO. OF INPUTS	AND/NAND FUNCTION	OR/NOR FUNCTION	OE	Α	В	С	D
2	3-state AND, with B inverted	3-state NOR, with A inverted		Input 1	L	Input 2	L
2	3-state AND, with B inverted	3-state NOR, with A inverted		Н	Input 2	Input 1	Н



NO. OF INPUTS	AND/NAND FUNCTION	OR/NOR FUNCTION	ŌĒ	Α	В	С	D
2	3-state AND, both inverted inputs	3-state NOR		Input 1	Н	Input 2	Н
2	3-state AND, both inverted inputs	3-state NOR	L	Input 2	Н	Input 1	Н



SCES594C-JULY 2004-REVISED DECEMBER 2007

3-STATE NAND/OR FUNCTIONS AVAILABLE

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I	nput 1	
I	Input 2	

NO. OF INPUTS	AND/NAND FUNCTION	OR/NOR FUNCTION	ŌĒ	Α	В	С	D
2	3-state NAND	3-state OR, with both inputs inverted	1	L	Input 1	Input 2	Н
2	3-state NAND	3-state OR, with both inputs inverted	L	L	Input 2	Input 1	Н



— Y

NO. OF INPUTS	AND/NAND FUNCTION	ND FUNCTION OR/NOR FUNCTION		Α	В	С	D
2	3-state NAND, with A inverted	3-state OR, with B inverted		Input 2	L	Input 1	Н
2	3-state NAND, with A inverted	3-state OR, with B inverted	L	Н	Input 1	Input 2	L

NO. OF INPUTS	AND/NAND FUNCTION	AND/NAND FUNCTION OR/NOR FUNCTION		Α	В	С	D
2	3-state NAND, with B inverted	3-state OR, with A inverted		Input 1	L	Input 2	Н
2	3-state NAND, with B inverted	3-state OR, with A inverted		Н	Input 2	Input 1	L



NO. OF INPUTS	AND/NAND FUNCTION	OR/NOR FUNCTION	OE	Α	В	С	D
2	3-state NAND, with both inputs inverted	3-state OR	1	Input 1	Н	Input 2	L
2	3-state NAND, with both inputs inverted	3-state OR	L	Input 2	Н	Input 1	L

3-STATE XOR/XNOR FUNCTIONS AVAILABLE

FUNCTION	OE	Α	В	С	D	
			Input 1	Х	L	Input 2
		Input 2	Х	L	Input 1	
	L	Х	Input 1	Н	Input 2	
3-state XOR		Х	Input 2	Н	Input 1	
		L	Н	Input 1	Input 2	
		L	Н	Input 2	Input 1	

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SCES594C-JULY 2004-REVISED DECEMBER 2007

Input 1 Π Υ Input 2 FUNCTION OE в С D Α 3-state XOR, with A inverted L Н L Input 1 Input 2 Input 1 П Υ П Input 2 FUNCTION OE С D Α в Input 2 3-state XOR, with B inverted н L L Input 1

3-STATE XOR/XNOR FUNCTIONS AVAILABLE (continued)



FUNCTION	ŌĒ	Α	В	С	D
3-state XNOR	L -	Н	L	Input 1	Input 2
3-state XNOR		Н	L	Input 2	Input 1

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	4.6	V
VI	Input voltage range ⁽²⁾		-0.5	4.6	V
Vo	Voltage range applied to any output in the high-in	npedance or power-off state ⁽²⁾	-0.5	4.6	V
Vo	Output voltage range in the high or low state ⁽²⁾		-0.5	/ _{CC} + 0.5	V
I _{IK}	Input clamp current	V ₁ < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
I _O	Continuous output current			±20	mA
	Continuous current through V _{CC} or GND			±50	mA
		DCT package		220	
θ_{JA}	Package thermal impedance ⁽³⁾	DCU package		227	°C/W
		YZP package		102	
T _{stg}	Storage temperature range	-65	150	°C	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The package thermal impedance is calculated in accordance with JESD 51-7.





Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT	
V _{CC}	Supply voltage		0.8	3.6	V	
VI	Input voltage		0	3.6	V	
V		Active state	0	V _{CC}	V	
Vo	Output voltage	3-state	0	3.6	v	
		$V_{CC} = 0.8 V$		-20	μΑ	
		V _{CC} = 1.1 V		-1.1		
I _{OH}	Lich loud output ourrent	V _{CC} = 1.4 V		-1.7		
	High-level output current	V _{CC} = 1.65 V		-1.9	mA	
		V_{CC} = 2.3 V		-3.1		
		$V_{CC} = 3 V$		-4		
		V _{CC} = 0.8 V		20	μΑ	
		V _{CC} = 1.1 V		1.1		
	Low lovel output ourrent	$V_{CC} = 1.4 V$		1.7		
I _{OL}	Low-level output current	V _{CC} = 1.65 V		1.9	mA	
		V_{CC} = 2.3 V		3.1		
		V _{CC} = 3 V		4		
Δt/Δv	Input transition rise or fall rate	$V_{CC} = 0.8 V \text{ to } 3.6 V$		200	ns/V	
T _A	Operating free-air temperature		-40	85	°C	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

8

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SCES594C-JULY 2004-REVISED DECEMBER 2007

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc}	т,	₄ = 25°C	T _A = −40° to 85°C		
			MIN	TYP MAX	MIN	MAX	
		0.8 V	0.3	0.6	0.3	0.6	
. ,		1.1 V	0.53	0.9	0.53	0.9	1
V _{T+} Positive-going		1.4 V	0.74	1.11	0.74	1.11	v
input threshold		1.65 V	0.91	1.29	0.91	1.29	V
voltage		2.3 V	1.37	1.77	1.37	1.77	
		3 V	1.88	2.29	1.88	2.29	
		0.8 V	0.1	0.6	0.1	0.6	
N7		1.1 V	0.26	0.65	0.26	0.65	
V _{T-} Negative-going		1.4 V	0.39	0.75	0.39	0.75	v
input threshold		1.65 V	0.47	0.84	0.47	0.84	v
voltage		2.3 V	0.69	1.04	0.69	1.04	
		3 V	0.88	1.24	0.88	1.24	
		0.8 V	0.07	0.5	0.07	0.5	
		1.1 V	0.08	0.46	0.08	0.46	
ΔV _T		1.4 V	0.18	0.56	0.18	0.56	
Hysteresis (V _{T+} – V _{T–})		1.65 V	0.27	0.66	0.27	0.66	V
		2.3 V	0.53	0.92	0.53	0.92	
		3 V	0.79	1.31	0.79	1.31	
	I _{OH} = -20 μA	0.8 V to 3.6 V	V _{CC} – 0.1		V _{CC} – 0.1		
	$I_{OH} = -1.1 \text{ mA}$	1.1 V	$0.75 \times V_{CC}$		$0.7 imes V_{CC}$		
	I _{OH} = -1.7 mA	1.4 V	1.11		1.03		
	I _{OH} = -1.9 mA	1.65 V	1.32		1.3		v
V _{OH}	I _{OH} = -2.3 mA	2.3 V	2.05		1.97		v
	I _{OH} = -3.1 mA	2.3 V	1.9		1.85		
	I _{OH} = -2.7 mA	3 V	2.72		2.67		
	$I_{OH} = -4 \text{ mA}$	3 V	2.6		2.55		
	I _{OL} = 20 μA	0.8 V to 3.6 V		0.1		0.1	
	I _{OL} = 1.1 mA	1.1 V		$0.3 \times V_{\text{CC}}$	0	$.3 \times V_{CC}$	
	I _{OL} = 1.7 mA	1.4 V		0.31		0.37	
N/	I _{OL} = 1.9 mA	1.65 V		0.31		0.35	v
V _{OL}	I _{OL} = 2.3 mA	2.3 V		0.31		0.33	v
	I _{OL} = 3.1 mA	2.3 V		0.44		0.45	
	I _{OL} = 2.7 mA	3 V		0.31		0.33	
	I _{OL} = 4 mA	51		0.44		0.45	
II All inputs	$V_1 = GND$ to 3.6 V	0 V to 3.6 V		0.1		0.5	μA
off	$V_1 \text{ or } V_0 = 0 \text{ V to } 3.6 \text{ V}$	0 V		0.2		0.6	μA
∆l _{off}	$V_1 \text{ or } V_0 = 0 \text{ V to } 3.6 \text{ V}$	0 V to 0.2 V		0.2		0.6	μA
I _{OZ}	$V_{O} = V_{CC}$ or GND	3.6 V		0.1		0.5	μA
lcc	$\frac{V_{I} = \text{GND or } (V_{CC} \text{ to } 3.6 \text{ V}),}{\text{OE} = \text{GND, } I_{O} = 0}$	0.8 V to 3.6 V		0.5		0.9	μA



SCES594C-JULY 2004-REVISED DECEMBER 2007

Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{cc}	т,	T _A = 25°C			C	UNIT
				MIN	TYP	MAX	MIN	MAX	
	Data inputs	$V_{I} = V_{CC} - 0.6 V^{(1)}_{,(1)} I_{O} = 0$	3.3 V			40		50	μA
ΔI_{CC}				110			120		
	All inputs	$V_I = GND$ to 3.6 V, $\overline{OE} = V_{CC}^{(2)}$	0.8 V to 3.6 V		0				nA
<u> </u>			0 V		1.5				~ Г
CI		$V_{I} = V_{CC}$ or GND	3.6 V		1.5				pF
Co		$V_{O} = V_{CC}$ or GND	3.6 V		3				pF

Switching Characteristics

over recommended operating free-air temperature range, C_L = 5 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM	TO (OUTPUT)	V _{cc}	T,	λ = 25°C		T _A = to 85		UNIT
	(INPUT)	(001201)		MIN	TYP	MAX	MIN	MAX	
			0.8 V		32				
			1.2 V ± 0.1 V	0.5	9.9	20.1	0.5	26.6	1
	A, B, C, or D	Y	1.5 V ± 0.1 V	1.4	6.6	11.9	0.5	16.8	
t _{pd}			1.8 V ± 0.15 V	1.8	5.3	8.9	1	13	ns
			2.5 V ± 0.2 V	2.1	3.9	5.8	1.3	8.9	
			3.3 V ± 0.3 V	1.9	3.3	4.8	1.2	7.4	-
	ŌE	Y	0.8 V		35				
			1.2 V ± 0.1 V	0.6	11.1	21.7	0.5	25.2	ns
			1.5 V ± 0.1 V	2.3	7.4	12.6	1.4	16.4	
t _{en}			1.8 V ± 0.15 V	2	5.7	9.4	1.1	12.8	
			2.5 V ± 0.2 V	2.1	4.1	6.2	1.2	8.5	
			3.3 V ± 0.3 V	1.9	3.4	5	1.1	6.7	
			0.8 V		9.8				
			1.2 V ± 0.1 V	1.4	4.5	7.7	1.5	8.2	
		V	1.5 V ± 0.1 V	1.7	3.2	4.8	1.7	6	
t _{dis}	ŌĒ	Y	1.8 V ± 0.15 V	1.5	3	4.7	1.3	6.1	ns
			2.5 V ± 0.2 V	0.9	1.9	3	0.7	4.2	
			3.3 V ± 0.3 V	0.8	2.5	4.4	0.7	4.5	



SCES594C-JULY 2004-REVISED DECEMBER 2007

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 10 \text{ pF}$ (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER		TO (OUTPUT)	v _{cc}	т,	T _A = 25°C			T _A = −40°C to 85°C	
	(INPUT)	(001901)	(001F01)		TYP	MAX	MIN	MAX	
			0.8 V		36				
			1.2 V ± 0.1 V	0.4	10.7	21.1	0.7	29.8	
		Y	1.5 V ± 0.1 V	2	7.2	12.6	1.1	18.5	
t _{pd}	A, B, C, or D	ř	1.8 V ± 0.15 V	2.3	5.8	9.5	1.5	14.5	ns
			2.5 V ± 0.2 V	2.5	4.4	6.3	1.7	10.5	
			3.3 V ± 0.3 V	2.3	3.7	5.2	1.5	8.4	
			0.8 V		0				ns
	OE	Y	1.2 V ± 0.1 V	1.4	12.1	22.8	0.8	29.3	
			1.5 V ± 0.1 V	2.8	8	13.3	2	18.7	
t _{en}			1.8 V ± 0.15 V	2.5	6.2	10	1.6	14.8	
			2.5 V ± 0.2 V	2.5	4.5	6.7	1.6	9.9	
			3.3 V ± 0.3 V	2.3	3.8	5.4	1.5	8.2	
			0.8 V		0				
			1.2 V ± 0.1 V	2	5.6	9.3	2	10	
	ŌĒ	V	1.5 V ± 0.1 V	2.5	4.1	5.8	2.4	7.6	ns
t _{dis}		Y	1.8 V ± 0.15 V	2.9	4.2	5.7	2.7	7.9	
			2.5 V ± 0.2 V	1.1	2.7	4.4	1.1	5.5	
			3.3 V ± 0.3 V	1.9	3.5	5.2	1.9	5.8	



SCES594C-JULY 2004-REVISED DECEMBER 2007

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 15 \text{ pF}$ (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{cc}	т,	λ = 25°C		T _A = −40°C to 85°C		UNIT
	(INFOT)	(001901)		MIN	TYP	MAX	MIN	MAX	
			0.8 V		38				
			1.2 V ± 0.1 V	0.9	11.4	22	0.5	30.8	
		Y	1.5 V ± 0.1 V	2.5	7.8	13.2	1.6	19.2	20
t _{pd}	A, B, C, or D	ř	1.8 V ± 0.15 V	2.7	6.3	10	1.9	15.1	ns
			2.5 V ± 0.2 V	2.8	4.7	6.6	2	10.8	
			3.3 V ± 0.3 V	2.6	4	5.5	1.8	8.8	
	ŌĒ		0.8 V		44				- ns
		Y	1.2 V ± 0.1 V	1.8	13	24.2	1.3	30.6	
			1.5 V ± 0.1 V	3.2	8.6	14.1	2.4	19.5	
t _{en}			1.8 V ± 0.15 V	2.9	6.7	10.6	2	15.4	
			2.5 V ± 0.2 V	2.8	4.9	7	1.9	10.3	
			3.3 V ± 0.3 V	2.6	4.1	5.7	1.8	8.6	
			0.8 V		13				
			1.2 V ± 0.1 V	2.7	6.3	9.9	2.8	10.7	
	OE	V	1.5 ± 0.1 V	3.2	4.6	6.1	3.1	8	ns
t _{dis}	OE	Y	1.8 V ± 0.15 V	3.2	4.8	6.6	3	8.8	
			2.5 V ± 0.2 V	2.2	3.4	4.7	2	6	
			3.3 V ± 0.3 V	2.4	4.4	6.5	2.3	7.2	



SCES594C-JULY 2004-REVISED DECEMBER 2007

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM	TO	V _{cc}	T,	_A - 25°C		T _A = −40°C to 85°C		UNIT
	(INPUT)	(OUTPUT)		MIN	TYP	MAX	MIN	MAX	
			0.8 V		48				
			1.2 V ± 0.1 V	3.1	14	24.9	2.6	36.1	
		Y	1.5 V ± 0.1 V	4.2	9.6	15.1	3.3	23.1	20
t _{pd}	A, B, C, or D	ř	1.8 V ± 0.15 V	4.1	7.9	11.7	3.3	18	ns
			2.5 V ± 0.2 V	4.1	5.9	7.9	3.1	12.7	
			3.3 V ± 0.3 V	3.7	5.1	6.7	2.8	10.4	
	ŌE		0.8 V		50				ns
		Y	1.2 V ± 0.1 V	4.4	16	27.6	3.9	36.8	
			1.5 V ± 0.1 V	5.3	10.7	16.2	4.3	23.6	
t _{en}			1.8 V ± 0.15 V	4.6	8.5	12.4	3.6	18.6	
			2.5 V ± 0.2 V	4.2	6.3	8.5	3.2	12.6	
			3.3 V ± 0.3 V	3.8	5.4	7.1	2.9	10.2	
			0.8 V		19				
			1.2 V ± 0.1 V	6	10.1	14.2	6	14.6	
	ŌĒ	V	1.5 V ± 0.1 V	5.1	7.4	10.6	5	10.1	ns
t _{dis}	UE	Y	1.8 V ± 0.15 V	5.5	8.6	11.6	5.5	12.1	
			2.5 V ± 0.2 V	3.3	5.9	8.3	3.3	8.9	
			3.3 V ± 0.3 V	6	8.7	10.9	5.9	11.8	

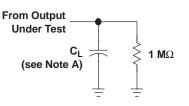
Operating Characteristics

 $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	V _{cc}	TYP	UNIT	
				0.8 V	4	
				1.2 ± 0.1 V	4	
		Outputs enabled		1.5 ± 0.1 V	4	
				1.8 V ± 0.15 V	4	
				2.5 V ± 0.2 V	5	
C	Dower dissinction conscitones		f = 10 MHz	3.3 V ± 0.3 V	5	- F
C _{pd}	Power dissipation capacitance			0.8 V	0	pF
				1.2 ± 0.1 V	0	
		Outpute disabled		1.5 ± 0.1 V	0	
		Outputs disabled		1.8 V ± 0.15 V	0	
				2.5 V ± 0.2 V	0	
				3.3 V ± 0.3 V	0	

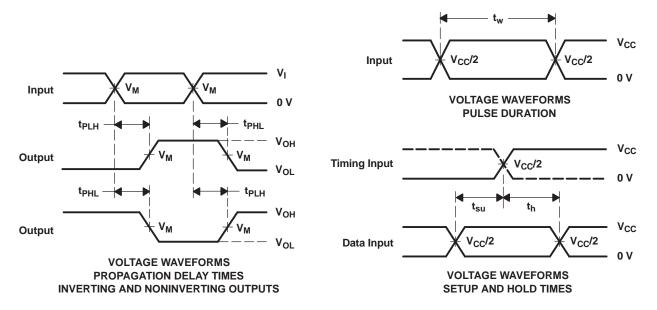


PARAMETER MEASUREMENT INFORMATION (Propagation Delays, Setup and Hold Times, and Pulse Width)



$V_{CC} = 1.2 V$ $V_{CC} = 1.5 V$ V_{CC} = 1.8 V $V_{CC} = 2.5 V$ V_{CC} = 3.3 V $V_{CC} = 0.8 V$ $\pm\,0.1$ V $\pm\,0.1$ V ± 0.15 V ± 0.2 V ± 0.3 V \mathbf{C}_{L} 5, 10, 15, 30 pF VM V_{CC}/2 V_{CC}/2 V_{CC}/2 V_{CC}/2 V_{CC}/2 V_{CC}/2 V_{CC} ٧ı V_{CC} V_{CC} V_{CC} v_{cc} v_{cc}

LOAD CIRCUIT



NOTES: A. C_L includes probe and jig capacitance.

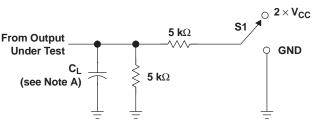
- B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z₀ = 50 Ω , for propagation delays t_{f}/t_{f} = 3 ns, for setup and hold times and pulse width t_{f}/t_{f} = 1.2 ns.
- C. The outputs are measured one at a time, with one transition per measurement.
- D. t_{PLH} and t_{PHL} are the same as t_{pd} .
- E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms



SCES594C-JULY 2004-REVISED DECEMBER 2007

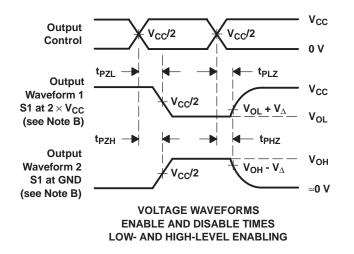
PARAMETER MEASUREMENT INFORMATION (Enable and Disable Times)



TEST	S1
t _{PLZ} /t _{PZL} t _{PHZ} /t _{PZH}	$2 \times V_{CC}$ GND

LOAD CIRCUIT

	V _{CC} = 0.8 V	V _{CC} = 1.2 V ± 0.1 V	V _{CC} = 1.5 V ± 0.1 V	V _{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V \pm 0.2 V	V _{CC} = 3.3 V ± 0.3 V
CL	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V _M	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2
V _I	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}
V _Δ	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_r/t_f = 3 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74AUP1G99DCTR	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G99DCTRE4	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G99DCTRG4	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G99DCTT	ACTIVE	SM8	DCT	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G99DCTTE4	ACTIVE	SM8	DCT	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G99DCTTG4	ACTIVE	SM8	DCT	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G99DCUR	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G99DCURE4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G99DCURG4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G99DCUT	ACTIVE	US8	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G99DCUTE4	ACTIVE	US8	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G99DCUTG4	ACTIVE	US8	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G99YZPR	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G99DCUR	US8	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUP1G99YZPR	DSBGA	YZP	8	3000	180.0	8.4	1.02	2.02	0.63	4.0	8.0	Q1

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

6-May-2011



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G99DCUR	US8	DCU	8	3000	202.0	201.0	28.0
SN74AUP1G99YZPR	DSBGA	YZP	8	3000	220.0	220.0	34.0

MECHANICAL DATA

MPDS049B - MAY 1999 - REVISED OCTOBER 2002

DCT (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion

D. Falls within JEDEC MO-187 variation DA.



DCT (R-PDSO-G8) PLASTIC SMALL OUTLINE Example Board Layout Example Stencil Design (Note C,E) (Note D) - 6x0,65 - 6x0,65 8x0,25-8x1,55 3,40 3,40 Non Solder Mask Defined Pad Example Pad Geometry -0,30 (Note C) 1,60 Example -0,07 Non-solder Mask Opening All Around (Note E) 4212201/A 10/11

NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



DCU (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.

D. Falls within JEDEC MO-187 variation CA.



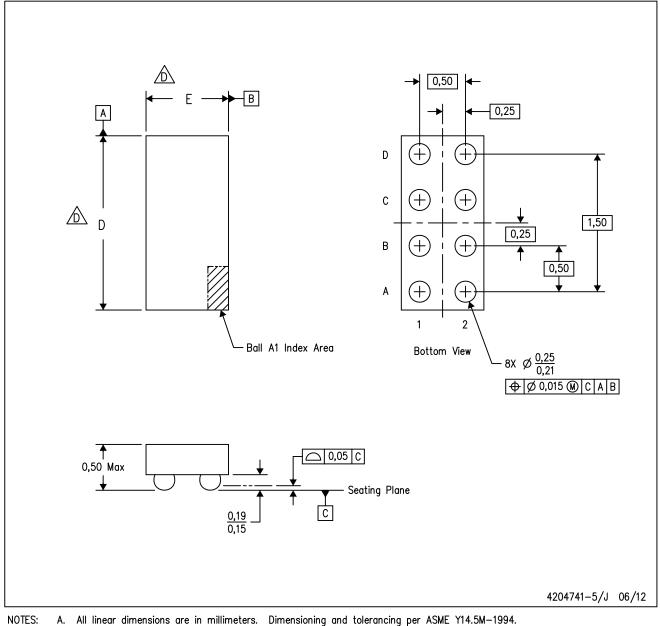


- NOTES: A. All linear dimensions are in millimeters. В. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



YZP (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.
- The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
 E. This package is a Pb-free solder ball design. Refer to the 8 YEP package (drawing 4204725) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.



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