# OBSOLETE - No Longer Available SN5486, SN54LS86A, SN54S86 SN7486, SN74LS86A, SN74S86 **QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES**

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- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

	TYPICAL AVERAGE	TYPICAL
TYPE	PROPAGATION	TOTAL POWER
	DELAY TIME	DISSIPATION
<b>'86</b>	14 ns	150 mW
'LS86A	10 ns	30.5 mW
'S86	7 ns	250 mW

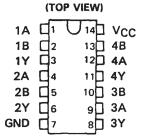
#### description

These devices contain four independent 2-input Exclusive-OR gates. They perform the Boolean functions  $Y = A \oplus B = \overline{A}B + A\overline{B}$  in positive logic.

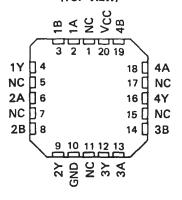
A common application is as a true/complement element. If one of the inputs is low, the other input will be reproduced in true form at the output. If one of the inputs is high, the signal on the other input will be reproduced inverted at the output.

The SN5486, 54LS86A, and the SN54S86 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN7486, SN74LS86A, and the SN74S86 are characterized for operation from 0°C to 70°C.

#### SN5486, SN54LS86A, SN54S86 . . . J OR W PACKAGE SN7486 . . . N PACKAGE SN74LS86A, SN74S86 . . . D OR N PACKAGE



#### SN54LS86A, SN54S86 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

#### exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



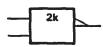
These are five equivalent Exclusive-OR symbols valid for an '86 or 'LS86A gate in positive logic; negation may be shown at any two ports.

# LOGIC IDENTITY ELEMENT



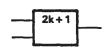
The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

#### **EVEN-PARITY**



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

#### **ODD-PARITY ELEMENT**



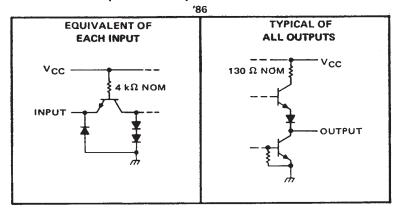
The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

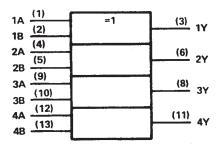


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#### schematics of inputs and outputs



#### logic symbol†



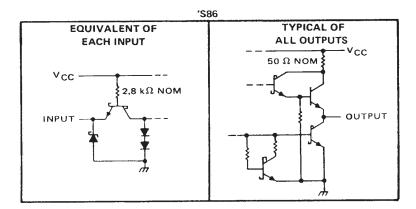
<sup>†</sup>This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, N, and W packages.

# LS86A EQUIVALENT OF EACH INPUT TYPICAL OF ALL OUTPUTS -Vcc 150 Ω vcc -NOM 12.5 kΩ NOM } INPUT -OUTPUT

#### **FUNCTION TABLE**

INP	UTS	OUTPUT
Α	В	Υ
L	L	L
L	Н	н
Н	L	н
н	н	[

H = high level, L = low level



# OBSOLETE - No Longer Available SN5486, SN54LS86A, SN54S86 SN7486, SN74LS86A, SN74S86 **QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES**

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)				. ,	 ٠						7 V
Input voltage											
Operating free-air temperature range: SN5486											-55°C to 125°C
SN7486											. 0°C to 70°C
Storage temperature range											-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

#### recommended operating conditions

		SN5486	5		SN7486	6	UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	CIVIT
Supply voltage, V <sub>CC</sub>	4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH			-800			-800	μΑ
Low-level output current, IOL			16			16	mA
Operating free-air temperature, TA	55		125	0		70	°C

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DADAMETER	TEST CONDITIONS†	1	SN5486	3		SN7486	3	UNIT
	PARAMETER	TEST CONDITIONS.	MIN	TYP‡	MAX	MIN	TYP‡	MAX	UNIT
ViH	High-level input voltage		2			2			V
VIL	Low-level input voltage				8.0			0.8	V
VIK	Input clamp voltage	V <sub>CC</sub> = MIN, i <sub>1</sub> = -8 mA	1		-1.5			-1.5	V
.,	Illian I a secondaria	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V,	2.4	3.4		2.4	3.4		v
VOH	High-level output voltage	$V_{1L} = 0.8 \text{ V},  i_{OH} = -800 \mu\text{A}$	2.4	3.4		2.4	3.4		1
1/-	Law law law and the same	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V		0.2	0.4		0.2	0.4	V
VOL	Low-level output voltage	V <sub>1L</sub> = 0.8 V, 1 <sub>OL</sub> = 16 mA		0.2	0.4		0.2	0.4	
4	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>1</sub> = 5.5 V			1			1	mA
11H	High-level input current	V <sub>CC</sub> = MAX, V <sub>1</sub> = 2.4 V			40			40	μΑ
11L	Low-level input current	V <sub>CC</sub> = MAX, V <sub>1</sub> = 0.4 V			-1.6			-1.6	mA
los	Short-circuit output current§	V <sub>CC</sub> = MAX	20		-55	-18		-55	mA
¹CC	Supply current	V <sub>CC</sub> = MAX, See Note 2		30	43		30	50	mA

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

#### switching characteristics, VCC = 5 V, TA = 25°C

PARAMETER¶	FROM (INPUT)	TEST COM	IDITIONS	MIN	TYP	MAX	UNIT
tPLH	A or B	Oah as is such law.	C <sub>L</sub> = 15 pF,		15	23	ns
tPHL t	AOIB	Other input low	R <sub>L</sub> = 400 Ω,		11	17	
tPLH	A or B	Oshovinova biob	See Note 3		18	30	ns
tPHL	AOIB	Other input high	See Note 5		13	22	

 $\P_{tplH}$  = propagation delay time, low-to-high-level output

tpHL = propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



 $<sup>^{\</sup>ddagger}$ All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

<sup>§</sup>Not more than one output should be shorted at a time.

NOTE 2: ICC is measured with the inputs grounded and the outputs open.

# SN5486, SN54LS86A, SN54S86 SN7486, SN74LS86A, SN74S86 OHADDUDLE 2 INDUSTRIAL QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V <sub>CC</sub> (see Note 1)													7 V
Input voltage													7 V
Operating free-air temperature range: SN54LS86A	١.									-5	5°C	to 1	25°C
SN74LS86A	١.										0°0	to	70°C
Storage temperature range													

NOTE 1: Voltage values are with respect to network ground terminal.

#### recommended operating conditions

	S	N54LS	36A	SI	6A	UNIT	
	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, V <sub>CC</sub>	4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH			-400			-400	μА
Low-level output current, IOL			4			8	mA
Operating free-air temperature, TA	-55		125	0		70	°C

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

			un izionist	SI	154LS8	6A	SI	174LS8	6A	UNIT
	PARAMETER	TEST CO	NDITIONS <sup>†</sup>	MIN	TYP‡	MAX	MIN	TYP‡	MAX	UNIT
VIH	High-level input voltage			2			2			\ \ \ _
VIL	Low-level input voltage					0.7			0.8	V
VIK	Input clamp voltage	VCC = MIN,	I <sub>I</sub> = -18 mA			-1.5			-1.5	V
v <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = V <sub>IL</sub> max	V <sub>IH</sub> = 2 V, , I <sub>OH</sub> = -400 μA	2.5	3.4		2.7	3.4		٧
V. 0.	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V,	IOL = 4 mA		0.25	0.4		0.25	0.4	\ \ \
VOL.	Low-level output vortage	VIL = VILmax	1 <sub>OL</sub> = 8 mA					0.35	0.5	
11	Input current at maximum input voltage	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 7 V			0.2			0.2	mA
Чн	High-level input current	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 2.7 V			40			40	μА
IIL	Low-level input current	V <sub>CC</sub> = MAX,	V <sub>1</sub> = 0.4 V			-0.8			-0.8	mA
los	Short-circuit output current§	V <sub>CC</sub> = MAX		- 20		- 100	- 20		- 100	mA
Icc	Supply current	V <sub>CC</sub> = MAX,	See Note 2		6.1	10		6.1	10	mA

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.  $^{\ddagger}$ All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_{A} = 25^{\circ}\text{C}$ .

NOTE 2: I<sub>CC</sub> is measured with the inputs grounded and the outputs open.

#### switching characteristics, VCC = 5 V, TA = 25°C

PARAMETER¶	FROM (INPUT)	TEST CON	IDITIONS	MIN	TYP	MAX	UNIT
tpLH	A or B	Out as in suct low	C 15 pE		12	23	ns
t <sub>PHL</sub>	A Of B	Other input low	$C_L = 15 pF$ , $R_L = 2 kQ$ ,		10	17	
tpLH	A or B	Other input high	See Note 3		20	30	ns
tPHL	AOIB	Other input night	See Note 5		13	22	

<sup>¶</sup>tpLH = propagation delay time, low-to-high-level output



Not more than one output should be shorted at a time.

tpHL = propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

# OBSOLETE - No Longer Available SN5486, SN54LS86A, SN54S86 SN7486, SN74LS86A, SN74S86 **QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES**

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)													7 V
Input voltage													5.5 V
Operating free-air temperature range: SN54S86	3.										-55°	C to	125°C
SN74S86	3.										. 0	°C t	o 70°C
Storage temperature range					 						-65°	C to	150°C

NOTE 1: Voltage values are with respect to network ground terminal.

#### recommended operating conditions

		SN54S8	6		SN74S8	6	UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	ONI
Supply voltage, V <sub>CC</sub>	4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH			1			-1	mA
Low-level output current, IOL			20			20	mA
Operating free-air temperature, TA	-55		125	0		70	°C

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		Teet constitutionst		SN54S8	6	SN74S86			UNIT
	PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	MIN	TYP <sup>‡</sup>	MAX	10km
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.8			0.8	٧
VIK	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>1</sub> = -18 mA			-1.2		-	-1.2	٧
v <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>1H</sub> = 2 V, V <sub>1L</sub> = 0.8 V, I <sub>OH</sub> = -1 mA	2.5	3.4		2.7	3.4		٧
VOL	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 20 mA			0.5			0.5	V
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>i</sub> = 5.5 V			1			1	mA
Чн	High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V			50			50	μА
TIL	Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5 V	1		-2			-2	mA
los	Short-circuit output current§	V <sub>CC</sub> = MAX	-40		-100	-40		-100	mA
Icc	Supply current	V <sub>CC</sub> = MAX, See Note 2		50	75		50	75	mA

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

#### switching characteristics, VCC = 5 V, TA = 25°C

PARAMETER¶	FROM (INPUT)	TEST COM	TEST CONDITIONS			MAX	UNIT
tPLH	A or B	Other input low	$C_L = 15 \text{ pF},$ $R_L = 280 \Omega,$ See Note 3		7	10.5	ns
<sup>†</sup> PHL	1	Other input low			6.5	10	
tpLH	A or B	Other input high			7	10.5	ns
tpHL		Other input night			6.5	10	

TtpLH = propagation delay time, low-to-high-level output



<sup>‡</sup>All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ} \text{C}$ .

Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: ICC is measured with the inputs grounded and the outputs open.

tpHL = propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

#### PACKAGE OPTION ADDENDUM

1-Jun-2012

#### **PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
JM38510/07501BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
JM38510/07501BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
JM38510/07501BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
JM38510/30502B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
JM38510/30502B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
JM38510/30502BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
JM38510/30502BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
JM38510/30502BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
JM38510/30502BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
M38510/07501BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
M38510/07501BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
M38510/07501BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
M38510/07501BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
M38510/30502B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
M38510/30502B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
M38510/30502BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
M38510/30502BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
M38510/30502BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
M38510/30502BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
SN5486J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	
SN5486J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	
SN54LS86AJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SN54LS86AJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SN54S86J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SN54S86J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SN7486N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	
SN7486N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	
SN7486N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	
SN7486N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	



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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN74LS86AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS86AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS86ADE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS86ADE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS86ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS86ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS86ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS86ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS86ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS86ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS86ADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS86ADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS86AN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS86AN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS86AN3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	
SN74LS86AN3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	
SN74LS86ANE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS86ANE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS86ANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS86ANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	



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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN74LS86ANSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS86ANSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS86ANSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS86ANSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74S86D	NRND	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74S86D	NRND	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74S86DE4	NRND	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74S86DE4	NRND	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74S86DG4	NRND	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74S86DG4	NRND	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74S86N	NRND	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74S86N	NRND	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74S86N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	
SN74S86N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	
SN74S86NE4	NRND	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74S86NE4	NRND	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SNJ5486J	OBSOLETE	CDIP	J	14		TBD	A42	N / A for Pkg Type	
SNJ5486J	OBSOLETE	CDIP	J	14		TBD	A42	N / A for Pkg Type	
SNJ5486W	OBSOLETE	CFP	W	14		TBD	Call TI	Call TI	
SNJ5486W	OBSOLETE	CFP	W	14		TBD	Call TI	Call TI	
SNJ54LS86AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54LS86AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54LS86AJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SNJ54LS86AJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	





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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SNJ54LS86AW	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
SNJ54LS86AW	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
SNJ54S86FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54S86FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54S86J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SNJ54S86J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SNJ54S86W	NRND	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
SNJ54S86W	NRND	CFP	W	14	1	TBD	A42	N / A for Pkg Type	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder humps used between the die and package, or 2) lead-based die adhesive used between

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN5486, SN54LS86A, SN54S86, SN74S86, SN74LS86A, SN74S86:





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● Catalog: SN7486, SN74LS86A, SN74S86

• Military: SN5486, SN54LS86A, SN54S86

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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#### TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS86ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS86ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

# **PACKAGE MATERIALS INFORMATION**

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#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS86ADR	SOIC	D	14	2500	346.0	346.0	33.0
SN74LS86ANSR	SO	NS	14	2000	346.0	346.0	33.0

#### 14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

# W (R-GDFP-F14)

# CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB



# FK (S-CQCC-N\*\*)

### LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



# N (R-PDIP-T\*\*)

### PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



# D (R-PDSO-G14)

#### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



# D (R-PDSO-G14)

# PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



#### **MECHANICAL DATA**

### NS (R-PDSO-G\*\*)

# 14-PINS SHOWN

#### PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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