

74HC2G02; 74HCT2G02

Dual 2-input NOR gate

Rev. 04 — 11 May 2009

Product data sheet

1. General description

The 74HC2G02 and 74HCT2G02 are high-speed Si-gate CMOS devices. They provide two 2-input NOR gates.

The HC device has CMOS input switching levels and supply voltage range 2 V to 6 V.

The HCT device has TTL input switching levels and supply voltage range 4.5 V to 5.5 V.

2. Features

- Wide supply voltage range from 2.0 V to 6.0 V
- Symmetrical output impedance
- High noise immunity
- Low power dissipation
- Balanced propagation delays
- Multiple package options
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package				Version
	Temperature range	Name	Description		
74HC2G02DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm		SOT505-2
74HCT2G02DP					
74HC2G02DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm		SOT765-1
74HCT2G02DC					
74HC2G02GD	-40 °C to +125 °C	XSON8U	plastic extremely thin small outline package; no leads; 8 terminals; UTLP based; body 3 × 2 × 0.5 mm		SOT996-2
74HCT2G02GD					

4. Marking

Table 2. Marking code

Type number	Marking code
74HC2G02DP	H02
74HCT2G02DP	T02
74HC2G02DC	H02
74HCT2G02DC	T02
74HC2G02GD	H02
74HCT2G02GD	T02

5. Functional diagram

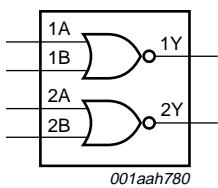


Fig 1. Logic symbol

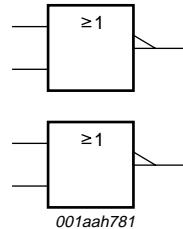


Fig 2. IEC logic symbol

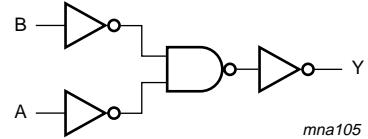


Fig 3. Logic diagram (one gate)

6. Pinning information

6.1 Pinning

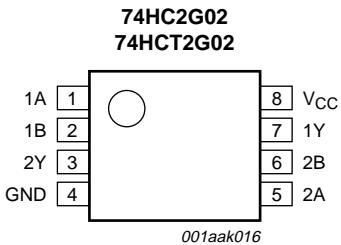


Fig 4. Pin configuration SOT505-2 (TSSOP8) and SOT765-1 (VSSOP8)

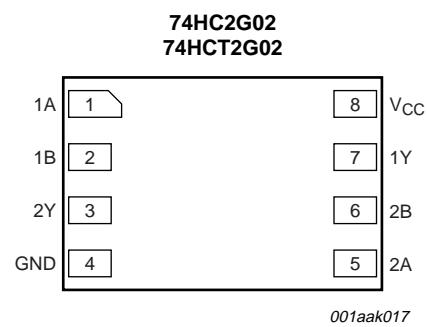


Fig 5. Pin configuration SOT996-2 (XSON8U)

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
1A, 2A	1, 5	data input
1B, 2B	2, 6	data input
GND	4	ground (0 V)
1Y, 2Y	7, 3	data output
V _{CC}	8	supply voltage

7. Functional description

Table 4. Function table^[1]

Input		Output
nA	nB	nY
L	L	H
L	H	L
H	L	L
H	H	L

[1] H = HIGH voltage level; L = LOW voltage level.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	[1] -	±20	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	[1] -	±20	mA
I _O	output current	V _O = -0.5 V to (V _{CC} + 0.5 V)	[1] -	25	mA
I _{CC}	supply current		[1] -	50	mA
I _{GND}	ground current		[1] -50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _D	dynamic power dissipation	T _{amb} = -40 °C to +125 °C	[2] -	300	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP8 package: above 55 °C the value of P_{tot} derates linearly with 2.5 mW/K.

For VSSOP8 package: above 110 °C the value of P_{tot} derates linearly with 8 mW/K.

For XSON8U package: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74HC2G02			74HCT2G02			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	−40 °C to +85 °C			−40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
74HC2G02								
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = −20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	V
		I _O = −20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	V
		I _O = −20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	V
		I _O = −4.0 mA; V _{CC} = 4.5 V	4.13	4.32	-	3.7	-	V
		I _O = −5.2 mA; V _{CC} = 6.0 V	5.63	5.81	-	5.2	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±1.0	-	±1.0	μA
I _{CC}	supply current	per input pin; V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	10	-	20	μA
C _I	input capacitance		-	1.5	-	-	-	pF

Table 7. Static characteristics ...continued
Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	−40 °C to +85 °C			−40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
74HCT2G02								
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} I _O = −20 μA; V _{CC} = 4.5 V I _O = −4.0 mA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 20 μA; V _{CC} = 4.5 V I _O = 4.0 mA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±1.0	-	±1.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	10	-	20	μA
ΔI _{CC}	additional supply current	per input; V _{CC} = 4.5 V to 5.5 V; V _I = V _{CC} − 2.1 V; I _O = 0 A	-	-	375	-	410	μA
C _I	input capacitance		-	1.5	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	−40 °C to +85 °C			−40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
74HC2G02								
t _{pd}	propagation delay	nA and nB to nY; see Figure 6	[2]					
		V _{CC} = 2.0 V	-	26	95	-	110	ns
		V _{CC} = 4.5 V	-	9	19	-	22	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	9	-	-	-	ns
		V _{CC} = 6.0 V	-	8	16	-	20	ns
t _f	transition time	see Figure 6	[3]					
		V _{CC} = 2.0 V	-	19	95	-	125	ns
		V _{CC} = 4.5 V	-	7	19	-	25	ns
		V _{CC} = 6.0 V	-	5	16	-	20	ns
C _{PD}	power dissipation capacitance	V _I = GND to V _{CC}	[4]	-	10	-	-	pF

Table 8. Dynamic characteristics ...continuedVoltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C			Unit
			Min	Typ ^[1]	Max	Min	Max		
74HCT2G02									
t_{pd}	propagation delay	nA and nB to nY; see Figure 6	[2]						
		$V_{CC} = 4.5 \text{ V}$	-	12	24	-	29	ns	
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	12	-	-	-	ns	
t_t	transition time	$V_{CC} = 4.5 \text{ V}$; see Figure 6	[3]	-	6	19	-	22	ns
C_{PD}	power dissipation	$V_I = \text{GND to } V_{CC} - 1.5 \text{ V}$	[4]	-	10	-	-	-	pF
	capacitance								

[1] All typical values are measured at $T_{amb} = 25 \text{ °C}$.[2] t_{pd} is the same as t_{PLH} and t_{PHL} .[3] t_t is the same as t_{TLH} and t_{THL} .[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

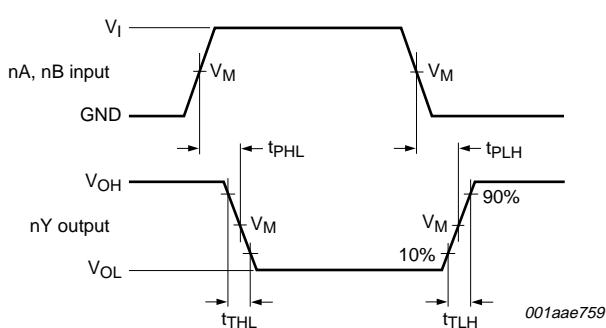
$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

 f_i = input frequency in MHz; f_o = output frequency in MHz; C_L = output load capacitance in pF; V_{CC} = supply voltage in V;

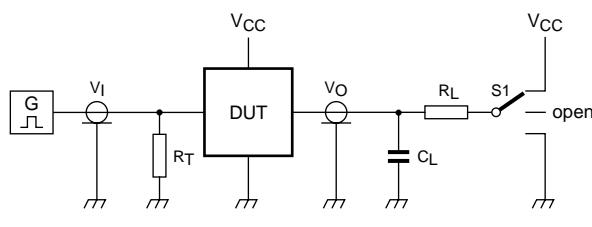
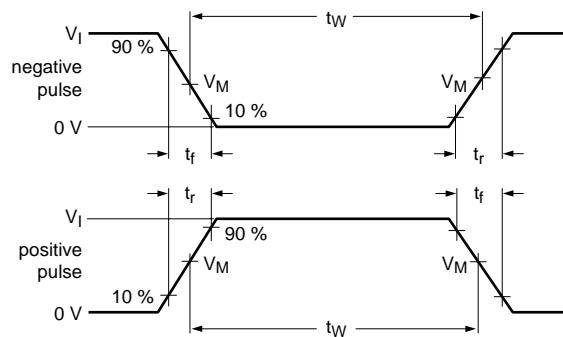
N = number of inputs switching;

$$\Sigma(C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs.}$$

12. Waveforms

Measurement points are given in [Table 9](#). V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.**Fig 6. Propagation delay data input (nA, nB) to data output (nY) and transition time output (nY)****Table 9. Measurement points**

Type	Input	Output
	V_M	V_M
74HC2G02	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74HCT2G02	1.3 V	1.3 V



001aad983

Test data is given in [Table 10](#).

Definitions for test circuit:

R_T = Termination resistance should be equal to output impedance Z_0 of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

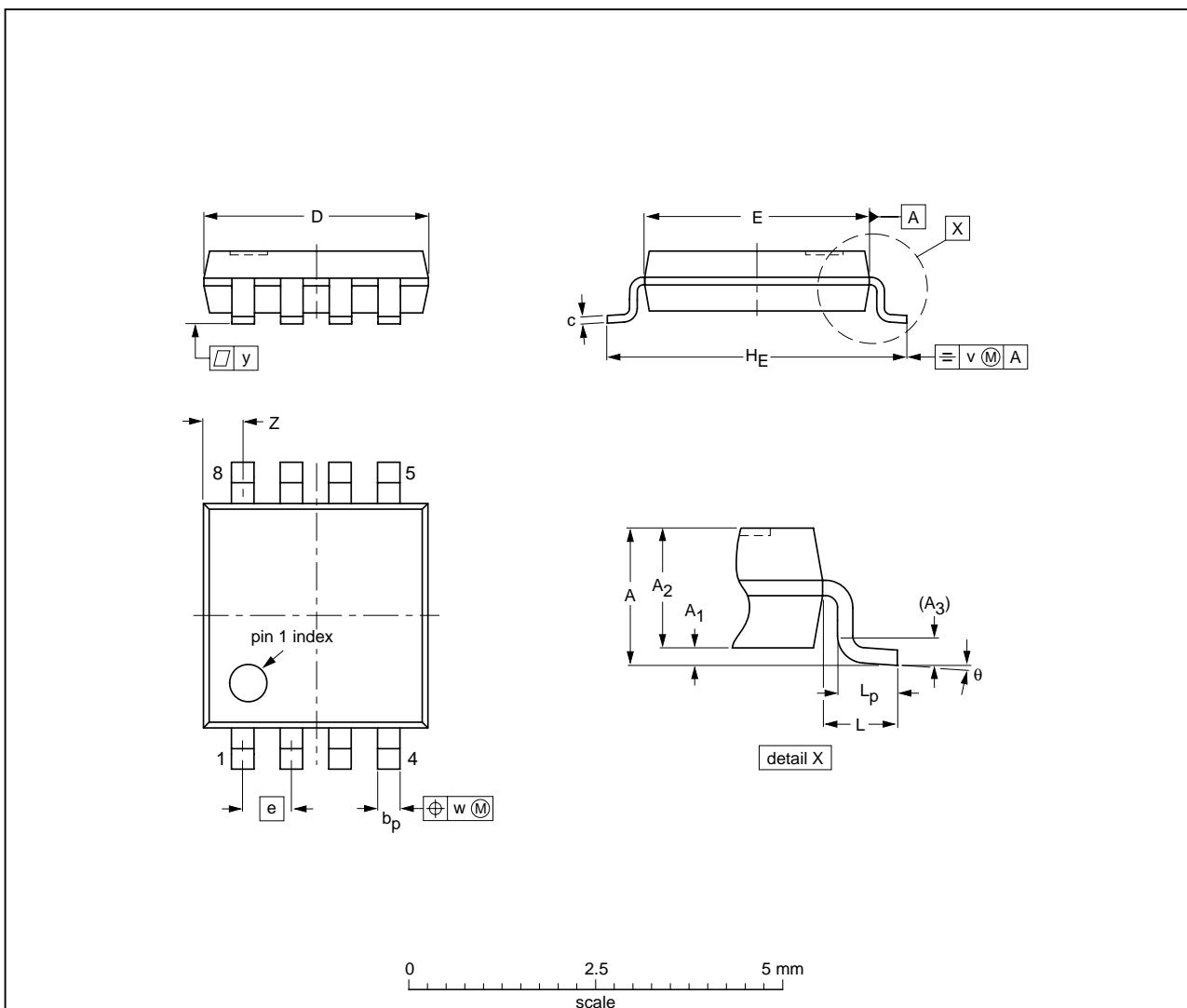
Fig 7. Load circuit for measuring switching times

Table 10. Test data

Type	Input		Load		S1 position
	V_I	t_r, t_f	C_L	R_L	
74HC2G02	GND to V_{CC}	≤ 6 ns	15 pF, 50 pF	1 k Ω	open
74HCT2G02	GND to 3 V	≤ 6 ns	15 pF, 50 pF	1 k Ω	open

13. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	v	w	y	Z ⁽¹⁾	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		---				02-01-16

Fig 8. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

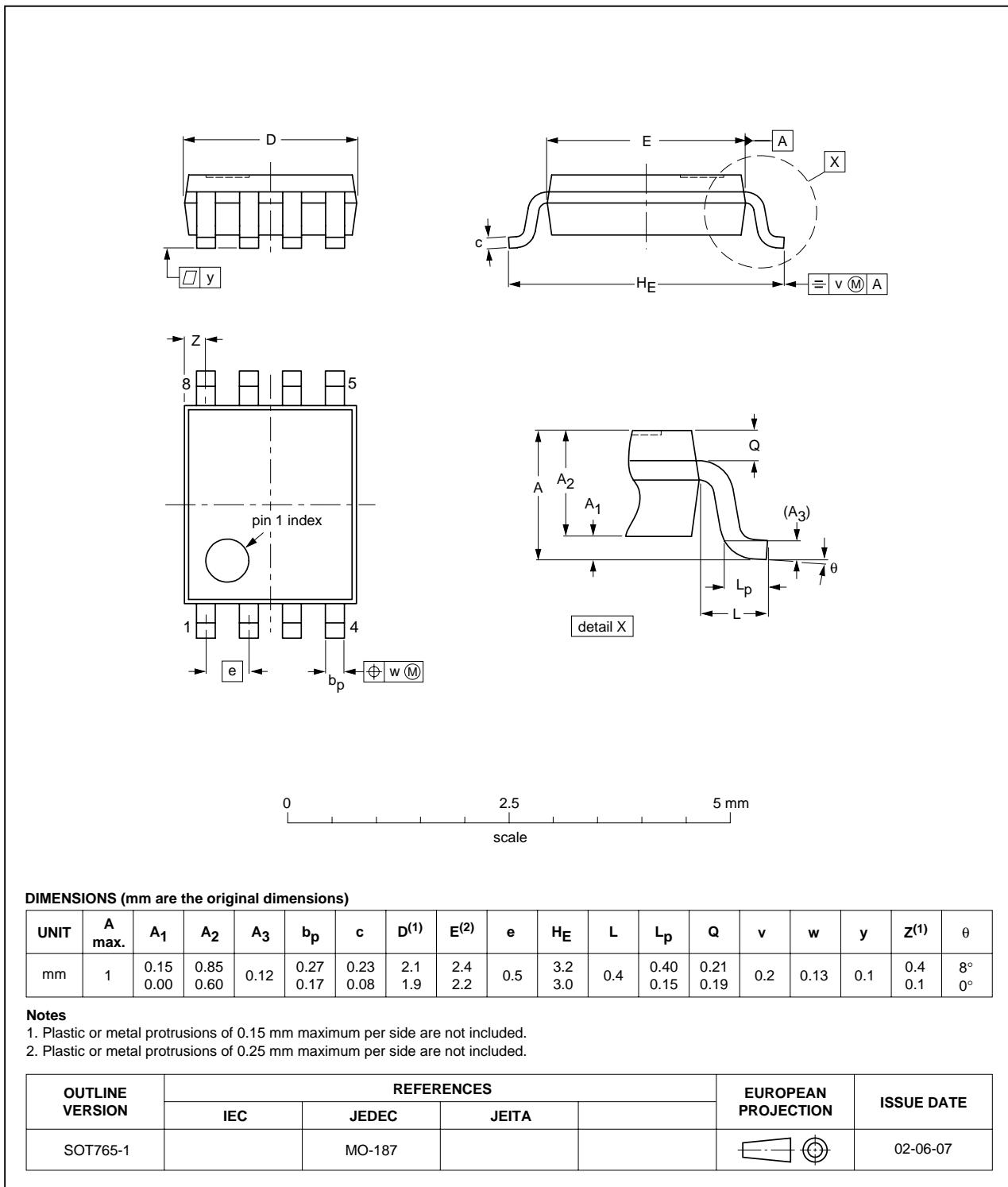


Fig 9. Package outline SOT765-1 (VSSOP8)

XSON8U: plastic extremely thin small outline package; no leads;
8 terminals; UTLP based; body 3 x 2 x 0.5 mm

SOT996-2

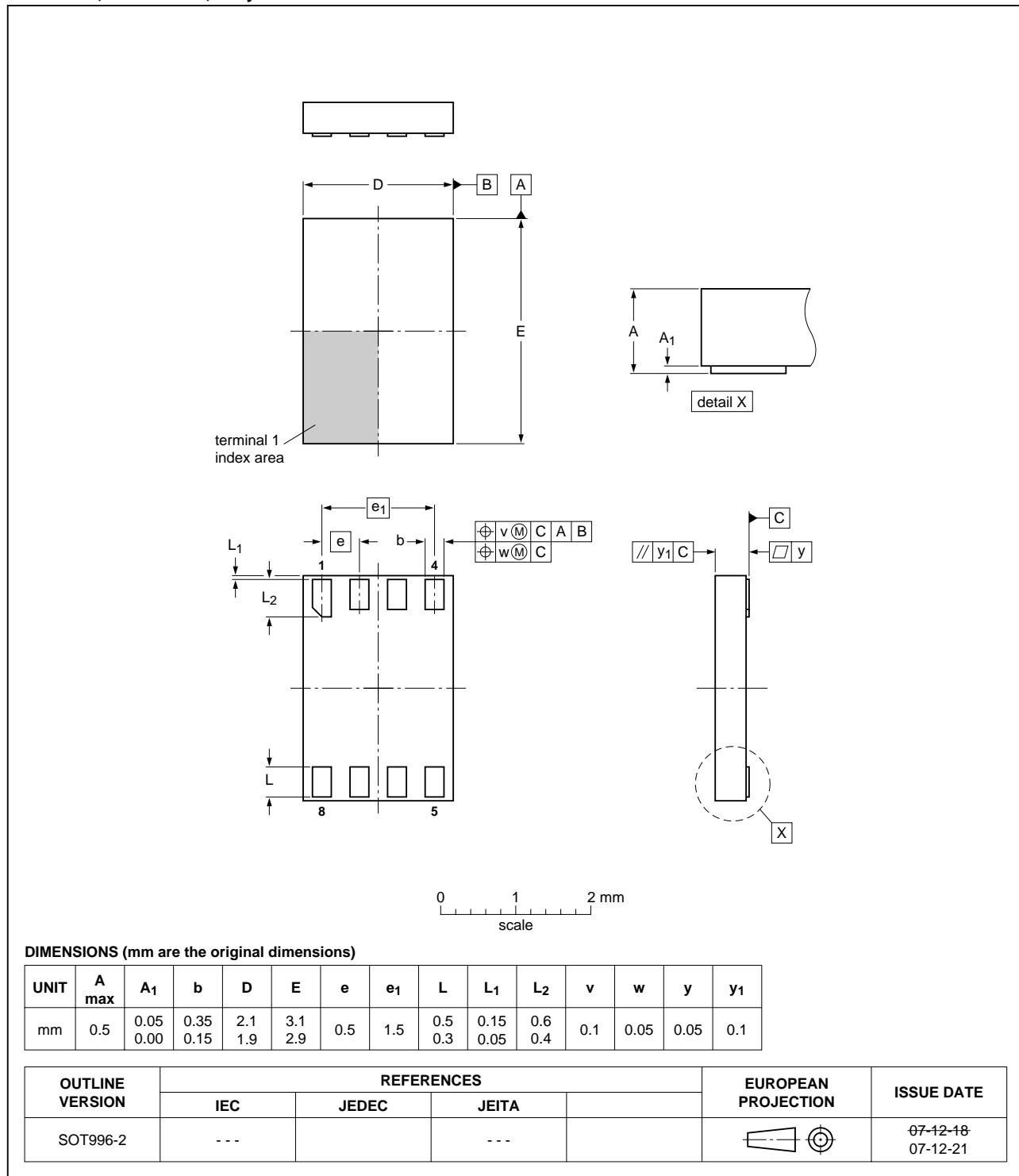


Fig 10. Package outline SOT996-2 (XSON8U)

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT2G02_4	20090511	Product data sheet	-	74HC_HCT2G02_3
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Added type number 74HC2G02GD and 74HCT2G02GD (XSON8U package) 			
74HC_HCT2G02_3	20030514	Product data sheet	-	74HC_HCT2G02_2
74HC_HCT2G02_2	20030203	Product specification	-	74HC_HCT2G02_1
74HC_HCT2G02_1	20020710	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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