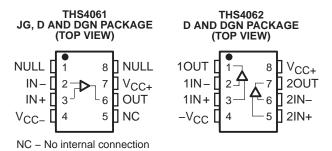
- High Speed
 - 180 MHz Bandwidth (G = 1, -3 dB)
 - 400 V/us Slew Rate
 - 40-ns Settling Time (0.1%)
- High Output Drive, I_O = 115 mA (typ)
- Excellent Video Performance
 - 75 MHz 0.1 dB Bandwidth (G = 1)
 - 0.02% Differential Gain
 - 0.02° Differential Phase
- Very Low Distortion
 - THD = –72 dBc at f = 1 MHz
- Wide Range of Power Supplies
 - V_{CC} = ± 5 V to ± 15 V
- Available in Standard SOIC, MSOP PowerPAD™, JG, or FK Package
- Evaluation Module Available

description

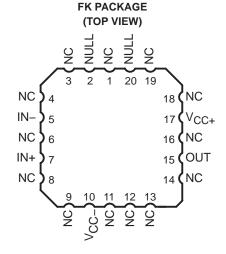
The THS4061 and THS4062 are generalpurpose, single/dual, high-speed voltage feedback amplifiers ideal for a wide range of applications including video, communication, and imaging. The devices offer very good ac performance with 180-MHz bandwidth, 400-V/µs slew rate, and 40-ns settling time (0.1%). The THS4061/2 are stable at all gains for both inverting and noninverting configurations. These amplifiers have a high output drive capability of 115 mA and draw only 7.8 mA supply current per channel. Excellent professional video results can be obtained with the low differential gain/phase errors of 0.02%/0.02° and wide 0.1 db flatness to 75 MHz. For applications requiring low distortion, the THS4061/2 is ideally suited with total harmonic distortion of -72 dBc at f = 1 MHz.

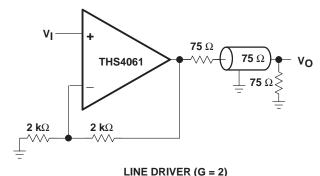




PowerPAD Option (DGN)

THS4061







CAUTION: The THS4061 and THS4062 provide ESD protection circuitry. However, permanent damage can still occur if this device is subjected to high-energy electrostatic discharges. Proper ESD precautions are recommended to avoid any performance degradation or loss of functionality



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments Incorporated.



	RELATED DEVICES
DEVICE	DESCRIPTION
THS4011/2	290-MHz Low Distortion High-Speed Amplifiers
THS4031/2	100-MHz Low Noise High Speed-Amplifiers
THS4061/2	180-MHz High-Speed Amplifiers

AVAILABLE OPTIONS

TA	NUMBER OF CHANNELS	PLASTIC SMALL OUTLINE [†] (D)	PLASTIC MSOP† (DGN)	CERAMIC DIP (JG)	CHIP CARRIER (FK)	MSOP SYMBOL	EVALUATION MODULES
0°C to	1	THS4061CD	THS4061CDGN	_	_	TIABS	THS4061EVM
70°C	2	THS4062CD	THS4062CDGN	_	_	TIABM	THS4062EVM
−40°C to	1	THS4061ID	THS4061IDGN	_	_	TIABT	_
85°C	2	THS4062ID	THS4062IDGN	_	_	TIABN	_
–55°C to 125°C	1	_	_	THS4061MJG	THS4061MFK	_	_

[†] The D and DGN packages are available taped and reeled. Add an R suffix to the device type (i.e., THS4061CDGNR).

functional block diagram

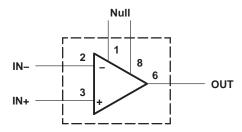


Figure 1. THS4061 - Single Channel

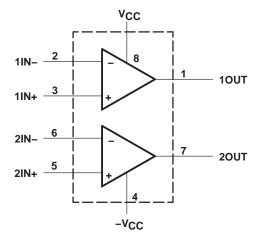


Figure 2. THS4062 - Dual Channel



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V _{CC} + to V _{CC}	
Input voltage, V _I	±V _{CC}
Output current, IO	150 mA
Differential input voltage, V _{IO}	
Continuous total power dissipation See	
Maximum junction temperature, T _{.1}	
Operating free-air temperature, TA: C-suffix	
I-suffix	–40°C to 85°C
M-suffix	–55°C to 125°C
Storage temperature, T _{stq}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds, D and DGN packag	
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds, JG package	300°C
Case temperature for 60 seconds, FK package	260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING	T _A = 125°C POWER RATING
D	740 mW	6 mW/°C	475 mW	385 mW	_
DGN [‡]	2.14 W	17.1 mW/°C	1.37 W	1.11 W	_
JG	1057 mW	8.4 mW/°C	627 mW	546 mW	210 mW
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW

[‡] The DGN package incorporates a PowerPAD on the underside of the device. This acts as a heatsink and must be connected to a thermal dissipation plane for proper power dissipation. Failure to do so can result in exceeding the maximum specified junction temperature, which could permanently damage the device.

recommended operating conditions

		MIN	NOM MAX	UNIT
Own book to be War and War	Dual supply	±4.5	±16	.,
Supply voltage, V _{CC} + and V _{CC} -	Single supply	9	32	V
	C-suffix	0	70	
Operating free-air temperature, TA	I-suffix	-40	85	°C
	M-suffix	-55	125	



SLOS234E - DECEMBER 1998 - REVISED DECEMBER 2003

electrical characteristics at T_A = 25°C, V_{CC} = ± 15 V, R_L = 150 Ω (unless otherwise noted)

dynamic performance

	PARAMETER	TEST CONDITIONS†			THS4061C/I, THS4062C/I			
				MIN	TYP	MAX		
		V _{CC} = ±5 V	Gain = 1		180		MHz	
	Dynamic performance small-signal bandwidth (–3 dB)	V _{CC} = ±15 V	Onto 4		50		MHz	
BW	bandwidth (=3 db)	V _{CC} = ±5 V	Gain = -1		50	50		
	Bandwidth for 0.1 dB flatness	V _{CC} = ±15 V	Coin 4	75			N 41 1-	
		V _{CC} = ±5 V	Gain = 1		20		MHz	
0.0	Olemente	$V_{CC} = \pm 15 \text{ V}$	Onto 4		400			
SR	Slew rate	V _{CC} = ±5 V	Gain = -1		350		V/μs	
	Contilion times to 0.404	$V_{CC} = \pm 15 \text{ V}, 5-\text{V step } (0 \text{ V to } 5 \text{ V})$	Onin 4		40			
_	Settling time to 0.1%	$V_{CC} = \pm 5 \text{ V}, \qquad V_{O} = -2.5 \text{ V to } 2.5 \text{ V},$	Gain = -1		40		ns	
t _S	Sottling time to 0.049/	$V_{CC} = \pm 15 \text{ V}, 5-\text{V step } (0 \text{ V to } 5 \text{ V})$	Coin 1		140			
	Settling time to 0.01%	$V_{CC} = \pm 5 \text{ V}, \qquad V_{O} = -2.5 \text{ V to } 2.5 \text{ V},$	Gain = -1		150		ns	

[†] Full range = 0°C to 70°C for C suffix and -40°C to 85°C for I suffix

noise/distortion performance

	PARAMETER		TEST CONDITIONS†			THS4061C/I, THS4062C/I		
						TYP	MAX	1
THD	Total harmonic distortion	f = 1 MHz				-72		dBc
٧n	Input voltage noise	f = 10 kHz,	$V_{CC} = \pm 5 \text{ V or } \pm 15 \text{ V}$			14.5		nV/√Hz
In	Input current noise	f = 10 kHz,	$V_{CC} = \pm 5 \text{ V or } \pm 15 \text{ V}$	_		1.6		pA/√Hz
	5.00			V _{CC} = ±15 V		0.02 %		
	Differential gain error	Gain = 2,	NTSC, 40 IRE modulation	V _{CC} = ±5 V		0.02 %		
			NEO (010E 1111	V _{CC} = ±15 V		0.02°		
	Differential phase error	Gain = 2,	NTSC, 40 IRE modulation	$V_{CC} = \pm 5 \text{ V}$		0.06°		
	Channel-to-channel crosstalk (THS4062 only)	V _{CC} = ±5 V 0	or ±15 V, f = 1 MHz			65		dB

[†] Full range = 0°C to 70°C for C suffix and –40°C to 85°C for I suffix

dc performance

	PARAMETER	TEST CONDITIONS [†]			THS4061C/I, THS4062C/I		
				MIN	TYP	MAX	
		V 145V V 140V B 410	T _A = 25°C	5	15		\//\/
	Open loop gain	$V_{CC} = \pm 15 \text{ V}, V_{O} = \pm 10 \text{ V}, R_{L} = 1 \text{ k}\Omega$	T _A = full range	4			V/mV
	Open loop gain	V 15V V- 105V B: 410	T _A = 25°C	2.5	8		\//\/
		$V_{CC} = \pm 5 \text{ V}, \qquad V_{O} = \pm 2.5 \text{ V}, R_{L} = 1 \text{ k}\Omega$	T _A = full range	2			V/mV
V	Input offset voltage	$V_{CC} = \pm 5 \text{ V or } \pm 15 \text{ V}$	T 6.11		2.5	8	mV
Vos	Offset drift	$V_{CC} = \pm 5 \text{ V or } \pm 15 \text{ V}$	T _A = full range		15		μV/°C
I _{IB}	Input bias current	$V_{CC} = \pm 5 \text{ V or } \pm 15 \text{ V}$	T _A = full range		3	6	μΑ
los	Input offset current	$V_{CC} = \pm 5 \text{ V or } \pm 15 \text{ V}$	T _A = full range		75	250	nA
	Offset current drift	T _A = full range			0.3		nA/°C

[†] Full range = 0°C to 70°C for C suffix and –40°C to 85°C for I suffix



electrical characteristics at T_A = 25°C, V_{CC} = ± 15 V, R_L = 150 Ω (unless otherwise noted) (continued) input characteristics

	PARAMETER		TEST CONDITIONS [†]			THS4061C/I, THS4062C/I		
					MIN	TYP	MAX	
V 0 1 1 1 1		$V_{CC} = \pm 15 \text{ V}$			±13.8	±14.1		.,
VICR	Common-mode input voltage range	$V_{CC} = \pm 5 \text{ V}$			±3.8	±4.3		V
CMDD	Common mode minetics matic	$V_{CC} = \pm 15 \text{ V},$	$V_{ICR} = \pm 12 V$	T _A = full range	70	110		dB
CMRR	Common mode rejection ratio	$V_{CC} = \pm 5 \text{ V},$	V _{ICR} = ±2.5 V		70	95		
R _I	Input resistance		•			1		MΩ
Ci	Input capacitance					2		pF

[†] Full range = 0°C to 70°C for C suffix and -40°C to 85°C for I suffix

output characteristics

PARAMETER		TEST CONDITIONS [†]			THS4061C/I, THS4062C/I		
				MIN	TYP	MAX	
		V _{CC} = ±15 V	$R_L = 250 \Omega$	±11.5	±12.5		.,
.,	Outrat valta as suita a	V _{CC} = ±5 V	R _L = 150 Ω	±3.2	±3.5		V
۷O	Output voltage swing	$V_{CC} = \pm 15 \text{ V}$	5 410	±13	±13.5		.,
		V _{CC} = ±5 V	$R_L = 1 k\Omega$	±3.5	±3.7		V
	Output summed	V _{CC} = ±15 V	D 00.0	80	115		4
Ю	Output current	V _{CC} = ±5 V	$R_L = 20 \Omega$	50	75		mA
Isc	Short-circuit current	V _{CC} = ±15 V			150		mA
RO	Output resistance	Open loop			12		Ω

[†] Full range = 0°C to 70°C for C suffix and –40°C to 85°C for I suffix

power supply

PARAMETER		TEST CONDITIONS	TEST CONDITIONS†			THS4061C/I, THS4062C/I			
				MIN	TYP	MAX			
		Dual supply		±4.5		±16.5			
VCC	Supply voltage operating range	Single supply	9		33	V			
		V _{CC} = ±15 V			7.8	10.5			
ICC	Quiescent current (per amplifier)	V _{CC} = ±5 V	T _A = full range		7.3	10	mA		
D0DD			T _A = 25°C	70	78		ID.		
PSRR	Power supply rejection ratio	$V_{CC} = \pm 5 \text{ V or } \pm 15 \text{ V}$	T _A = full range	68			dB		

[†] Full range = 0°C to 70°C for C suffix and -40°C to 85°C for I suffix



THS4061, THS4062 180-MHz HIGH-SPEED AMPLIFIERS

SLOS234E - DECEMBER 1998 - REVISED DECEMBER 2003

electrical characteristics at T_A = 25°C, V_{CC} = ± 15 V, R_L = 150 Ω (unless otherwise noted)

dynamic performance

	DADAMETED				TH				
	PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT	
	Unity-gain bandwidth	Closed loop,	$R_L = 1 \text{ k}\Omega$	V _{CC} = ±15 V	*140	180		MHz	
		V _{CC} = ±15 V		0-1- 4		180		N 41 1-	
	Dynamic performance small-signal	V _{CC} = ±5 V		Gain = 1		180		MHz	
BW	bandwidth (-3 dB)	$V_{CC} = \pm 15 \text{ V}$		0		50			
		$V_{CC} = \pm 5 \text{ V}$		Gain = -1		50		MHz	
		$V_{CC} = \pm 15 \text{ V}$		0.:. 4		75		MHz	
	Bandwidth for 0.1 dB flatness	$V_{CC} = \pm 5 \text{ V}$		Gain = 1		20			
SR	Slew rate	$V_{CC} = \pm 15 \text{ V}$	$R_L = 1 k\Omega$		*400	500		V/μs	
	Outlies time to 0.494	$V_{CC} = \pm 15 \text{ V},$	5-V step (0 V to 5 V)	Onto 4		40			
	Settling time to 0.1%	$V_{CC} = \pm 5 \text{ V},$	$V_0 = -2.5 \text{ V to } 2.5 \text{ V},$	Gain = -1		40		ns	
t _S	Settling time to 0.01%	$V_{CC} = \pm 15 \text{ V},$	5-V step (0 V to 5 V)	Gain = -1		140			
		$V_{CC} = \pm 5 \text{ V},$	$V_{O} = -2.5 \text{ V to } 2.5 \text{ V},$	Gain = -1		150		ns	

[†] Full range = -55° C to 125° C for M suffix

noise/distortion performance

			TEST SOUDITIONS!		THS4061M			
	PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
THD	Total harmonic distortion	f = 1 MHz				-72		dBc
٧n	Input voltage noise	f = 10 kHz,	$V_{CC} = \pm 5 \text{ V or } \pm 15 \text{ V}$			14.5		nV/√ Hz
In	Input current noise	f = 10 kHz,	$V_{CC} = \pm 5 \text{ V or } \pm 15 \text{ V}$			1.6		pA/√ Hz
	Differential main arms	Onia O	NTOO 40 IDE Madelation	$V_{CC} = \pm 15 \text{ V}$		0.02		0/
	Differential gain error	Gain = 2,	NTSC, 40 IRE Modulation	$V_{CC} = \pm 5 \text{ V}$		0.02		%
	Differential phase arror	Gain = 2.	NTCC 40 IDE Modulation	$V_{CC} = \pm 15 \text{ V}$		0.02°		
	Differential phase error	Gain = 2,	NTSC, 40 IRE Modulation	V _{CC} = ±5 V		0.06°		

[†] Full range = -55°C to 125°C for M suffix

dc performance

	DADAMETED	7507	CONDITIONS		TH	Λ	UNIT	
	PARAMETER	1531	CONDITIONST		MIN	TYP	MAX	UNII
		$V_{CC} = \pm 15 \text{ V}, V_{O} = \pm 10$	$V_{CC} = \pm 15 \text{ V}, V_{O} = \pm 10 \text{ V}, R_{L} = 1 \text{ k}\Omega$			9		
Open loop gain		$V_{CC} = \pm 5 \text{ V}, \qquad V_{O} = \pm 2.$	$V_{CC} = \pm 5 \text{ V}, \qquad V_{O} = \pm 2.5 \text{ V}, R_{L} = 1 \text{ k}\Omega$			6		V/mV
	Input offset voltage	V 15V 22145V	D 410	T _A = 25°C		2.5	8	mV
VIO		$V_{CC} = \pm 5 \text{ V or } \pm 15 \text{ V}$	$R_L = 1 k\Omega$	T _A = full range			9	mV
	Offset drift	$V_{CC} = \pm 5 \text{ V or } \pm 15 \text{ V}$	$R_L = 1 \text{ k}\Omega$	T _A = full range		15		μV/°C
I _{IB}	Input bias current	$V_{CC} = \pm 5 \text{ V or } \pm 15 \text{ V}$	$R_L = 1 \text{ k}\Omega$	T _A = full range		3	6	μΑ
ΙΙΟ	Input offset current	$V_{CC} = \pm 5 \text{ V or } \pm 15 \text{ V}$	$R_L = 1 \text{ k}\Omega$	T _A = full range		75	250	nA
	Offset current drift	$V_{CC} = \pm 5 \text{ V or } \pm 15 \text{ V}$	$R_L = 1 \text{ k}\Omega$	T _A = full range		0.3		nA/°C

[†] Full range = -55° C to 125° C for M suffix



^{*}This parameter is not tested.

electrical characteristics at T_A = full range, V_{CC} = ± 15 V, R_L = 1 k Ω (unless otherwise noted) (continued)

input characteristics

	DADAMETED	TEST SOMBITIONS.	T	И	UNIT	
	PARAMETER	TEST CONDITIONS†	MIN	TYP	MAX	UNII
.,	Opening and investment and	$V_{CC} = \pm 15 \text{ V}$	±13.8	±14.1		.,
VICR	Common-mode input voltage range	V _{CC} = ±5 V	±3.8	±4.3		V
CMDD	Common mode rejection ratio	$V_{CC} = \pm 15 \text{ V}, \qquad V_{ICR} = \pm 12 \text{ V}$	70	86		J.
CMRR		$V_{CC} = \pm 5 \text{ V}, \qquad V_{ICR} = \pm 2.5 \text{ V}$	80	90		dB
R _I	Input resistance			1		МΩ
Ci	Input capacitance			2		pF

[†] Full range = -55° C to 125° C for M suffix

output characteristics

	242445772			Т	Л	UNIT	
	PARAMETER	TEST CONDITIONS	TEST CONDITIONS				UNII
		V _{CC} = ±15 V	$R_L = 250 \Omega$	±12	±13.1		.,
v _O o	Output walks are suited	V _{CC} = ±5 V	$R_L = 150 \Omega$	±3.2	±3.5		V
	Output voltage swing	V _{CC} = ±15 V	D 410	±13	±13.5		V
		V _{CC} = ±5 V	$R_L = 1 k\Omega$	±3.5	±3.7		
	• • •	V _{CC} = ±15 V		70	115		
lO	Output current	V _{CC} = ±5 V	$R_L = 20 \Omega$	50	75		mA
Isc	Short-circuit current	V _{CC} = ±15 V	T _A = 25°C		150		mA
RO	Output resistance	Open loop			12		Ω

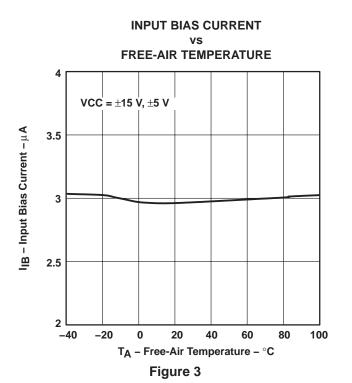
[†] Full range = -55°C to 125°C for M suffix

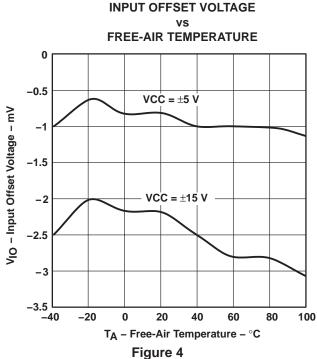
power supply

	24244555	TEGT GOVERNO		TH	VI	UNIT	
	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNII
.,	0 1 1	Dual supply		±4.5		±16.5	
VCC	Supply voltage operating range	Single supply		9		33	٧
	Quiescent current	V _{CC} = ±15 V	T. 0500		7.8	9	
١.		V _{CC} = ±5 V	$T_A = 25$ °C		7.3	8.5	mA
ICC		V _{CC} = ±15 V	T 6.11			11	
		V _{CC} = ±5 V	T _A = full range			10.5	
PSRR	Power supply rejection ratio	Vo o - +5 V or +15 V	T _A = 25°C	76	80		dВ
		$V_{CC} = \pm 5 \text{ V or } \pm 15 \text{ V}$	T _A = full range	74	78		dB

[†] Full range = -55° C to 125°C for M suffix

			FIGURE
I _{IB}	Input bias current	vs Free-air temperature	3
VIO	Input offset voltage	vs Free-air temperature	4
	Open-loop gain	vs Frequency	5
	Phase	vs Frequency	5
	Differential gain	vs Number of loads	6, 8
	Differential phase	vs Number of loads	7, 9
	Closed-loop gain	vs Frequency	10, 11
	Output amplitude	vs Frequency	12, 13
CMRR	Common-mode rejection ratio	vs Frequency	14
		vs Frequency	15
PSRR	Power supply rejection ratio	vs Free-air temperature	16
V _{O(PP)}	Output voltage swing	vs Supply voltage	17
ICC	Supply current	vs Free-air temperature	18
Env	Noise spectral density	vs Frequency	19
THD	Total harmonic distortion	vs Frequency	20, 21
	Crosstalk	vs Frequency	22, 23



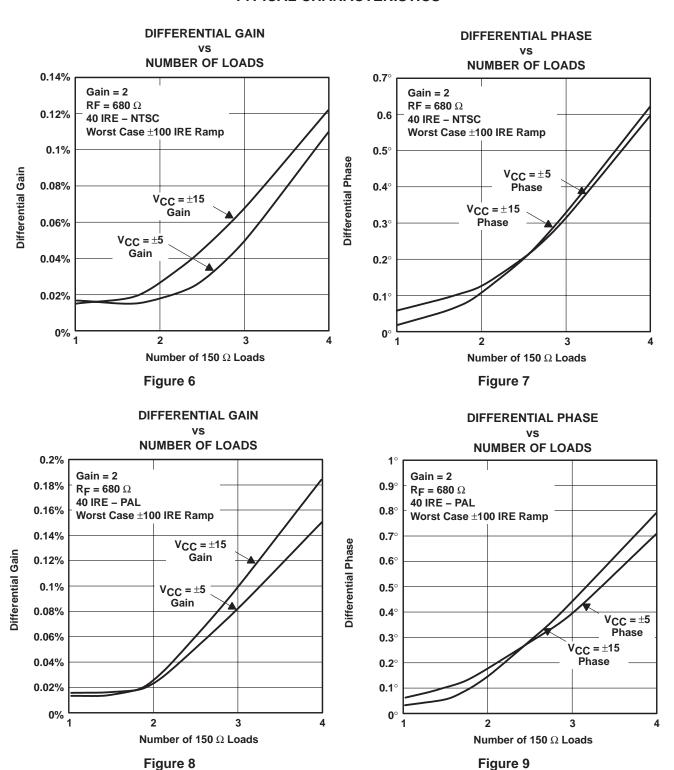


OPEN-LOOP GAIN AND PHASE

vs **FREQUENCY** 90 80 **0**° 70 Open-Loop Gain - dB 60 –45° Phase 50 40 **-90**° 30 20 -135° 10 0 –180° 10M 1k 10k 100k 1M 100M 1G f - Frequency - Hz



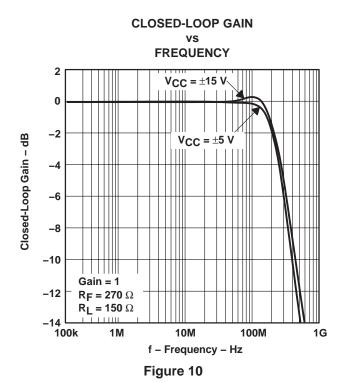
Figure 5

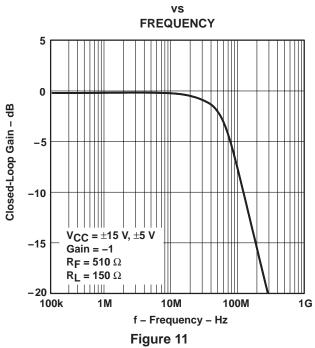


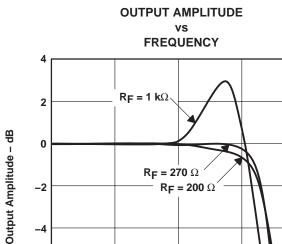


CLOSED-LOOP GAIN

TYPICAL CHARACTERISTICS







-2

-4

-6

-8

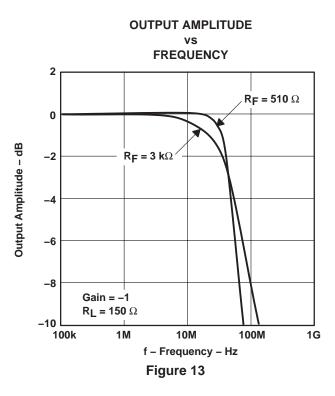
100k

Gain = 1

 $R_L = 150 \Omega$

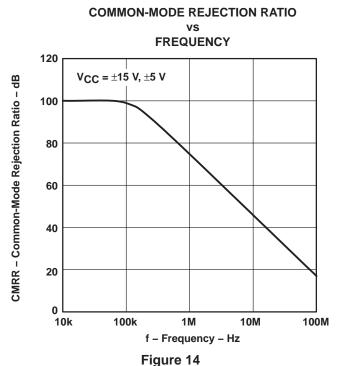
1M

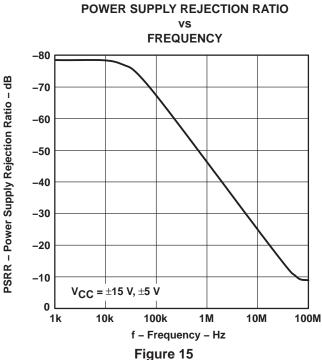
 $R_F = 270 \Omega$ $R_F = 200 \Omega$

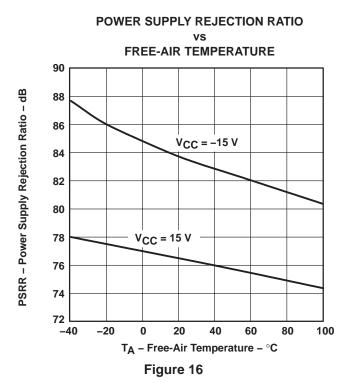


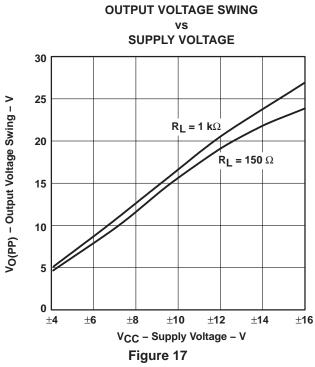
10M 100M f - Frequency - Hz Figure 12

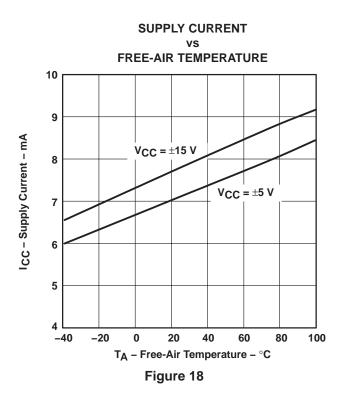
1G

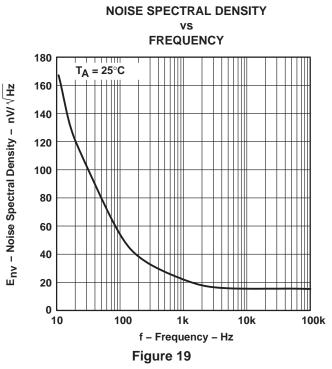


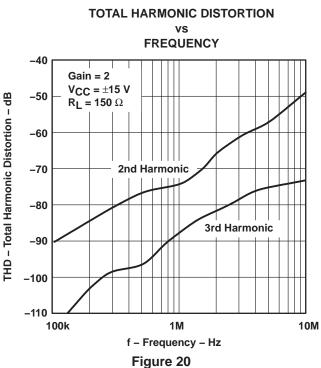


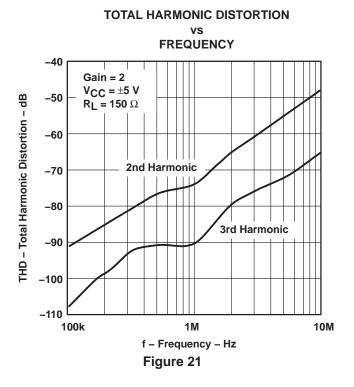


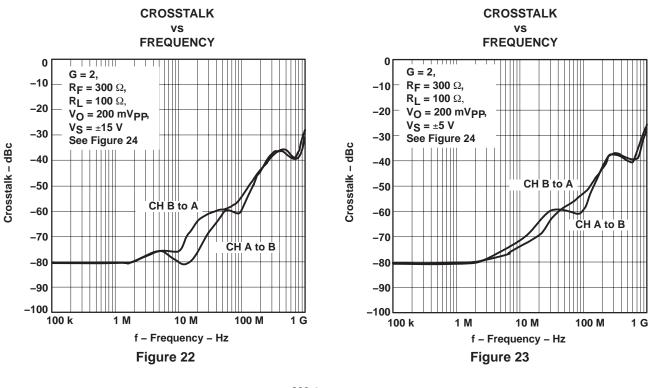












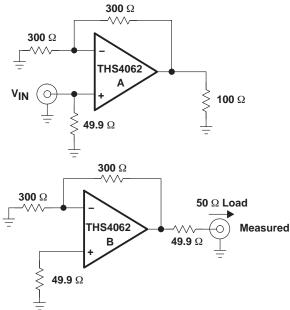


Figure 24. Test Circuits

theory of operation

The THS406x is a high speed, operational amplifier configured in a voltage feedback architecture. It is built using a 30-V, dielectrically isolated, complementary bipolar process with NPN and PNP transistors possessing f_{TS} of several GHz. This results in an exceptionally high performance amplifier that has a wide bandwidth, high slew rate, fast settling time, and low distortion. A simplified schematic is shown in Figure 25.

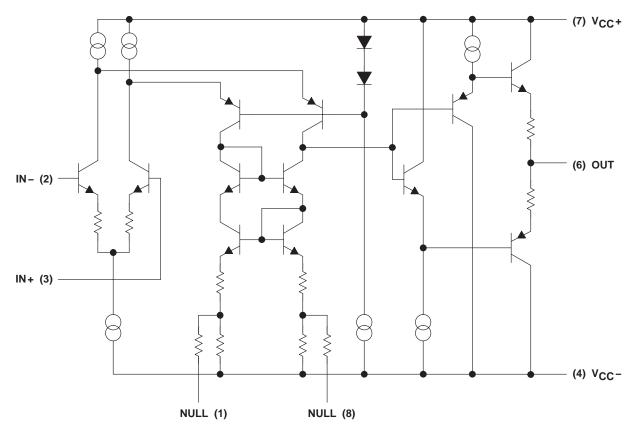


Figure 25. THS4061 Simplified Schematic

offset nulling

The THS4061 has very low input offset voltage for a high-speed amplifier. However, if additional correction is required, an offset nulling function has been provided. By placing a potentiometer between terminals 1 and 8 and tying the wiper to the negative supply, the input offset can be adjusted. This is shown in Figure 26.

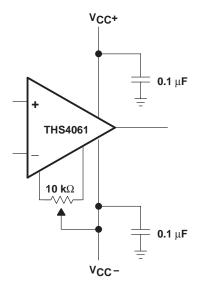


Figure 26. Offset Nulling Schematic

optimizing unity gain response

Internal frequency compensation of the THS406x was selected to provide very wideband performance yet still maintain stability when operated in a noninverting unity gain configuration. When amplifiers are compensated in this manner there is usually peaking in the closed loop response and some ringing in the step response for very fast input edges, depending upon the application. This is because a minimum phase margin is maintained for the G=+1 configuration. For optimum settling time and minimum ringing, a feedback resistor of 270 Ω should be used as shown in Figure 27. Additional capacitance can also be used in parallel with the feedback resistance if even finer optimization is required.

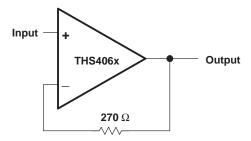


Figure 27. Noninverting, Unity Gain Schematic



driving a capacitive load

Driving capacitive loads with high performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS406x has been internally compensated to maximize its bandwidth and slew rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 28. A minimum value of 20 Ω should work well for most applications. For example, in 75- Ω transmission systems, setting the series resistor value to 75 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

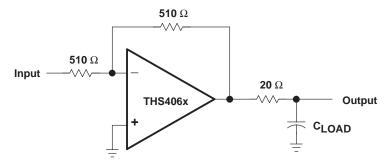


Figure 28. Driving a Capacitive Load

circuit layout considerations

In order to achieve the levels of high frequency performance of the THS406x, it is essential that proper printed-circuit board high frequency design techniques be followed. A general set of guidelines is given below. In addition, a THS406x evaluation board is available to use as a guide for layout or for evaluating the device performance.

- Ground planes It is highly recommended that a ground plane be used on the board to provide all
 components with a low inductive ground connection. However, in the areas of the amplifier inputs and
 output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distances increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets Sockets are not recommended for high-speed operational amplifiers. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements Optimum high frequency performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This helps to minimize stray capacitance at the input of the amplifier.



circuit layout considerations (continued)

 Surface-mount passive components – Using surface-mount passive components is recommended for high-frequency amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout, thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

evaluation board

An evaluation board is available for the THS4061 (literature number SLOP226) and THS4062 (literaure number SLOP235). This board has been configured for very low parasitic capacitance in order to realize the full performance of the amplifier. A schematic of the evaluation board is shown in Figure 29. The circuitry has been designed so that the amplifier may be used in either an inverting or noninverting configuration. To order the evaluation board contact your local TI sales office or distributor. For more detailed information, refer to the THS4061 EVM User's Manual (literature number SLOU038) or the THS4062 EVM User's Manual (literature number SLOU040)

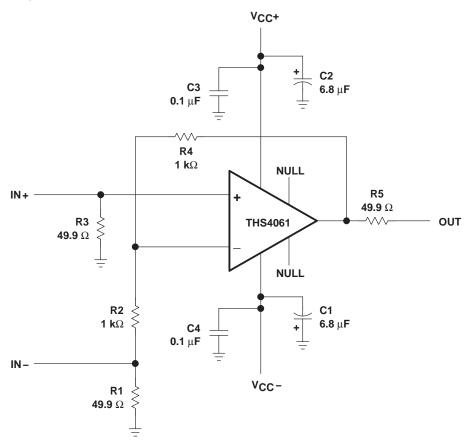


Figure 29. THS4061 Evaluation Board Schematic



5-Sep-2011

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-9960101Q2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-9960101QPA	ACTIVE	CDIP	JG	8	1	TBD	Call TI	Call TI	
THS4061CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
THS4061CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
THS4061CDGN	ACTIVE	MSOP- PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
THS4061CDGNG4	ACTIVE	MSOP- PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
THS4061CDGNR	ACTIVE	MSOP- PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
THS4061CDGNRG4	ACTIVE	MSOP- PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
THS4061CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
THS4061CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
THS4061ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
THS4061IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
THS4061IDGNR	ACTIVE	MSOP- PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
THS4061IDGNRG4	ACTIVE	MSOP- PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
THS4061IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
THS4061IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
THS4061MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
THS4061MJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	
THS4061MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	





5-Sep-2011

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
THS4062CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
THS4062CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
THS4062CDGN	ACTIVE	MSOP- PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
THS4062CDGNG4	ACTIVE	MSOP- PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
THS4062CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
THS4062CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
THS4062ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
THS4062IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
THS4062IDGN	ACTIVE	MSOP- PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
THS4062IDGNG4	ACTIVE	MSOP- PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
THS4062IDGNR	ACTIVE	MSOP- PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
THS4062IDGNRG4	ACTIVE	MSOP- PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
THS4062IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
THS4062IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.



PACKAGE OPTION ADDENDUM

5-Sep-2011

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF THS4061, THS4061M:

Catalog: THS4061

Military: THS4061M

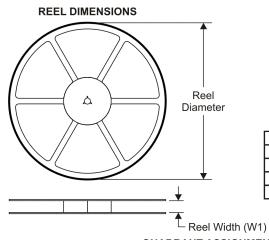
NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

www.ti.com 25-Jun-2011

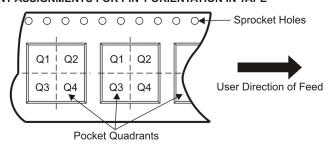
TAPE AND REEL INFORMATION



TAPE DIMENSIONS + K0 - P1 - B0 W Cavity - A0 -

	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4061CDGNR	MSOP- Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4061CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4061IDGNR	MSOP- Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4061IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4062CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4062IDGNR	MSOP- Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4062IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

www.ti.com 25-Jun-2011



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4061CDGNR	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0
THS4061CDR	SOIC	D	8	2500	346.0	346.0	29.0
THS4061IDGNR	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0
THS4061IDR	SOIC	D	8	2500	346.0	346.0	29.0
THS4062CDR	SOIC	D	8	2500	346.0	346.0	29.0
THS4062IDGNR	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0
THS4062IDR	SOIC	D	8	2500	346.0	346.0	29.0

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification.
- E. Falls within MIL STD 1835 GDIP1-T8

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



DGN (S-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com www.ti.com.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO-187 variation AA-T

PowerPAD is a trademark of Texas Instruments.



DGN (S-PDSO-G8)

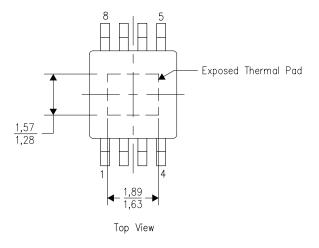
PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD $^{\text{M}}$ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

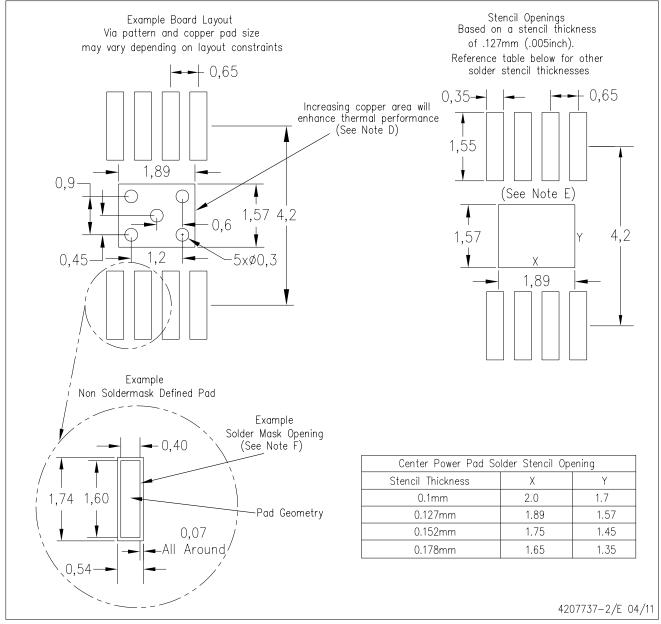
4206323-2/H 05/11

NOTE: All linear dimensions are in millimeters



DGN (R-PDSO-G8)

PowerPADTM PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com www.ti.com. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Applications

interface.ti.com

Audio www.ti.com/audio Communications and Telecom www.ti.com/communications **Amplifiers** amplifier.ti.com Computers and Peripherals www.ti.com/computers dataconverter.ti.com Consumer Electronics www.ti.com/consumer-apps **Data Converters DLP® Products** www.dlp.com **Energy and Lighting** www.ti.com/energy DSP dsp.ti.com Industrial www.ti.com/industrial Clocks and Timers www.ti.com/clocks Medical www.ti.com/medical

Logic logic.ti.com Space, Avionics and Defense www.ti.com/space-avionics-defense

Security

Power Mgmt power.ti.com Transportation and Automotive www.ti.com/automotive

Microcontrollers microcontroller.ti.com Video and Imaging www.ti.com/video

RFID <u>www.ti-rfid.com</u>
OMAP Mobile Processors www.ti.com/omap

Interface

Wireless Connctivity www.ti.com/wirelessconnectivity

TI E2E Community Home Page <u>e2e.ti.com</u>

www.ti.com/security