SN54ALS33A, SN74ALS33A QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS WITH OPEN-COLLECTOR OUTPUTS

SN7

SDAS034C - APRIL 1982 - REVISED FEBRUARY 2009

 Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

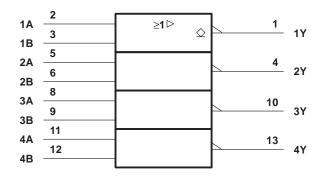
description

These devices contain four independent 2-input positive-NOR buffers with open-collector outputs. Open-collector outputs require resistive pullup to perform correctly. They can deliver higher V_{OH} levels and commonly are used in wired-AND applications. These devices perform the Boolean functions $Y = \overline{A} \bullet \overline{B}$ or $Y = \overline{A + B}$ in positive logic.

The SN54ALS33A is characterized for operation over the full military temperature range of -55° C to 125°C. The SN74ALS33A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)									
	INPUTS OUTPUT								
	Α	В	Y						
Γ	Н	Х	L						
	Х	Н	L						
	L	L	Н						

logic symbol[†]

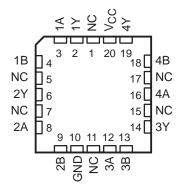


⁺ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the D, J, and N packages.

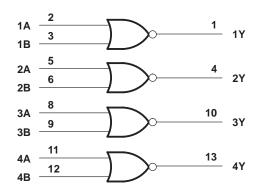
SN54ALS33A J PACKAGE 174ALS33A D OR N PACKAGE (TOP VIEW)									
		\cup	h						
1Y L	1	14	ll vcc						
1Y [1A [13] ∨ _{CC}] 4Y						
1B [3	12]4B						
2Y [4	11]4A						
2A [5	10]3Y						
2B [6	9] 3B						
2A [2B [GND [7	8] 3A						

SN54ALS33A . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

logic diagram (positive logic)



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Off-state output voltage		
	SN54ALS33A	
operating nee an temperature range, rg.	SN74ALS33A	
Storage temperature range		. −65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54ALS33A		SN74ALS33A				
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
VOH	High-level output voltage			5.5			5.5	V
IOL	Low-level output current			12			24	mA
Т _А	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

				SN54ALS33A		SN74ALS33A			
PARAMETER	TES	TEST CONDITIONS			MAX	MIN	TYP‡	MAX	UNIT
VIK	V _{CC} = 4.5 V,	lı = –18 mA			-1.5			-1.5	V
	N 45V	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	
VOL	$V_{CC} = 4.5 V$	I _{OL} = 24 mA					0.35	0.5	V
lj	V _{CC} = 5.5 V,	$V_{I} = 7 V$			0.1			0.1	mA
Iн	V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μA
١ _{١L}	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.1			-0.1	mA
ЮН	V _{CC} = 4.5 V,	V _{OH} = 5.5 V			0.1			0.1	mA
Іссн	V _{CC} = 5.5 V,	$V_{I} = 0$		1.7	2.8		1.7	2.8	mA
ICCL	V _{CC} = 5.5 V,	V _I = 4.5 V		5.6	9		5.6	9	mA

[‡] All typical values are at V_{CC} = 5 V, T_A = 25° C.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	то (оитрит)	$V_{CC} = 4.5 V \text{ to } 5.5 V,$ $C_L = 50 \text{ pF},$ $R_L = 680 \Omega,$ $T_A = \text{MIN to MAX}$ §				UNIT
			SN54A				
			MIN	MAX	MIN	MAX	
^t PLH	A or B	v	10	59	10	33	ns
^t PHL	AUD		2	18	2	12	115

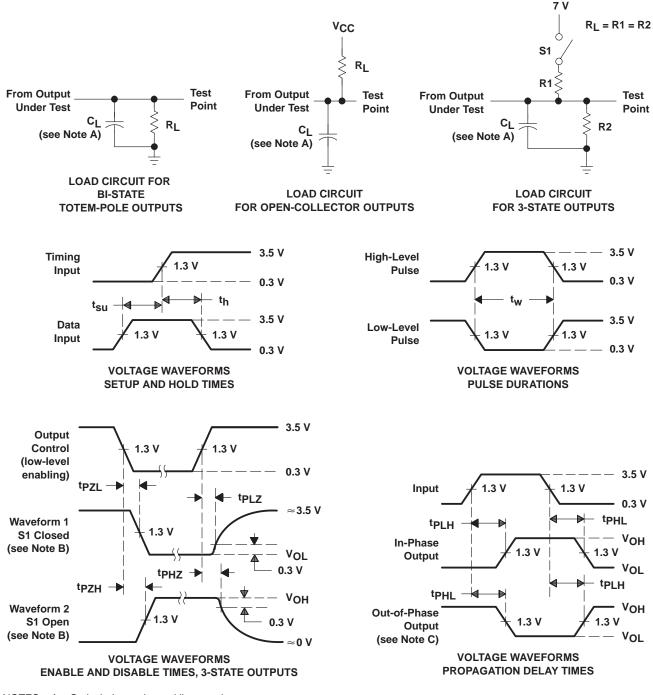
§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



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PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
- D. All input pulses have the following characteristics: PRR \leq 1 MHz, t_r = t_f = 2 ns, duty cycle = 50%.
- E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



PACKAGING INFORMATION

RUMENTS

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN54ALS33AJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
SN74ALS33AD	NRND	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS33ADE4	NRND	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS33ADG4	NRND	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS33AN	NRND	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS33AN3	OBSOLETE	PDIP	Ν	14		TBD	Call TI	Call TI
SN74ALS33ANE4	NRND	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SNJ54ALS33AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54ALS33AJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T**) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

LEADLESS CERAMIC CHIP CARRIER

FK (S-CQCC-N**) 28 TERMINAL SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.





NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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