The **Seiko Instruments** family of LCDC-1330 controller boards features the advanced SED1330 IC described in the previous section. These controller boards are designed to allow the user to quickly interface our graphic modules with the Intel 8085 or Motorola 6800 series microprocessors to display text, graphics, and overlayed text and graphics. The controller boards support 32K bytes of static RAM as display memory that can be defined as text space or graphics space. These memory spaces may be overlayed to produce mixed graphics and text, inverse video, area blinking, and overlay masking.

MEMORY SIZE SELECTION

Resolution of LCD	Min. memory size for 1 screen	Model number
128 X 128	2K	LCDC-1300-32A
240 X 64	2K	LCDC-1300-32A
192 X 128	3K	LCDC-1300-32A
192 X 192	5K	LCDC-1300-32A
240 X 128	4K	LCDC-1300-32A
320 X 200	8K	LCDC-1300-32A
320 X 240	8K	LCDC-1300-32A
640 X 20	16K	LCDC-1300-32A

LCDC-1330 FEATURES

CHARACTER DISPLAY MODE

- Programmable or automatic cursor shift function
- Flexible scroll function
- ▶ Two or three screen layered function
- Block or underline cursor function
- Area flashing function
- ▶ Internal character generator: JIS 160 characters (5x7)
- External character generator: 256 characters (8x8 or 8x16)

GRAPHIC DISPLAY MODE

- Maximum display size: 640 dots (H) x 256 dots (V)
- 2 or 3 screen overlayed function
- ▶ Independent block flashing and on/off control
- Graphic display mode can be mixed with character display mode

Electrical Characteristics (T_{OPR} =0°C TO 50°C V_{DD}=5V±5%, V_{SS}=0V)

Symbol	Paramater	Min.	Тур.	Max.	Units	Conditions	Terminals
V _{DD}	Supply Voltage	4.0	5.0	6.0	V		V _{DD}
V _{DDPD}	Power Down Supply Voltage	2.0		6.0	V		
TTL							
V _{IHT}	Input High Voltage (TTL)	2.2		$V_{DD}=0.3$	V		<u>D</u> ₀ - <u>D</u> ₇ , <u>A0</u>
V _{ILT}	Input Low Voltage (TTL)	-0.3		0.8	V		CS RD WR
V _{OHT}	Output High Voltage (TTL)	2.4			V	I _{OH} =-0.5mA	
V _{OLT}	Output Low Voltage (TTL)			0.4	V	I _{OL} =5.0mA	
CMOS							
V _{IHC}	Input High Voltage (CMOS)	$0.8V_{DD}$			V		DB0-DB3, FLM, M
V _{ILC}	Input Low Voltage (CMOS)			0.2V _{DD}	V		CL1 CL2
V _{OHC}	Output High Voltage (CMOS)	V _{DD} -0.4			V	I _{OH} =1.6mA	
V _{OLC}	Output Low Voltage (CMOS)	-		0.4	V	I _{OL} =1.6mA	
SCHMITT							
V _{T+}	Positive-going Threshold Voltage	0.5V _{DD}	0.7V _{DD}	0.8V _{DD}	V		RES
V _{T-}	Negative-going Threshold Voltage	- 0.2V _{DD} -	$0.3V_{DD}$	$0.5V_{DD}$	V		RES
I _{LI}	Input Leakage Current	-	0.05	2.0	μΑ		
I _{LO}	Output Leakage Current	-	0.10	5.0	μΑ		
I _{OPR}	Average Dynamic Power Consumption	-	8.0	12	mA		
Ι _Q	Average Static Power Consumption	-	0.05	20	μΑ		

PIN ASSIGNMENT

CN1: C	CN1: CONNECTION FOR MICROPROCESSOR INTERFACE							
PIN#	PIN# SIGNAL PIN# SIGNAL							
1	*RESET	9	D ₃					
2	*RD (E)	10	D ₄					
3	*WR (R/*W)	11	D ₅					
4	*CS	12	D ₆					
5	AO	13	D ₇					
6	D ₀	14	V _{DD} (+5V)					
7	D ₁	15	V _{SS} (GND)					
8	D ₂	16	V _{LCD}					

*Active low on the control signal

	CN2: CONNECTION FOR LCD INTERFACE								
PIN#	PIN# SIGNAL PIN# SIGNAL								
1	DB ₃	7	CL1 (LP)						
2	DB ₂	8	CL2 (XSCL)						
3	DB ₁	9	V _{DD} (+5V)						
4	DB ₀	10	V _{SS} (GND)						
5	FLM (YD)	11	V ₀						
6	M (WF)	12	V _{LCD}						

The microprocessor may access the command/status register or read/write data by changing the value of *RD, *WR, and A0.

CN3: CONTRAST ADJUSTMENT						
PIN# SIGNAL						
1	V _{DD} (+5V)					
2	V ₀					
3	V _{LCD}					

J1: JUMPER SETTINGS FOR CPU
1-2: Select Intel 8085 or Z80 microprecessor
2-3: Select Motorola 6800 microprocessor

CONTROL SIGNAL STATUS

INTEL 8080 SERIES						
A0 *RD *WR FUNCTION						
0	0	1	Status Register Read			
1	0	1	Read Data			
0	1	0	Write Data			
1	1	0	Command Register Write			

*Active low on the control signal

MOTOROLA 6800 SERIES					
A0 E R/W FUNCTION					
0	0	1	Status Register Read		
1	0	1	Read Data		
0	1	0	Write Data		
1	1	0	Command Register Write		

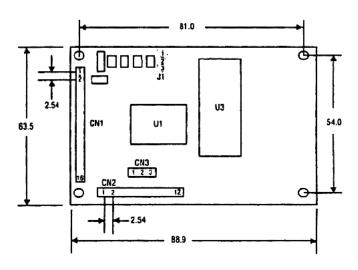
*Active low on the control signal

Except for the Erase command, the LCDC-1330 does not require the CPU to check the ready status between passing commands or parameters. When issuing the Erase command, the CPU must wait for at least two frame times before writing a new command to the LCDC-1330.

LCDC-1330 CHARACTERISTICS

Absolute Maximum Ratings						
ITEM	SPECIFICATION					
Supply Voltage (V _{DD}) Voltage on Any Pin Width	-0.3V to +7 0V					
Respect to Ground (V _{SS})	-0.5V to V _{DD} + 0 5					
Operating Temperature	0°C to 50°C					
Storage Temperature	-20°C to 60°C					
Power Consumption	60mW					

DIMENSIONS OF LCDC-1330 (MM)

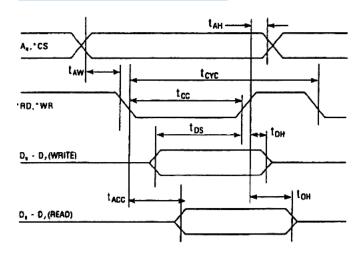


MICROPROCESSOR INTERFACE TIMING

(T_{OPR}=0°C TO 50°C V_{DD}=5.0V+10%)

Signal	Symbol	Parameter	Min.	Max.	Units
80 SERIES TIMING					
WR,RD	t _{cyc}	System Cycle Time	1000		ns
	t _{cc}	Control Pulse Width	220		ns
68 SERIES TIMING					
A0 CS RW	tcyc	System Cycle Time	1000		ns
E	t _{ew}	Enable Pulse Width	220		ns
TIMING FOR 80 MD 6	58 Series Pro	CESSORS			
A0, CS	t _{ah}	Address Hold Time	10		ns
	t _{aw}	Address Setup Time	30		ns
D_0-D_7	t _{DS}	Data Setup Time	120		ns
	t _{dh}	Data Hold Time	10		ns
	tacc	RD Access Time		120	ns
	t _{он}	Output Disable Time	10	50	ns

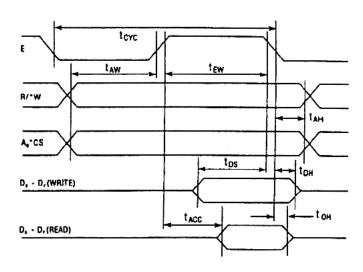
80 (Series Timing Diagram)



INSTRUCTION SET SUMMARY

System Set	0100000	40h	
Display On	01011001	59h	
Display Off	01011000	58h	
Overlay	01011011	5Bh	
CG RAM Address	01011100	5Ch	
Scroll	01000100	44h	
Horiz. Dot Scroll	01011010	5Ah	
Cursor Format	01011101	5Dh	
Cursor Right	01001100	4Ch	
Cursor Left	01001101	4Dh	
Cursor Up	01001110	4Eh	
Cursor Down	01001111	4Fh	
Cursor Write	01000110	46h	
Cursor Read	01000111	47h	
Memory Write	01000010	42h	
Memory Read	01000011	43h	
Erase	01010010	52h	
Sleep	01010011	53h	

68 (Series Timing Diagram)



CONTROL COMMAND DESCRIPTION

SYSTEM SET (C:40H)

Symbol	D7	D6	D5	D4	D3	D2	D1	D0	Description
P1	0	0	IV	1	0	M2	M1	M0	Mode of Operation
	M0	0: Inte							
	M1:				l or CG naracter				
					naracter	-			
	M2:					'charac s/chara			
	IV:	0: First				5/ 01 101 0	CICI		
					lly used	d)			
P2	WF	0	0	0	0	FX2	FX1	FX0	Width of a
	WF	0: Line				,			character field
	FXn				drive (lly used	1)	
	1 /11					3 pixels	wide)		
P3	0	0	0	0	FY3	FY2	FY1	FY0	Height of a
	FYn				ht of th				character field
P4		(norm	ally 01		sed for	8 pixei	s high)		Characters per row
P4	C/R:	To	tal nivl			/ided b	v FX		Characters per row
P5	0/10.	10			C/R	nucu b	<u>y 1 / </u>		Timing per character
-	T/C x	L/F x F	R x 9 =	Fosc					row (Adjust frame
		Lines			rtical pi	xels/sc	reen)		frequency)
	FR:					Hz to 80	OHz)		
	Fosc				CDC-13				
		6Mhz	(6 x 10	6) for I	built-in	contro	ller		
P6		L/F						Lines per graphics	
	L/F:	Ve	rtical p		er scree	en			screen
P7		Ν.			PL				Virtual screen low
D0	APL:	No	rmally		C/R+1	is used			byte
P8		N-	rmall		PH				Virtual screen high
	APH:	NO	rmally	uun is	usea				byte

DISPLAY	ON(C:59h)
---------	------------------

Symbol	D7	D6	D5	D4	D3	D2	D1	D0	Note
P1	FP5	FP4	FP3	FP2	FP1	FP0	FC1	FC0	
	FC1	FC0		Curso	or Conti	rol			
	0	0		Curso	or off				
	0	1		Curso	or on, n	o blink			
	1	1		On w					
	1	1		On w	ith 1 Hz	ı blink ı			
	FP1	FP0		SAD1	(L1)	Layer 1			
	FP3	FP2	22 SAD2 (L2)						Layer 2
	FP5	FP4		SADE	(L3)		Layer 3		
	0	0		Layer	off				
	0	1		Layer	on, no	blink			
	1	0		On w	ith 2 Hz	z blink i	rate		
	1	1		On w	ith 16 F	lz blink	rate		

DISPLAY OFF (C:58h)

This command causes the controller to inhibit the display of all enabled layers. The function of the paramater P1 that follows is the same as Display On.

OVERLAY (C:5BH)

This command controls the plane interrelations defined by the following parameter byte. Options include or, xor, intersection, and priority overlay.

Symbol	D7	D6	D5	D4	D3	D2	D1	D0	Note
P1	0	0	0	0V	DM1	DM0	MX1	MX0	
	MX1	MX0		Metho	od of O	verlay			
	0	0		L1 U	L2 U L	Simple	e Overlay		
	0	1		(L1 €) L2) U	L3		Revers	se Overlay
	1	0		(L1 🔿	n L2) U	Selective Overlay			
	1	1	1 L1 > L2 > L3						y Overlay
	DM0	0: SA	D1 defi	ned as	charac		The second		
		1: SA	D1 defi	ned as	graphi		layer can be		
	DM1	0: SA	D3 defi	ned as	charac		used as		
		1: SA	1: SAD3 defined as graphic layer						graphic
	0V	0: Cor	nfigure	d for 2	layers				layer only
		1: Coi	nfigure	d for 3	layers				

CG RAM ADDRESS (C:5Ch)

The parameters of this command define the base address of a memory character generator table. (Normally F000h is used.)

P1 (SAGL): Sets the lower byte of the CG RAM address P2 (SAGH): Sets the higher byte of the CG RAM address

This command is not needed if the internal CG ROM is used. It is needed if an external CG RAM is used. A memory

block of 2K or 4K bytes is required for vertical dot sizes of 8 or 16 respectively (depends on M2 of System Set command).

SCROLL (C:44h)

The SCROLL command is used to set the beginning display address of each layer and the number of lines in that layer. By modifying the beginning address of the last year, the screen may be made to scroll up or down.

P1 (SAD1L):	Sets the lower byte of the first layer address
P2 (SAD1H):	Sets the higher byte of the first layer address
P3 (SL1):	Sets the line number per frame for the first layer
P4 (SAD2L):	Sets the lower byte of the second layer address
P5 (SAD2H):	Sets the higher byte of the second layer address
P6 (SL2):	Sets the line number per frame for the second layer
P7 (SAD3L):	Sets the lower byte of the third layer address
P8 (SAD3H):	Sets the higher byte of the third layer address

HORIZ. DOT SCROLL (C:5Ah)

This command allows the screen to be scrolled by pixel increments. When used in conjunction with the Scroll command, smooth scrolling of the screen is possible. The number of pixels to offset by is passed in the parameter byte as follows:

P1: 0 0 0 0 0 D₂ D₁ D₀

CURSOR FORMAT (C:5Dh)

The va	riab	le si	ze b	lock	and	unde	erline	e cui	rsor can be set.
P1:	0	0	0	0	0	D_2	D1	D٥	Cursor width
P2:	0	0	0	0	D₃	D_2	D_1	D_0	Cursor height
CM:	•	Unde Bloci	erline k						

CURSOR CONTROL

The CURSOR CONTROL commands are used to set the default cursor direction which points to the location to be modified. After every memory read or memory write 1 operation, the cursor is automatically positioned to the next memory location.

citiony location.	
Cursor Right:	(C:4Ch - 01001100)
Cursor Left:	(C:4Dh - 01001101)
Cursor Up:	(C:4Eh - 01001110)
Cursor Down:	(C:4Fh - 01001111)

CURSOR WRITE (C:46h)

This comm	and sets the current cursor address.
P1 (CSRL):	Sets the lower byte of the cursor address
P2 (CSRH):	Sets the higher byte of the cursor address

CURSOR READ (C:47h)

This command returns the current cursor address.

P1 (CSRL):Reads the lower byte of the cursor addressP2 (CSRH):Reads the higher byte of the cursor address

MEMORY WRITE (42h)

This command sets the controller into the write mode. The data that is passed to the parameter will be written to the memory location specified by the current cursor address. After the Memory Write command, the controller automatically advances the cursor to the next sequential location defined by the cursor direction. This allows the users to write many bytes of data to the screen without issuing another write command.



MEMORY READ (43h)

This command sets the controller into the read mode. The data that is read from the parameter will be from the memory locaiton specified by the current cursor address. After the Memory Read command, the controller automatically advances the cursor to the next sequential location defined by the cursor direction. This allows the users to read many bytes of data to the screen without issuing another read command.



ERASE (C:52h)

This command clears the screens that are enabled from the current cursor position to the end of the screens. After Erase command is issued, two frame time (min.) delay is needed before issuing the next command (e.g., 34 ms is needed for 60 Hz frame frequency).

SLEEP (C:53h)

This command turns off the display, stops all internal operations, stops the oscillator, and enters the sleep mode. The controller may be brought out of the sleep mode by issuing the System Set command. The contents in the memory remain unchanged.

Command	Symbol	G121C	G191C	G242C	G2436	G321D	G321E G324E	G648D G649E	Note
System Set	С	40h	40h	40h	40h	40h	40h	40h	
	P1	30h	30h	30h	30h	30h	30h	30h	P5 is
	P2	87h	85h	85h	85h	87h	87h	87h	based on
	P3	07h	07h	07h	07h	07h	07h	07h	70 Hz
	P4	0Fh	1 Fh	27h	27h	27h	27h	4Fh	frame
	P5	7Ch	7Ch	7Ch	F8h	4Fh	42h	4Fh	rate with
	P6	7Fh	7Fh	7Fh	3Fh	C7h	Efh	C7h	$F_{OSC} =$
	P7	0Fh	1 Fh	27h	27h	27h	27h	4Fh	10 MHz
	P8	00h	00h	00h	00h	00h	00h	00h	
Display On	С	59h	59h	59h	59h	59h	59h	59h	
	P1	05h	05h	05h	05h	05h	05h	05h	
Overlay	С	5Bh	5Bh	5Bh	5Bh	5Bh	5Bh	5Bh	
	P1	00h	00h	00h	00h	00h	00h	00h	
Scroll	С	44h	44h	44h	44h	44h	44h	44h	
	P1	00h	00h	00h	00h	00h	00h	00h	
	P2	00h	00h	00h	00h	00h	00h	00h	
	P3	7Fh	7Fh	7Fh	3Fh	C7h	EFh	C7h	
	P4	00h	00h	00h	00h	00h	00h	00h	
	P5	04h	04h	06h	04h	08h	10h	10h	
	P6	7Fh	7Fh	7Fh	3Fh	C7h	EfFh	C7h	
Cursor Format	С	5Dh	5Dh	5Dh	5Dh	5Dh	5Dh	5Dh	
	P1	07h	05h	05h	05h	07h	07h	07h	
	P2	87h	87h	87h	87h	87h	87h	87h	
Cursor Write	С	46h	46h	46h	46h	46h	46h	46h	
	P1	00h	00h	00h	00h	00h	00h	00h	
	PC	00h	00h	00h	00h	00h	00h	00h	
Cursor Direction	С	4Ch	4Ch	4Ch	4Ch	4Ch	4Ch	4Ch	
Memory Write	С	42h	42h	42h	42h	42h	42h	42h	
	P1 -	ASCII Code:	20h - 7Fh						
	Pn	ASCII Code:	20h - 7Fh						

INITIALIZATION SETTINGS FOR SEIKO INSTRUMENTS LCD MODULES