## Applications

- Repeaters
- BTS Transceivers
- BTS High Power Amplifiers
- CDMA / WCDMA / LTE
- General Purpose Wireless


## Product Features

- $400-4000 \mathrm{MHz}$
- $\quad+29.5 \mathrm{dBm}$ P1dB
- $\quad+45 \mathrm{dBm}$ Output IP3
- 16.5 dB Gain @ 2140 MHz
- +5 V Single Supply, 235 mA Current
- Internal RF overdrive protection
- Internal DC overvoltage protection
- On chip ESD protection
- Capable of handling 10:1 VSWR @ 5Vcc, 2.14 GHz, 29.5 dBm CW Pout or 20 dBm WCDMA Pout
- SOT-89 Package


## General Description

The TQP7M9103 is a high linearity driver amplifier in industry standard, RoHS compliant, SOT-89 surface mount package. This InGaP/GaAs HBT delivers high performance across a broad range of frequencies with +45 dBm OIP3 and +29.5 dBm P1dB while only consuming 235 mA quiescent current. All devices are $100 \% \mathrm{RF}$ and DC tested.

The TQP7M9103 incorporates on-chip features that differentiate it from other products in the market. The amplifier integrates an on-chip DC over-voltage and RF over-drive protection. This protects the amplifier from electrical DC voltage surges and high input RF input power levels that may occur in a system.

The TQP7M9103 is targeted for use as a driver amplifier in wireless infrastructure where high linearity, medium power, and high efficiency are required. The device an excellent candidate for transceiver line cards and high power amplifiers in current and next generation multicarrier 3G / 4G base stations.


3-pin SOT-89 Package
Functional Block Diagram


Pin Configuration

| Pin \# | Symbol |
| :--- | :--- |
| 1 | RF Input |
| 3 | RF Output / Vcc |
| 2,4 | Ground |

## Ordering Information

| Part No. | Description |
| :--- | :--- |
| TQP7M9103 | 1 W High Linearity Amplifier |
| TQP7M9103-PCB900 | TQP7M9103 920-960MHz EVB |
| TQP7M9103-PCB2140 | TQP7M9103 2.11-2.17GHz EVB |

Standard T/R size $=1000$ pieces on a 7 " reel.

## Specifications

| Absolute Maximum Ratings |  |
| :--- | :--- |
| Parameter Rating <br> Storage Temperature -65 to $+150^{\circ} \mathrm{C}$ <br> Device Voltage, $\mathrm{V}_{\mathrm{cc}}$ +8 V <br> Maximum Input Power, CW +30 dBm |  |

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

| Parameter | Min | Typ |  | Max |  | Units |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{cc}}$ |  | +5 | +5.25 | V |  |  |
| $\mathrm{~T}_{\text {case }}$ | -40 |  | +85 | ${ }^{\circ} \mathrm{C}$ |  |  |
| Tj (for $>10^{6}$ hours MTTF) |  |  | 160 | ${ }^{\circ} \mathrm{C}$ |  |  |

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

## Electrical Specifications

Test conditions unless otherwise noted: $+25^{\circ} \mathrm{C},+5 \mathrm{~V}$ Vsupply, $50 \Omega$ system, tuned application circuit

| Parameter | Conditions | Min | Typical | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Operational Frequency Range |  | 400 |  | 4000 | MHz |
| Test Frequency |  |  | 2140 |  | MHz |
| Gain |  |  | 16.6 |  | dB |
| Input Return Loss |  |  | 12.0 |  | dB |
| Output Return Loss |  |  | 15.0 |  | dB |
| Output P1dB |  |  | +29.1 |  | dBm |
| Output IP3 | See Note 1. |  | +45 |  | dBm |
| WCDMA Pout @ - 50 dBc ACLR | See Note 2. |  | +20 |  | dBm |
| Noise Figure |  |  | 4.4 |  | dB |
| Vcc |  |  | +5 |  | V |
| Quiescent Current, Icq |  |  | 235 |  | mA |
| Thermal Resistance (jnc to case) $\theta_{\mathrm{jc}}$ |  |  |  | 35.6 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

Notes

1. OIP3 measured with two tones at an output power of $+15 \mathrm{dBm} /$ tone separated by 1 MHz . The suppression on the largest IM3 product is used to calculate the OIP3 using 2:1 rule.
2. ACLR Test set-up: 3GPP WCDMA, TM1 $+64 \mathrm{DPCH},+5 \mathrm{MHz}$ offset, $\mathrm{PAR}=10.2 \mathrm{~dB}$ at $0.01 \%$ Prob.

## Device Characterization Data




Note: The gain for the unmatched device in 50 ohm system is shown as the trace in red color, [gain $(\mathrm{S}(21)$ ]. For a tuned circuit for a particular frequency, it is expected that actual gain will be higher, up to the maximum stable gain. The maximum stable gain is shown in the black [Gain (MAX)]. The impedance plots are shown from $0.01-4 \mathrm{GHz}$.

## S-Parameter Data

$\mathrm{V}_{\mathrm{cc}}=+5 \mathrm{~V}, \mathrm{I}_{\mathrm{cq}}=235 \mathrm{~mA}, \mathrm{~T}=+25^{\circ} \mathrm{C}$, unmatched 50 ohm system, calibrated to device leads

| Freq <br> $(\mathbf{M H z})$ | $\mathbf{S 1 1}(\mathbf{d B})$ | $\mathbf{S 1 1}(\mathbf{a n g})$ | $\mathbf{S 2 1 ( d B )}$ | $\mathbf{S} 21(\mathbf{a n g})$ | $\mathbf{S 1 2}(\mathbf{d B})$ | $\mathbf{S 1 2}(\mathbf{a n g})$ | $\mathbf{S 2 2}(\mathbf{d B})$ | $\mathbf{S 2 2}(\mathbf{a n g})$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 50 | -1.05 | 179.35 | 15.75 | 154.01 | -35.54 | -2.51 | -2.94 | -171.04 |
| 100 | -1.15 | 176.19 | 13.33 | 155.93 | -35.54 | -9.63 | -2.28 | -176.20 |
| 200 | -2.07 | 171.50 | 11.63 | 168.26 | -37.45 | -27.07 | -2.00 | 176.45 |
| 400 | -1.01 | -176.54 | 15.01 | 153.46 | -36.02 | 22.73 | -3.38 | 172.64 |
| 600 | -0.61 | 173.92 | 13.87 | 137.55 | -35.08 | 6.61 | -3.21 | 171.33 |
| 800 | -0.59 | 169.36 | 13.05 | 125.26 | -34.89 | 0.27 | -3.18 | 168.76 |
| 1000 | -0.62 | 164.62 | 12.35 | 114.05 | -34.56 | -4.24 | -3.13 | 166.33 |
| 1200 | -0.62 | 160.93 | 11.51 | 103.77 | -34.60 | -7.64 | -3.21 | 164.22 |
| 1400 | -0.67 | 156.67 | 10.73 | 94.67 | -34.79 | -12.27 | -3.18 | 162.12 |
| 1600 | -0.64 | 153.26 | 10.00 | 86.25 | -34.75 | -15.00 | -3.21 | 159.50 |
| 1800 | -0.75 | 149.43 | 9.12 | 78.19 | -34.75 | -17.78 | -3.25 | 156.37 |
| 2000 | -0.64 | 145.77 | 8.50 | 70.63 | -34.81 | -20.08 | -3.09 | 154.32 |
| 2200 | -0.62 | 142.62 | 7.90 | 63.72 | -34.51 | -23.77 | -3.24 | 151.96 |
| 2400 | -0.77 | 139.07 | 7.16 | 57.32 | -34.72 | -26.63 | -3.10 | 148.69 |
| 2600 | -0.66 | 135.41 | 6.58 | 51.13 | -34.60 | -29.04 | -3.07 | 147.12 |
| 2800 | -0.73 | 132.81 | 6.04 | 45.43 | -34.65 | -33.24 | -3.16 | 144.43 |
| 3000 | -0.69 | 128.99 | 5.51 | 39.41 | -34.51 | -33.49 | -3.09 | 141.32 |
| 3200 | -0.74 | 125.72 | 5.01 | 33.18 | -34.65 | -34.26 | -3.12 | 138.96 |
| 3400 | -0.74 | 122.13 | 4.52 | 27.44 | -34.60 | -37.56 | -3.09 | 136.12 |
| 3600 | -0.72 | 119.18 | 4.02 | 22.42 | -34.56 | -43.68 | -3.13 | 133.54 |
| 3800 | -0.77 | 116.00 | 3.52 | 16.74 | -34.37 | -44.96 | -3.04 | 130.91 |
| 4000 | -0.80 | 113.01 | 3.15 | 11.74 | -34.33 | -46.26 | -2.96 | 128.69 |

## Application Circuit 920-960 MHz (TQP7M9103-PCB900)



Notes:

1. See PC Board Layout, page 8 for more information.
2. Components shown on the silkscreen but not on the schematic are not used.
3. $0 \Omega$ resistor (B1) may be replaced with copper trace in the target application layout.
4. The recommended component values are dependent upon the frequency of operation.
5. All components are of 0603 size unless stated on the schematic.
6. Critical component placement locations:

Distance from U1 Pin 1 (left edge) to Z1 (right edge): 365 mils Distance from U1 Pin 3 (right edge) to Z5 (left edge): 130 mils
Distance from U1 Pin 3 (right edge) to Z6 (left edge): 250 mils

## Bill of Material

| Ref Des | Value | Description | Manuf. | Part Number |
| :---: | :---: | :---: | :---: | :---: |
| n/a | n/a | Printed Circuit Board | TriQuint | 1080068 |
| U1 | n/a | TQP7M9103 Amplifier, SOT-89 pkg. | TriQuint | TQP7M9103 |
| Z1 | 3.9 pF | Cap., Chip, 0603, $\pm 0.05 \mathrm{pF}, 50 \mathrm{~V}$, Accu-P | AVX | 06035J3R9ABSTR |
| Z2,B1 | $0 \Omega$ | Resistor, Chip, 0603, 5\%, 1/16W | various |  |
| Z5 | 2.2 nH | Inductor, 0603, $\pm 0.3 \mathrm{nH}$ | Toko | LL1608-FSL2N2S |
| Z6 | 4.7 pF | Cap., Chip, 0603, $\pm 0.05 \mathrm{pF}, 50 \mathrm{~V}$, Accu-P | AVX | 06035J4R7ABSTR |
| Z7 | 3.3 pF | Cap., Chip, 0603, $\pm 0.05 \mathrm{pF}, 50 \mathrm{~V}$, Accu-P | AVX | 06035J3R3ABSTR |
| Z8, C3 | 100 pF | Cap., Chip, 0603, 5\%, 50V, NPO/COG | various |  |
| L1 | 33 nH | Inductor, 0805, 5\%, Coilcraft CS Series | Coilcraft | 0805CS-330XJLB |
| C4 | $1.0 \mu \mathrm{~F}$ | Cap., Chip, 0603, 10\%, 10V, X5R | various |  |
| C7 | $0.1 \mu \mathrm{~F}$ | Cap., Chip, 0603, 50V, X5R | various |  |

IW High Linearity Amplifier

## Typical Performance $920-960 \mathrm{MHz}$

| Frequency | $\mathbf{M H z}$ |  | $\mathbf{9 2 0}$ | $\mathbf{9 4 0}$ |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Gain | dB | 20.6 | 20.7 | 20.8 |  |  |
| Input Return Loss | dB | -10.0 | -10.8 | -10.8 |  |  |
| Output Return Loss | dB | -19.4 | -20.4 | -22.5 |  |  |
| Output P1dB | dBm | +29.5 | +29.4 | +29.5 |  |  |
| Output IP3 (+19 dBm/tone, $\Delta \mathrm{f}=1 \mathrm{MHz})$ | dBm | +46.7 | +45.4 | +44.0 |  |  |
| WCDMA Channel power (at 50 dBc ACLR) $[1]$ | dBm | +20 | +20 | +20 |  |  |
| Noise Figure | dB | 5.8 | 5.8 | 5.8 |  |  |
| Supply Voltage, Vcc | V |  | +5 |  |  |  |
| Quiescent Collector Current, Icq | mA |  | 235 |  |  |  |

Notes:

1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, $\mathrm{PAR}=10.2 \mathrm{~dB}$ at $0.01 \%$ Prob.

RF Performance Plots 920-960 MHz


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## Application Circuit 2110-2170 MHz (TQP7M9103-PCB2140)



Notes:

1. See PC Board Layout, page 8 for more information.
2. Components shown on the silkscreen but not on the schematic are not used.
3. $0 \Omega$ resistors (Z7,B1) may be replaced with copper trace in the target application layout.
4. The recommended component values are dependent upon the frequency of operation.
5. All components are of 0603 size unless stated on the schematic.
6. Critical component placement locations:

Distance from U1 Pin 1 (left edge) to Z2 (right edge): 130 mils Distance from U1 Pin 1 (left edge) to Z3 (right edge): 40 mils Distance from U1 Pin 3 (right edge) to Z4 (left edge): 40 mils Distance from U1 Pin 3 (right edge) to Z6 (left edge): 250 mils

## Bill of Material

| Ref Des | Value | Description | Manuf. | Part Number |
| :---: | :---: | :---: | :---: | :---: |
| n/a | n/a | Printed Circuit Board | TriQuint | 1080068 |
| U1 | n/a | TQP7M9103 Amplifier, SOT-89 pkg. | TriQuint | TQP7M9103 |
| Z2,Z3 | 1.5 pF | Cap., Chip, 0603, $\pm 0.1$ pF. 200V. NPO/COG | AVX | 06032U1R5BAT2A |
| Z4 | 1.2 pF | Cap., Chip, 0603, $\pm 0.1$ pF. 200V. NPO/COG | AVX | 06035J1R2ABSTR |
| Z5,B1,Z7 | $0 \Omega$ | Resistor, Chip, 0603, 5\%, 1/16W | various |  |
| Z6 | 0.6 pF | Cap., Chip, 0603, $\pm 0.05 \mathrm{pF}, 50 \mathrm{~V}$, Accu-P | AVX | 06035J0R6ABSTR |
| C3,Z8 | 22 pF | Cap., Chip, 5\%, 50V, NPO/COG | various |  |
| L1 | 33 nH | Inductor, 0805, 5\%, Coilcraft CS Series | Coilcraft | 0805CS-330XJLB |
| C4 | $1.0 \mu \mathrm{~F}$ | Cap., Chip, 0603, 10\%, 10V, X5R | various |  |
| C7 | $0.1 \mu \mathrm{~F}$ | Cap., Chip, 0603, 50V, X5R | various |  |

IW High Linearity Amplifier

## Typical Performance 2110-2170 MHz

| Frequency | $\mathbf{M H z}$ |  | $\mathbf{2 1 1 0}$ | $\mathbf{2 1 4 0}$ |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathbf{2 1 7 0}$ |  |  |  |  |  |  |
| Gain | dB | 16.7 | 16.6 | 16.6 |  |  |
| Input Return Loss | dB | -11.7 | -12.0 | -11.7 |  |  |
| Output Return Loss | dB | -15.2 | -15.0 | -14.9 |  |  |
| Output P1dB | dBm | +29.1 | +29.1 | +29.2 |  |  |
| Output IP3 $(+15$ dBm/tone, $\Delta \mathrm{f}=1 \mathrm{MHz})$ | dBm | +45.0 | +45.0 | +45.0 |  |  |
| WCDMA Channel power $($ at -50 dBc ACLR $)[1]$ | dBm | +20 | +20 | +20 |  |  |
| Noise Figure | dB | 4.4 | 4.4 | 4.6 |  |  |
| Supply Voltage, Vcc | V |  | +5 |  |  |  |
| Quiescent Collector Current, Icq | mA |  | 235 |  |  |  |

Notes:

1. ACLR Test set-up: 3GPP WCDMA, TM1 $+64 \mathrm{DPCH},+5 \mathrm{MHz}$ offset, $\mathrm{PAR}=10.2 \mathrm{~dB}$ at $0.01 \%$ Prob.

RF Performance Plots 2110-2170 MHz










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## Pin Configuration and Description



| Pin | Symbol | Description |
| :--- | :--- | :--- |
| 1 | RF IN | RF Input. Requires external match for optimal performance. External DC Block <br> required. |
| 2,4 | GND | RF/DC Ground Connection |
| 3 | RFout / Vcc | RF Output. Requires external match for optimal performance. External DC Block <br> and supply voltage is required. |

## Applications Information

## PC Board Layout

PCB Material (stackup):
1 oz . Cu top layer
0.014 inch Nelco N-4000-13, $\varepsilon_{\mathrm{r}}=3.7$

1 oz . Cu MIDDLE layer 1
Core Nelco N-4000-13
1 oz . Cu middle layer 2
0.014 inch Nelco N-4000-13

1 oz . Cu bottom layer
Finished board thickness is $0.062 \pm .006$
50 ohm line dimensions: width $=.031$ ", spacing $=.035 \prime$ "
The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary
 from supplier to supplier, careful process development is recommended.

## Mechanical Information

## Package Information and Dimensions

This package is lead-free/RoHScompliant. The plating material on the leads is NiPdAu. It is compatible with both lead-free (maximum $260{ }^{\circ} \mathrm{C}$ reflow temperature) and lead (maximum $245^{\circ} \mathrm{C}$ reflow temperature) soldering processes.


The component will be marked with a "7M9103" designator with an alphanumeric lot code on the top surface of package.


## Mounting Configuration

All dimensions are in millimeters (inches). Angles are in degrees.


Notes:

1. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35 mm ( $\# 80 / .0135$ ") diameter drill and have a final plated thru diameter of $.25 \mathrm{~mm}\left(.010^{\prime \prime}\right)$.
2. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
3. RF trace width depends upon the PC board material and construction.
4. Use 1 oz . Copper minimum.

## Product Compliance Information

## ESD Information



## Gaution! ESD-Sensitive Device

ESD Rating: Class 2

Value: $\quad \geq 2000 \mathrm{~V}$ and $<4000 \mathrm{~V}$
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114
ESD Rating: Class IV
Value: $\quad \geq 2000$ V min
Test: $\quad$ Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

## MSL Rating

Level 3 at $+260^{\circ} \mathrm{C}$ convection reflow The part is rated Moisture Sensitivity Level 3 at $260^{\circ} \mathrm{C}$ per JEDEC standard IPC/JEDEC J-STD-020.

## Solderability

Compatible with the latest version of J-STD-020, Lead free solder, $260^{\circ}$

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A $\left(\mathrm{C}_{15} \mathrm{H}_{12} \mathrm{Br}_{4} \mathrm{O}_{2}\right)$ Free
- PFOS Free
- SVHC Free


## Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

$$
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