

Ring Generator Controller IC

Features

- ▶ 3.3V operation, logic inputs 3.3V & 5.0V compatible
- ▶ Digital control of ring frequency, amplitude, and offset
- ▶ Control via 8-bit bus or via individual inputs
- ▶ 8 built-in ring frequencies: 12, 16²/₃, 20, 25, 33¹/₃, 40, 50, 60Hz
- ▶ External ring frequency input
- ▶ Low distortion sine wave synthesizer
- ▶ AC-only, AC+DC, or DC-only ringer output
- ▶ Adjustable over-current protection
- ▶ Internal precision voltage references
- ▶ Power-on reset and undervoltage lockout for hotswap capability
- ▶ Sync output with adjustable lead time for synchronizing ringing relays
- ▶ Fault output for problem detection
- ▶ Open or closed loop operation
- ▶ Efficient 4-quadrant operation
- ▶ Zero-cross turn-on with zero-cross turn-off option

Applications

- ▶ PBX
- ▶ DLC
- ▶ Key Systems
- ▶ Remote Terminal
- ▶ Wireless Loop Systems

General Description

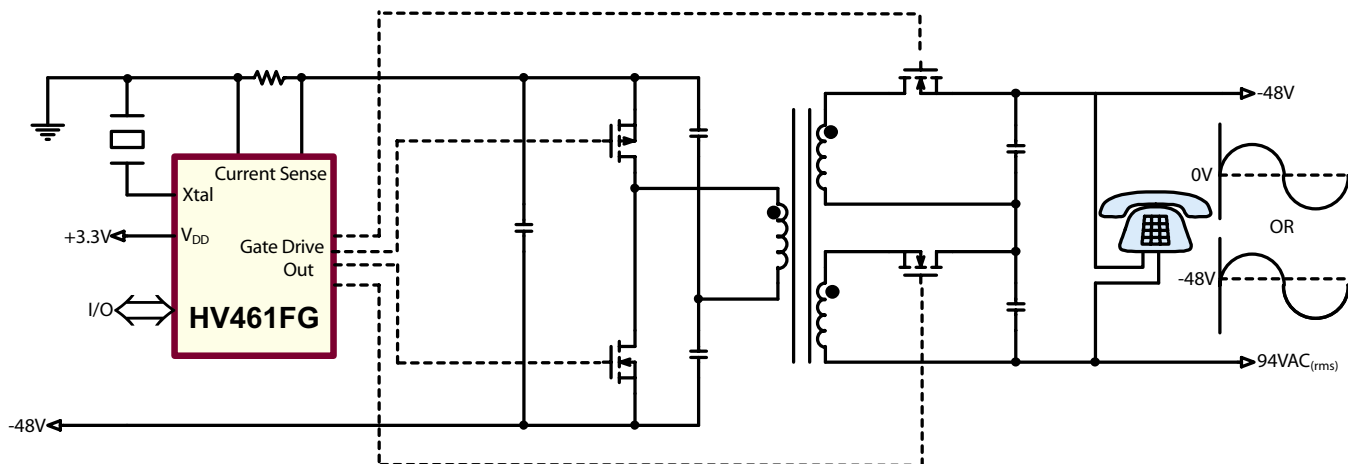
The HV461FG is a highly integrated ring generator controller IC, designed to work with a patented four-quadrant inverter topology, with synchronous rectifiers on the secondary side to achieve higher efficiencies. The inverter delivers the desired ring voltage from a standard -48V Telecom power supply.

The HV461 consists of a sine wave synthesizer that can provide eight different ring frequencies for universal applications. Any other frequency in the 12 to 63Hz range can be obtained by applying an external logic signal to the IC. A transparent latch permits control of the ringer output individually or through the 8-bit bus. The output amplitude and DC offset can be digitally controlled providing high flexibility to the designers. The patented inverter topology using the HV461 controller IC is capable of achieving higher efficiencies, typically over 80%, and drive up to a 40 REN load.

The controller allows ring generators to provide a floating 94VAC (rms) waveform that can be referenced to either the -48V or any other offset level by using the programmable offset pins of the IC. Output offset may be achieved by directly generating the offset within the power stage, or by floating the output stage on a DC source, or both.

The HV461 also has an internal boost converter that can be used to provide the gate drive voltages for the two MOSFETS on the primary side and the two secondary rectifiers on the secondary side.

Typical Application Circuit



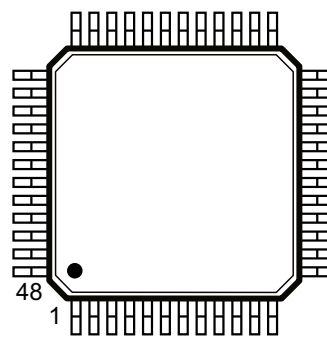
Ordering Information

| Device | Package Option |
|--------|--|
| | 48-Lead LQFP 7.00x7.00mm body 1.6mm height (max) 0.50mm pitch |
| HV461 | HV461FG-G |

-G indicates package is RoHS compliant ('Green')

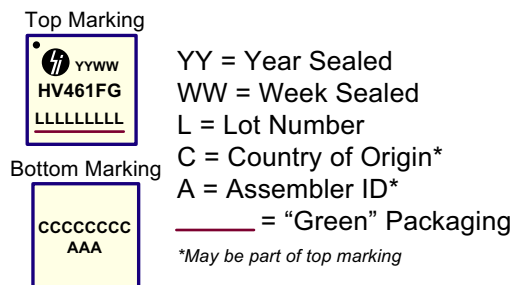


Pin Configuration



48-Lead LQFP (FG)
(top view)

Product Marking



48-Lead LQFP (FG)

Absolute Maximum Ratings

| Parameter | Value |
|-----------------------|-----------------|
| V_{DD} | +4.0V |
| Digital inputs | -0.5V to +7.0V |
| Analog inputs | -0.5V to +7.0V |
| Storage temperature | -65°C to +150°C |
| Operating temperature | -40°C to +85°C |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Electrical Specifications (unless otherwise specified: $V_{DD} = 3.3V$, $T_A = -40^\circ C$ to $+85^\circ C$)

External Supply

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|----------|---|-----|-----|-----|-------|---|
| V_{DD} | Supply voltage | 3.0 | 3.3 | 3.6 | V | --- |
| I_{DD} | Supply current ($AV_{DD} + DV_{DD}$) | - | 7 | 30 | mA | $f_{PWM} = 100kHz$ $f_{osc} = 19.6608MHz$ SW outputs NC Open loop config, External V_{GD} |

Gate Drive Supply

| Sym | Parameter | Min | Typ | Max | | Conditions |
|--------------|---------------------------|----------------|-----|-----------|----------|--|
| V_{GD} | Boost circuit voltage | 9.0 | 9.6 | 10.2 | V | --- |
| I_{GD} | Gate drive supply current | - | - | 5.0 10 | mA mA | $V_{DD} = 2.97 - 3.63V$, SW outputs unloaded $V_{DD} = 2.50 - 2.93V$, SW outputs unloaded |
| $V_{DR(lo)}$ | Drive voltage, low | - | - | 0.2 | V | $I_{OUT} = -10\mu A$ |
| $V_{DR(hi)}$ | Drive voltage, hi | $V_{DD} - 0.4$ | - | - | V | $I_{OUT} = 10\mu A$ |
| t_{RISE} | Rise time | - | - | 100 | ns | $C_L = 200pF$ |
| t_{FALL} | Fall time | - | - | 100 | ns | $C_L = 200pF$ |
| f_{GD} | Converter frequency | same as PWM | | | | --- |
| D_{GD} | Duty cycle | 45 | 50 | 55 | % | --- |

Voltage Reference

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|-------------------|-------------------------|-------|-------|-------|------------------------------|---------------------------------------|
| V_{REF1} | Reference voltage 1 | 1.213 | 1.250 | 1.288 | V | $T_a = 25^\circ\text{C}$ |
| TC_{REF1} | Temperature coefficient | - | 200 | - | $\mu\text{V}/^\circ\text{C}$ | --- |
| ΔV_{ref1} | Output regulation | -6.25 | - | +6.25 | mV | $I_{out} = \pm 100\mu\text{A}$ |
| V_{REF2} | Reference voltage 2 | 2.425 | 2.500 | 2.575 | V | $T_A = 25^\circ\text{C}$ |
| TC_{REF2} | Temperature coefficient | - | 500 | - | $\mu\text{V}/^\circ\text{C}$ | --- |
| ΔV_{ref2} | Output regulation | -12.5 | - | 0 | mV | $I_{out} = 0 - 100\mu\text{A source}$ |

Logic Inputs

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|--------------|--------------------|--------------------|-----|--------------------|---------------|------------------------|
| $V_{IN(lo)}$ | Input voltage low | - | - | $0.3 \cdot V_{DD}$ | V | --- |
| $V_{IN(hi)}$ | Input voltage high | $0.7 \cdot V_{DD}$ | - | - | V | --- |
| $I_{IN(lo)}$ | Input current low | - | - | -1 | μA | $V_{IN} = 0\text{V}$ |
| $I_{IN(hi)}$ | Input current high | - | - | 1 | μA | $V_{IN} = 5.0\text{V}$ |
| C_{IN} | Input capacitance | - | - | 10 | pF | --- |
| t_S | Set-up time | - | - | 100 | ns | --- |
| t_H | Hold time | - | - | 100 | ns | --- |

Reset

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|------------------|-----------------------|-------|-------|-------|---------------|------------|
| $V_{RESET(ON)}$ | RESET on voltage | 1.200 | 1.325 | 1.450 | V | --- |
| $V_{RESET(OFF)}$ | RESET off voltage | 1.000 | 1.125 | 1.250 | V | --- |
| $V_{RESET(HYS)}$ | RESET hysteresis | 0.150 | 0.200 | 0.250 | V | --- |
| I_{P-UP} | RESET pull-up current | 7.0 | 10.0 | 13.0 | μA | --- |

Undervoltage Lockout

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|---------------|----------------------|-----------------------------------|------|------|-------|------------|
| $V_{DD(ON)}$ | V_{DD} on voltage | 2.75 | 2.85 | 2.95 | V | --- |
| $V_{DD(OFF)}$ | V_{DD} off voltage | 2.50 | - | - | V | --- |
| $V_{DD(HYS)}$ | V_{DD} hysteresis | - | 0.10 | - | V | --- |
| $V_{GD(ON)}$ | V_{GD} on voltage | same as V_{GD} regulation point | | | V | --- |
| $V_{GD(OFF)}$ | V_{GD} off voltage | 7.0 | - | - | V | --- |
| $V_{GD(HYS)}$ | V_{GD} hysteresis | 0.20 | - | - | V | --- |

Fault Output

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|--------------------------|---------------------|-----|-----|-----|-------|---------------------------|
| V _{OUT(lo)} | Output voltage low | - | - | 0.2 | V | I _{OUT} = 1mA |
| K _{FAULT(on)} | FAULT on threshold | 6 | 8 | 10 | %* | C _{FAULT} = 10μF |
| K _{FAULT(off)} | FAULT off threshold | 1 | 2 | 3 | %* | C _{FAULT} = 10μF |
| t _{FAULT(hold)} | FAULT hold time | 50 | - | - | mS | C _{FAULT} = 10μF |

* Percent of time PWM overrange or overcurrent is active.

Amplifiers

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|-----------------------|------------------------------|----------------------|----------------------|------|-------|--|
| V _{IN} | Input range | 0.25 | - | 2.50 | V | --- |
| I _{IN} | Input bias current | -500 | - | 500 | nA | V _{IN} = 0.5V to V _{DD} -0.5 |
| V _{OFFSET} | Input offset voltage | -15 | - | 15 | mV | --- |
| V _{OUT(min)} | Min output | - | 0.1 | 0.2 | V | I _{OUT} = ±100uA |
| V _{OUT(max)} | Max output | V _{DD} -0.2 | V _{DD} -0.1 | - | | I _{OUT} = ±100uA |
| A _{VOL} | Open loop gain | 60 | 80 | - | dB | --- |
| CMRR | Common mode rejection ratio | -40 | -60 | - | dB | --- |
| GBW | Gain-bandwidth product | 1.0 | - | - | MHz | --- |
| SL | Slew rate | 0.1 | - | - | V/μs | --- |
| PSRR | Power supply rejection ratio | -30 | - | - | dB | f<10kHz |

Sinewave Synthesizer

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|------------------|---------------------|--------------|--------------|--------------|--------------------------------------|--|
| V _{DC} | DC level | 1.213 | 1.250 | 1.288 | V | --- |
| A | Amplitude | 1.900 | 2.000 | 2.100 0 | V _{P-P} V _{P-P} | AMP ≠ 00 AMP = 00 |
| f ₀ | Frequency | - | 16 2/3 | - | Hz | FREQ = 000, f _{OSC} = 19.6608MHz |
| f ₁ | Frequency | - | 20 | - | Hz | FREQ = 001, f _{OSC} = 19.6608MHz |
| f ₂ | Frequency | - | 25 | - | Hz | FREQ = 010, f _{OSC} = 19.6608MHz |
| f ₃ | Frequency | - | 30 | - | Hz | FREQ = 011, f _{OSC} = 19.6608MHz |
| f ₄ | Frequency | - | 33 1/3 | - | Hz | FREQ = 100, f _{OSC} = 19.6608MHz |
| f ₅ | Frequency | - | 40 | - | Hz | FREQ = 101, f _{OSC} = 19.6608MHz |
| f ₆ | Frequency | - | 50 | - | Hz | FREQ = 110, f _{OSC} = 19.6608MHz |
| f ₇ | Frequency | - | 60 | - | Hz | FREQ = 111, f _{OSC} = 19.6608MHz |
| Δf | Frequency accuracy | - | - | 0.1 | % | f _{OSC} = 19.6608MHz |
| THD | Harmonic distortion | - | - | 3 | % | C _{SINE} = 33nF f _{ring} = 16 2/3 to 60Hz |
| R _{OUT} | Output resistance | 14.4 72.0 | 16.0 80.0 | 17.6 88.0 | kΩ kΩ | AMP ≠ 00 AMP = 00 |

External Ring Frequency

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|-----------------------|----------------------------|--------------------|-----|----------------|-------|---|
| $f_{CAP(lo)}$ | Capture frequency low* | - | 12 | - | Hz | loop filter = (33 μ F+10k Ω) 4.7 μ F |
| $f_{CAP(hi)}$ | Capture frequency high* | - | 63 | - | Hz | loop filter = (33 μ F+10k Ω) 4.7 μ F |
| $V_{IN(lo)}$ | Input low | - | - | 0.3 - V_{DD} | V | --- |
| $V_{IN(hi)}$ | Input high | 0.7 $\cdot V_{DD}$ | - | - | V | --- |
| $\Delta\theta_{RING}$ | Phase jitter, sine ref out | -5 | - | +5 | deg | loop filter = (33 μ F+10k Ω) 4.7 μ F |

* Lock range is the same as capture range

Sine Reference Attenuator

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|-----------|-------------|-------|-------|----------------|-------|-----------------------|
| V_{DC} | DC level | 1.213 | 1.250 | 1.288 | V | $V_{IN(DC)} = 1.250V$ |
| A_{OFF} | Attenuation | - | - | 0.010 | V/V | AMP = 00 |
| A_{LO} | Attenuation | 0.490 | 0.500 | 0.510 | V/V | AMP = 01 |
| A_{MED} | Attenuation | 0.735 | 0.750 | 0.765 | V/V | AMP = 10 |
| A_{HI} | Attenuation | 0.980 | 1.000 | 1.020 | V/V | AMP = 11 |
| V_{IN} | Input range | 0.2 | - | $V_{DD} - 0.2$ | V | --- |

DC REF Multiplexer

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|-----------|---------------------|------|-----|----------|---------|-----------------------------------|
| V_{IN} | Input range | 0.0 | - | V_{DD} | V | --- |
| I_{IN} | Input bias current | -500 | - | +500 | nA | --- |
| I_{OFF} | Off leakage current | - | - | 1.0 | μ A | $V_{IN} = 0.5$ to $V_{DD} - 0.5V$ |

Enable and SYNC

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|------------------|--------------------------|----------------|-----|---------|--------------------------|--|
| $V_{OUT(lo)}$ | SYNC output voltage low | - | - | 0.2 | V | $I_{OUT} = 1.0mA$ sink |
| $V_{OUT(hi)}$ | SYNC output voltage high | $V_{DD} - 0.2$ | - | - | V | $I_{OUT} = 1.0mA$ source |
| t_{ON} | ENABLE delay, on | - | - | 5 | μ s | --- |
| t_{OFF} | ENABLE delay, off | 0 | - | 60 1 | μ s ring cycle | SYNCMODE = 0 SYNCMODE = 1 |
| $T_{SYNC(ON)}$ | SYNC on lead time | 4.5 | 5.0 | 5.5 | ms | $C_{SINE} = 0$ $R_{SYNC} = 154k\Omega$ $C_{SYNC} = 47nF$ |
| $T_{SYNC(OFF)}$ | SYNC off delay | -250 | 0 | +250 | μ s | $C_{SINE} = 10nF$ |
| $t_{SYNC(rise)}$ | SYNC rise time | - | - | 300 | ns | $C_L = 50pF$ |
| $t_{SYNC(fall)}$ | SYNC fall time | - | - | 300 | ns | $C_L = 50pF$ |

PWM Controller

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|-----|-----------|-----|-----|-----|-------|------------|
|-----|-----------|-----|-----|-----|-------|------------|

PWM Frequency

| | | | | | | |
|---------------------------|--------------------------------|----------------|----------------|----------------|---------------|---|
| f_{PWM} | PWM frequency | 21.25 127.5 | 25.00 150.0 | 28.75 172.5 | kHz kHz | $R_{\text{PWM}} = 500\text{k}\Omega$ $R_{\text{PWM}} = 83\text{k}\Omega$ |
| $t_{\text{PWMSYNC(OUT)}}$ | PWM sync output pulse width | 30 | 50 | 70 | ns | --- |
| $t_{\text{PWMSYNC(IN)}}$ | PWM sync input pulse width | 25 | - | - | ns | --- |
| $f_{\text{PWMSYNC(IN)}}$ | PWM sync input frequency range | 25 | - | 150 | kHz | --- |
| $V_{\text{PWMSYNC(lo)}}$ | PWM sync output low voltage | - | - | 0.2 | V | $I_{\text{OUT}} = 1.0\text{mA sink}$ |
| I_{PWMSYNC} | PWM sync pull-up current | - | 100 | - | μA | --- |

Switch Driver Outputs

| | | | | | | |
|----------------------|----------------------|-----------------------|---|-----|----|---------------------------------------|
| $V_{\text{OUT(lo)}}$ | Output voltage, low | - | - | 0.2 | V | $I_{\text{OUT}} = 20\text{mA sink}$ |
| $V_{\text{OUT(hi)}}$ | Output voltage, high | $V_{\text{GD}} - 0.2$ | - | - | V | $I_{\text{OUT}} = 20\text{mA source}$ |
| t_{RISE} | Rise time | - | - | 50 | ns | $C_{\text{L}} = 4\text{nF}$ |
| t_{FALL} | Fall time | - | - | 50 | ns | $C_{\text{L}} = 4\text{nF}$ |

Timing

| | | | | | | |
|--------------------|--------------------------------|----------------------|----------------------|----------------------|---------------------|--|
| D | Duty cycle | 23 48 73 | 25 50 75 | 27 52 77 | % % % | $\text{PWM}_{\text{IN}} = 0.625\text{V}$ $\text{PWM}_{\text{IN}} = 1.250\text{V}$ $\text{PWM}_{\text{IN}} = 1.875\text{V}$ $V_{\text{DCL}} = 0\text{V}$ |
| D_{limit} | Duty cycle limit | 12 72 22 62 | 20 80 30 70 | 28 88 38 78 | % % % % | $V_{\text{DCL}} = 0.50\text{V}, \text{PWM}_{\text{IN}} = 0\text{V}$ $V_{\text{DCL}} = 0.50\text{V}, \text{PWM}_{\text{IN}} = 2.5\text{V}$ $V_{\text{DCL}} = 0.75\text{V}, \text{PWM}_{\text{IN}} = 0\text{V}$ $V_{\text{DCL}} = 0.75\text{V}, \text{PWM}_{\text{IN}} = 2.5\text{V}$ |
| I_{DCL} | V_{DCL} input current | - | - | 1.0 | μA | $V_{\text{DCL}} = 0 - 1.0\text{V}$ |
| t_{DB} | Primary switch deadband | 0 0.95 | 100 1.00 | 150 1.05 | ns μs | $C_{\text{DB}} = 0\text{pF}$ $R_{\text{DB}} = 14\text{k}\Omega, C_{\text{DB}} = 100\text{pF}$ |
| t_{DLY} | Secondary switch delay | 0 0.95 | 100 1.00 | 150 1.05 | ns μs | $C_{\text{DLY}} = 0\text{pF}$ $R_{\text{DLY}} = 14\text{k}\Omega, C_{\text{DLY}} = 100\text{pF}$ |

Switch Outputs

| ENABLE | AMP | OFF | SW1 | SW2 | SW3 | SW4 |
|--------|-----|-----|-----------|-----------|-----------|-----------|
| 0 | 00 | XX | Off | Off | Off | Off |
| 0 | ≠00 | XX | Off | Off | Switching | Switching |
| 1 | XX | XX | Switching | Switching | Switching | Switching |

X = don't care, #00 = 01, 10, or 11

Figure 1: Switch Timing Diagram

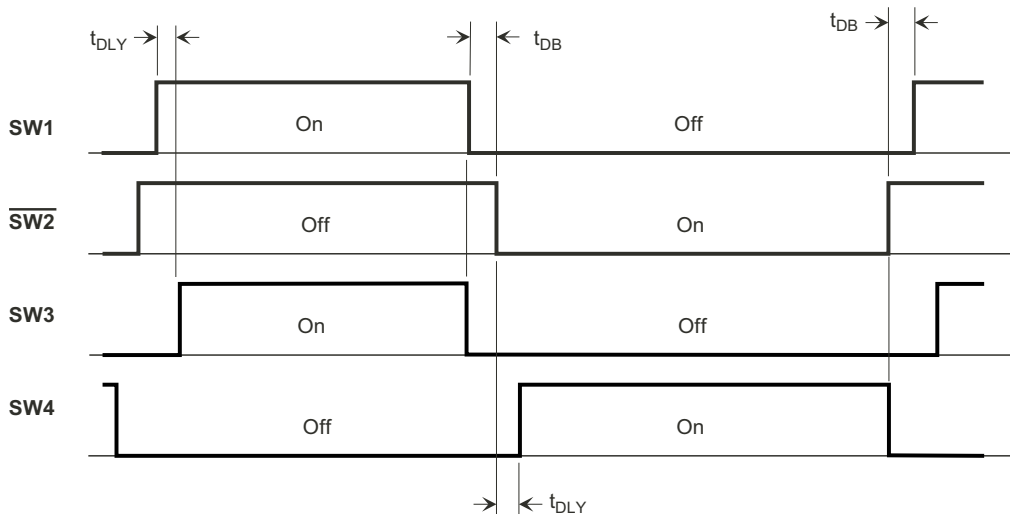


Figure 2: ENABLE and SYNC Timing - SYNCMODE = 0

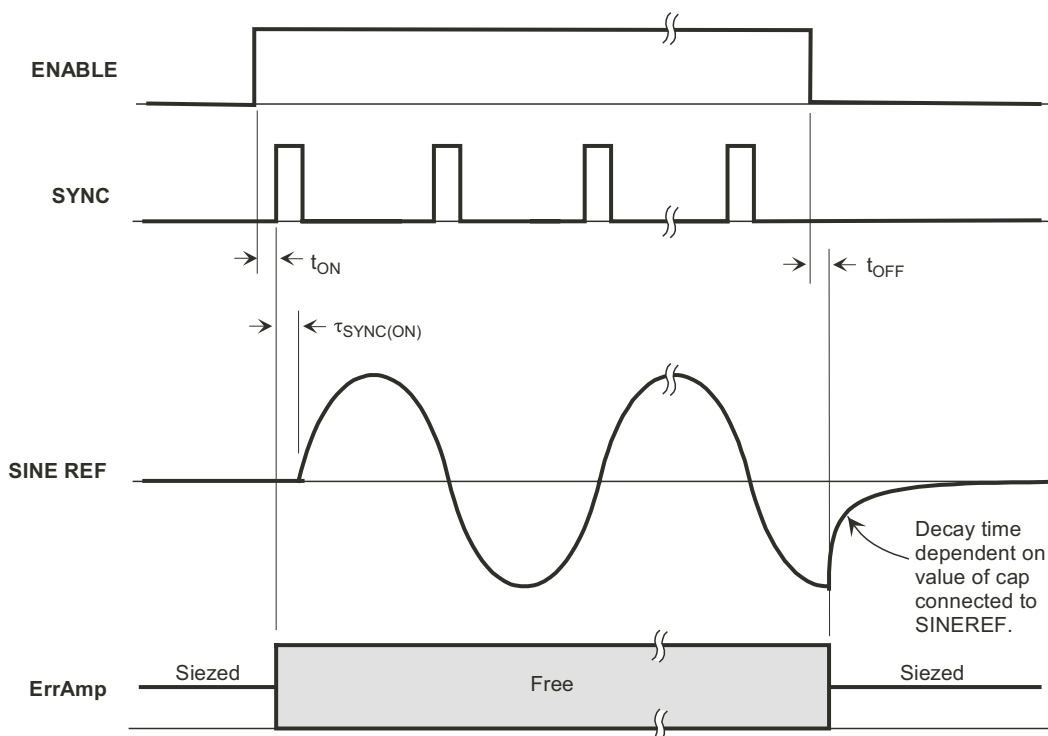


Figure 3: ENABLE and SYNC Timing - SYNCMODE = 1

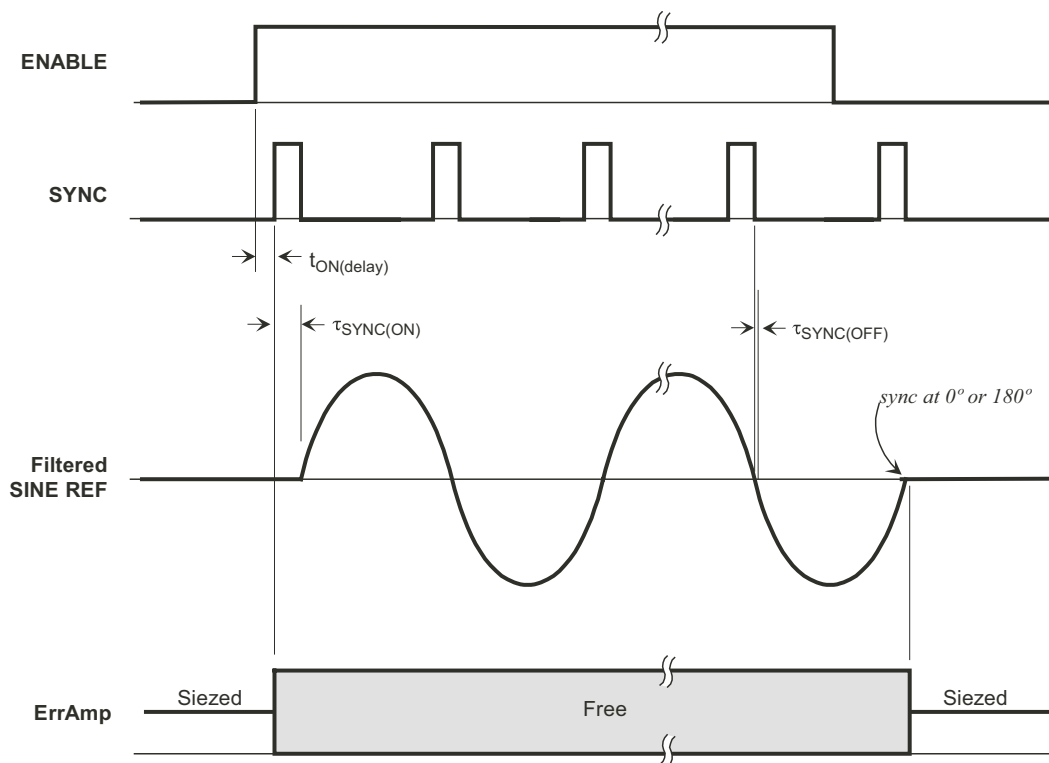
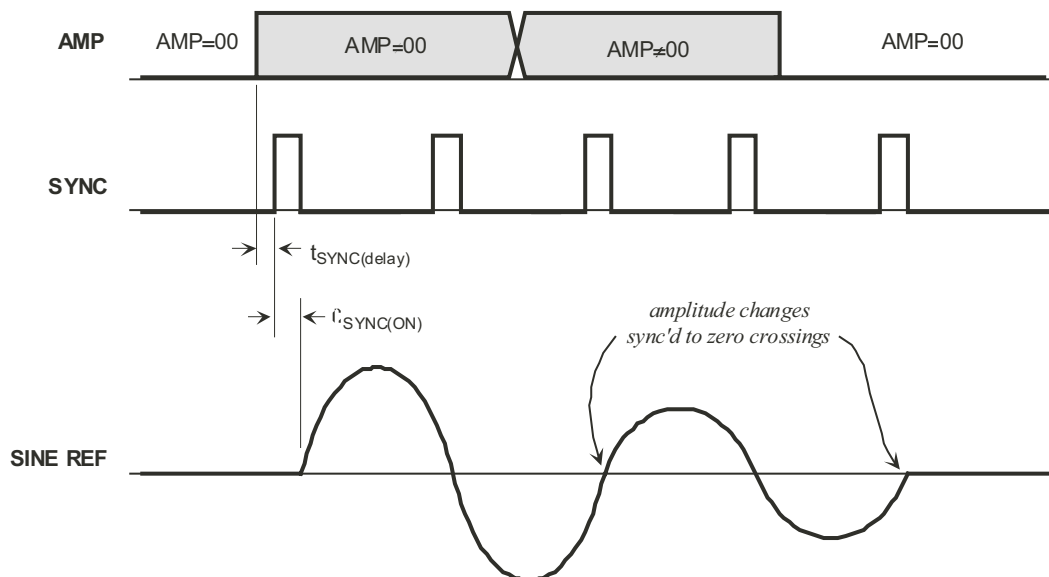


Figure 4: AMP Timing



Typical Application

Figures 5 and 6 on pages 9 and 10 show the schematic of a typical 15 REN ring generator application. The basic design equations for elements connected to different pins are given in the Pin Descriptions Table beginning on page 11.

Figure 5: Block Diagram and Typical Application Circuit

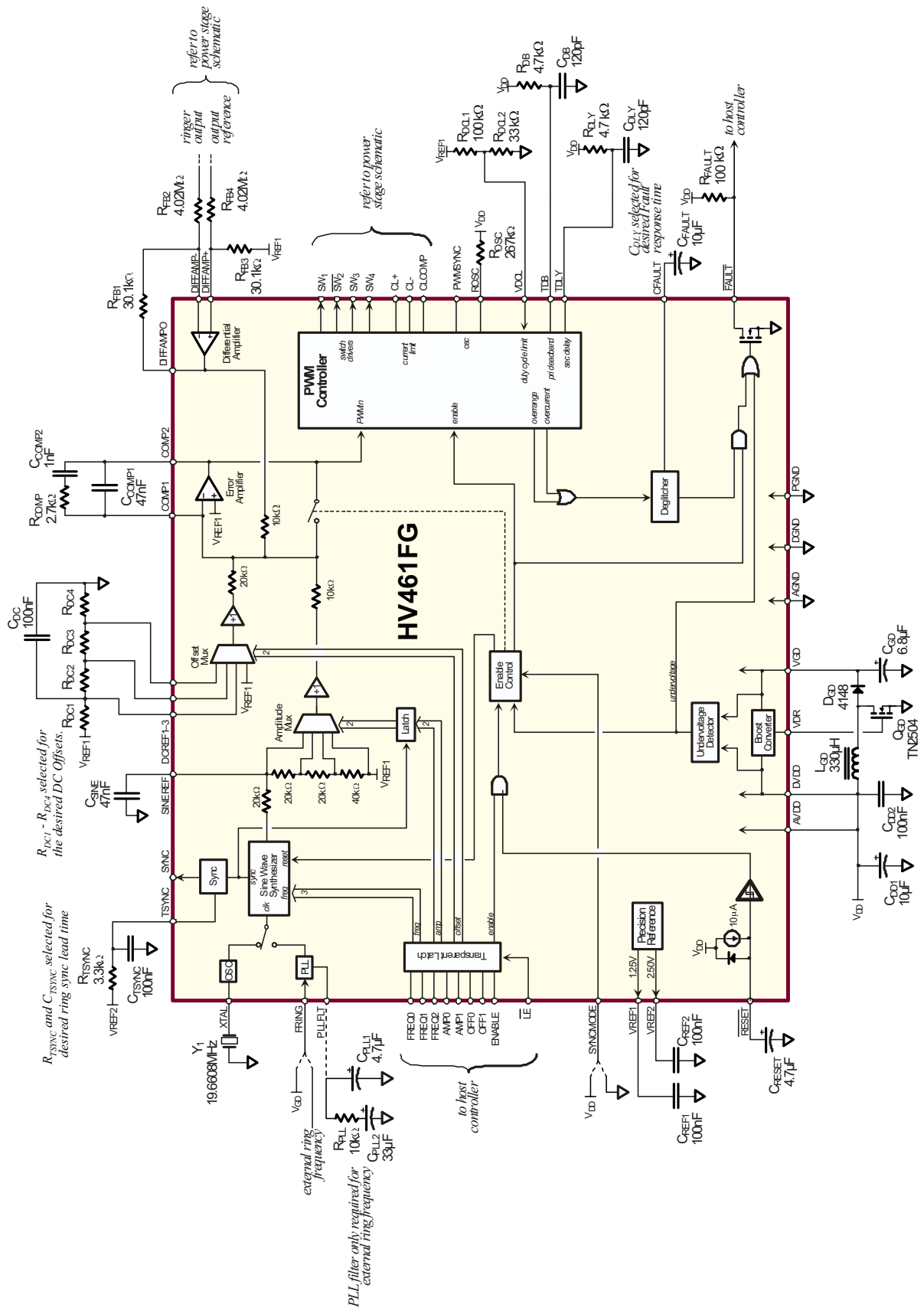
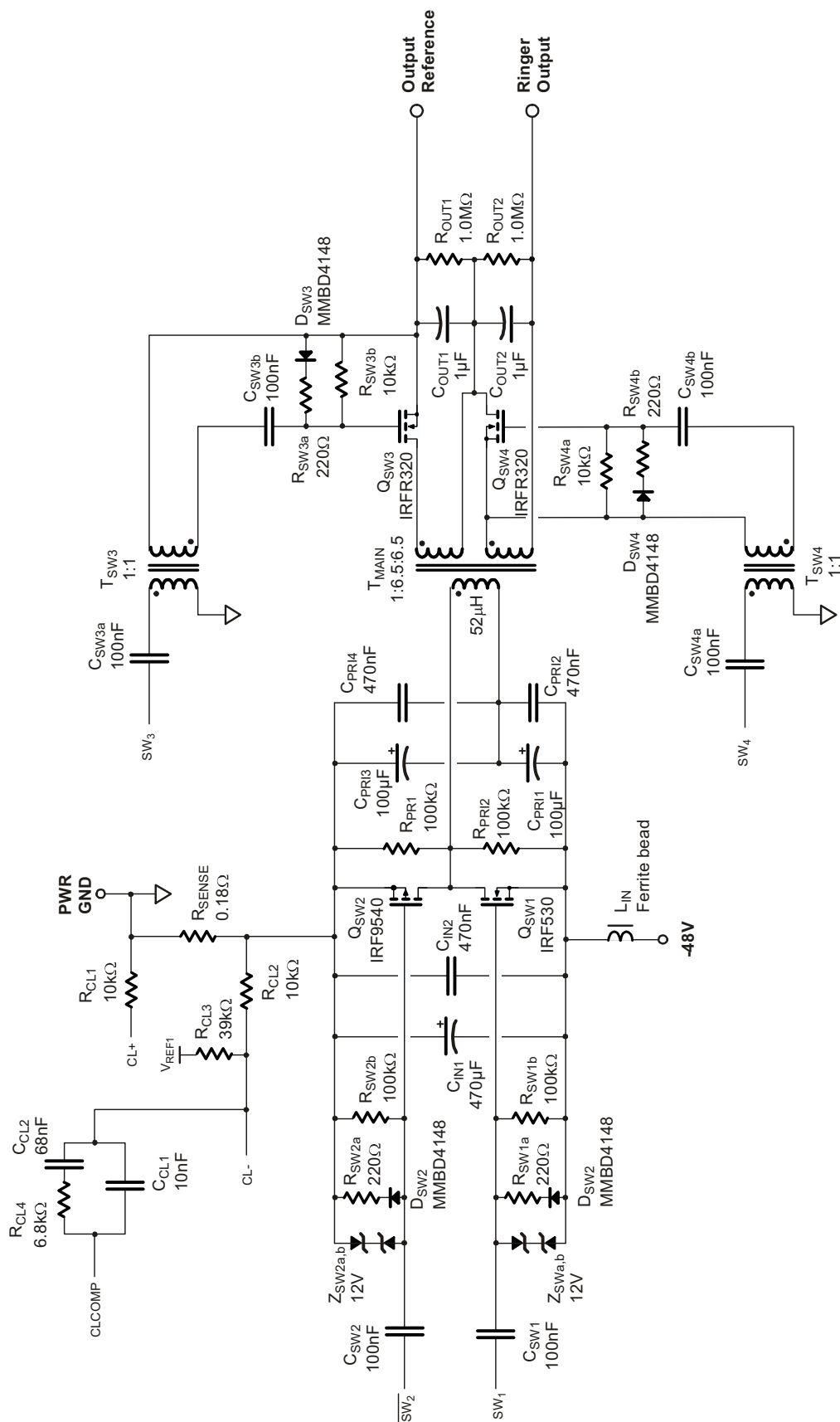


Figure 6: Typical Power Stage for 15 REN Ring Generator



Pin Description (refer to pin configuration on page 2)

| Pin | Name | Description |
|-----|---------------------------|--|
| 1 | DCREF3 | See DCREF1 and DCREF2 (pins 47 & 48). |
| 2 | VREF1 | Outputs a 1.25V nominal reference voltage. Bypass with a 100nF capacitor to ground. |
| 3 | VREF2 | Outputs a 2.50V nominal reference voltage. Bypass with a 100nF capacitor to ground. |
| 4 | AVDD | Supply for the analog section. 3.0 to 3.6V Must be from the same source as DVDD. Bypass with a 100nF capacitor to ground as close as possible to the IC. |
| 5 | TSYNC | An RC network connected to this pin determines the SYNC pulse lead time (see SYNC pin 14). $t_{LEAD} = 0.48RC$ If SYNC is not utilized, TSYNC must still have a connected RC network. |
| 6 | XTAL | A crystal from this pin to ground provides the frequency reference for the internal sine wave synthesizer. A 19.6608MHz baud rate crystal provides the 8 most common ring frequencies. The crystal is operated in the series mode. A loading capacitor is not necessary. See also FREQ0–2 (pins 21–23) and FRING (pin 7). |
| 7 | FRING | Ring frequency is normally selected from the 8 built-in frequencies using control inputs FREQ0–2. Other arbitrary frequencies in the range of 12 to 63Hz may be obtained by applying an external signal to FRING. This external signal sets the ring frequency at a 1:1 ratio. The ring signal remains a sine wave, with amplitude and offset still controlled via AMPx and OFFx. The ring signal, while frequency locked to the FRING signal, is not phase-synchronized to it. This allows the ring signal to immediately start at 0° when enabled via ENABLE or AMP ≠ 00. When unused, this input must be connected to VGD. |
| 8 | PLLFLT | Phase locked loop filter. An RC network connected to this pin stabilizes the PLL that locks on to the optional external ring frequency signal. (See FRING, pin 7) The RC network determines the lock time of the PLL. Due to the low frequencies involved, it may take a couple seconds to lock to the external signal. See the typical application schematic for typical values. When unused, this pin should be left unconnected. |
| 9 | ROSC | A resistor from this pin to VDD sets the PWM frequency. $f_{PWM} \approx 12.5GHz\Omega / R_{OSC}$ (valid for 20–150kHz) |
| 10 | $\overline{\text{RESET}}$ | A capacitor from this pin to ground provides a power-on reset interval. It has an internal 10μA pull-up to charge the external reset capacitor. Alternatively, an external logic-level or open-drain signal may be applied to implement the reset function. During the reset interval when $V_{RESET} < 1.325V$, the ringer output is disabled regardless of the state of the ENABLE input, allowing time for the host controller to assume control. Use a low leakage tantalum or ceramic capacitor. $t_{RESET} = 1.325V \cdot C_{RESET} / 10\mu A$ |
| 11 | PWMSYNC | This pin functions as both an input and an output. It is open-drain with an internal 100μA pull-up. As an output, it provides a short, low-going pulse at the internal PWM frequency. As an input, it synchronizes internal PWM frequency to the externally applied signal, provided the external signal is at a higher frequency. The low-going applied sync pulse should be between 25ns and less than the PWM period in duration. The external source should be open drain. If the PWMSYNC pins of multiple HV461s are tied together, their PWM frequencies will be phase-locked to the HV461 with the highest free-running frequency. A maximum of 10 HV461s may be tied together. If unused, this pin should be left unconnected. |
| 12 | CFAULT | A capacitor from this pin to ground sets the integration time of the FAULT detection circuitry. A larger capacitor provides less susceptibility to transient problems, while a smaller capacitor provides quicker response. Values in the range of 1μF to 100μF are appropriate. If the FAULT output is not used, this pin should be grounded. See also FAULT (pin 15). |

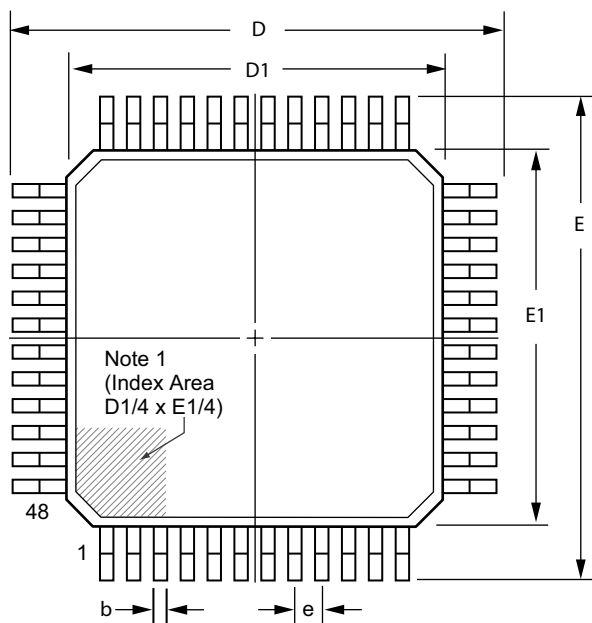
Pin Description (cont.)

| Pin | Name | Description |
|-----|---------------------------|---|
| 13 | SYNCMODE | With SYNCMODE low, ringer output ceases the instant ENABLE goes low. When high, ringer output ceases at the next ring signal phase crossing (0°/180°) after ENABLE goes low. |
| 14 | SYNC | Outputs a pulse indicating sine reference 0° and 180° phase crossing (not to be confused with zero-voltage crossing). The rising edge precedes phase crossing by a user-adjustable time period (see TSYNC pin 44). Falling edge coincides with sine reference phase crossing. SYNC is digitally derived, therefore phase shifts caused by the external filter capacitor at SINEREF will not be reflected at the SYNC output. |
| 15 | $\overline{\text{FAULT}}$ | Indicates abnormal operating conditions of output overcurrent, supply undervoltage (VDD & VGD), or PWM overrange (duty cycle limit – see VDCL, pin 3). Together, these 3 conditions catch most any problem. When an overcurrent or overrange condition exists for more than 8% of the time, this output becomes active. It is cleared when the problem occurs less than 2% of the time. Undervoltage conditions immediately activate the FAULT output. It is active low and open drain to allow wire-ORing. See CFAULT (pin 15) for additional information. |
| 16 | ENABLE | Ringer output enable. Active high. When enabled, the ring signal always starts immediately at 0 degrees. If AMP≠00, SW1 and SW2 are held off when ENABLE=0 but SW3 and SW4 continue switching. If AMP=00, SW3 and SW4 are held off as well. When disabled, the error amplifier is set at unity gain to prevent saturation, reducing turn-on glitches when re-enabled. See SYNCMODE (pin 13) for additional information. |
| 17 | OFF0 | Sets ring DC offset. Offset changes are effected at the next phase crossing (0°/180°) of the ring signal. Except for 00, offsets are set by the voltages at DCREf1–3. (OFF0 is LSB) Offset = $\frac{1}{2} \times \text{Gain} \times (V_{\text{DCREFx}} - V_{\text{REF1}})$ |
| 18 | OFF1 | 00 = 0V 01 = DCREf1 10 = DCREf2 11 = DCREf3 |
| 19 | AMP0 | Sets ring amplitude. Amplitude changes are effected at the next phase crossing (0°/180°) of the ring signal. Amplitudes, as a percentage of full scale, are: (AMP0 is LSB) |
| 20 | AMP1 | Full scale amplitude = $0.707V_{\text{RMS}} \times \text{Gain}$ 00 = 0% 01 = 50% 10 = 75% 11 = 100% |
| 21 | FREQ0 | Sets ring frequency. Frequency changes are effected at the next phase crossing (0°/180°) of the ring signal. |
| 22 | FREQ1 | Frequencies when using a 19.6608MHz crystal are: (FREQ0 is LSB) |
| 23 | FREQ2 | 000 = 16.7Hz 001 = 20Hz 010 = 25Hz 011 = 30Hz 100 = 33.3Hz 101 = 40Hz 110 = 50Hz 111 = 60Hz |
| 24 | $\overline{\text{LE}}$ | Latch enable. The latch gates control inputs FREQ0–2, AMP0–1, OFF0–1, and ENABLE. When LE is high, latch outputs follow inputs. On a low-going transition, outputs are latched. |
| 25 | TDLY | An RC network on this pin sets the primary to secondary switch delay. This prevents the secondary-side switches (SW3&4) from turning on prematurely. $t_{\text{DLY}} = 0.48\text{RC}$ |
| 26 | TDB | An RC network on this pin sets the deadband (break-before-make time) on the primary-side switches (SW1&2). Deadband prevents both switches from conducting simultaneously. $t_{\text{DB}} = 0.48\text{RC}$ |
| 27 | DGND | Digital ground. Connect to AGND and PGND close to the IC. |
| 28 | SW4 | Secondary-side switch driver output. |
| 29 | SW3 | Secondary-side switch driver output. |
| 30 | SW2 | Primary-side N-channel switch driver output. |

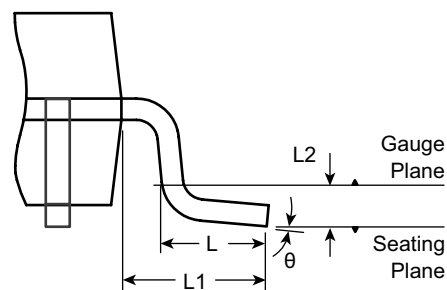
| Pin | Name | Description | |
|-----|----------|---|---|
| 31 | SW1 | Primary-side P-channel switch driver output. | |
| 32 | PGND | Power ground. Connect to AGND and DGND close to the IC. | |
| 33 | VGD | Supply for the SW1–4 drivers. An external boost converter controlled by VDR provides 9.6V for driving the power stage MOSFETs. An undervoltage condition on this supply pin disables ringer output and activates the FAULT output. | |
| 34 | VDR | Gate drive for the external boost converter circuit. Outputs a fixed 50% duty cycle at the ringer PWM frequency (see ROSC, pin 9). Output voltage regulation is via burp-mode operation. This output is bootstrapped to VGD, thus during startup VDR amplitude is VDD and after startup is VGD. (See VGD, pin 33) | |
| 35 | DVDD | Supply for the digital section. 3.0V to 3.6V input. Undervoltage disables ringer output. Must be from the same source as AVDD. Bypass with a 100nF capacitor to ground as close as possible to the IC. An undervoltage condition on this supply pin disables ringer output and activates the FAULT output. | |
| 36 | CL+ | Current limit amplifier non-inverting input. | |
| 37 | CL- | Current limit amplifier inverting input. | |
| 38 | CLCOMP | Current limit compensation. An RC network connected between this pin and CL- establishes current limit reaction time and stability. | |
| 39 | DIFFAMP+ | Differential amplifier non-inverting input. | <p>The differential amplifier sets gain, establishing output amplitude and DC offset in conjunction with AMPx and OFFx.</p> <p>Gain = R_{FB2}/R_{FB1} ($R_{FB3} = R_{FB1}$ and $R_{FB4} = R_{FB2}$, see schematic)</p> |
| 40 | DIFFAMP- | Differential amplifier inverting input. | |
| 41 | DIFFAMPO | Differential amplifier output. | |
| 42 | COMP2 | Error amplifier compensation. An RC network connected between these pins establishes loop stability. | |
| 43 | COMP1 | COMP1 is the error amp inverting input. COMP2 is the error amp output. | |
| 44 | SINEREF | Sine wave reference. Amplitude is $2V_{p,p}$ nominal. Output impedance is approximately 16kΩ. An external 33nF capacitor from this pin to ground should be employed to remove high frequency synthesizer ripple. Synthesizer ripple is at a frequency of $2^{15} \cdot f_{RING}$ | |
| 45 | AGND | Analog ground. Connect to AGND and DGND close to the IC. | |
| 46 | VDCL | Voltage applied to this pin sets the min/max duty cycle limits. If the PWM controller hits these limits, clipping of the ringer output will occur and the FAULT output will be activated. $D_{MIN} = 0.4V_{DCL}$ $D_{MAX} = 1 - 0.4V_{DCL}$ | |
| 47 | DCREF1 | In conjunction with the OFFx control inputs, voltages applied to these inputs set the output DC offset. Output offset is the selected DCREFx voltage multiplied by gain. See also OFF0 & OFF1 (pins 17 & 18) | |
| 48 | DCREF2 | | |

48-Lead LQFP Package Outline (FG)

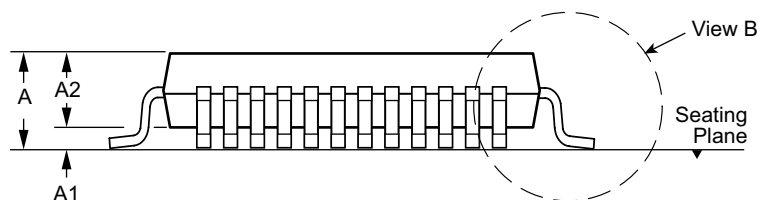
7.00x7.00mm body, 1.60mm height (max), 0.50mm pitch



Top View



View B



Side View

Note:
 1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 Identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

| Symbol | A | A1 | A2 | b | D | D1 | E | E1 | e | L | L1 | L2 | θ | |
|----------------|-----|-------|------|------|------|-------|-------|-------|-------|----------|------|----------|----------|----|
| Dimension (mm) | MIN | 1.40* | 0.05 | 1.35 | 0.17 | 8.80* | 6.80* | 8.80* | 6.80* | 0.50 BSC | 0.45 | 1.00 REF | 0.25 BSC | 0° |
| | NOM | - | - | 1.40 | 0.22 | 9.00 | 7.00 | 9.00 | 7.00 | | 0.60 | | 3.5° | |
| | MAX | 1.60 | 0.15 | 1.45 | 0.27 | 9.20* | 7.20* | 9.20* | 7.20* | | 0.75 | | 7° | |

JEDEC Registration MS-026, Variation BBC, Issue D, Jan. 2001.

* This dimension is not specified in the original JEDEC drawing. The value listed is for reference only.

Drawings are not to scale.

Supertex Doc. #: DSPD-48LQFPFG Version, B090808.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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