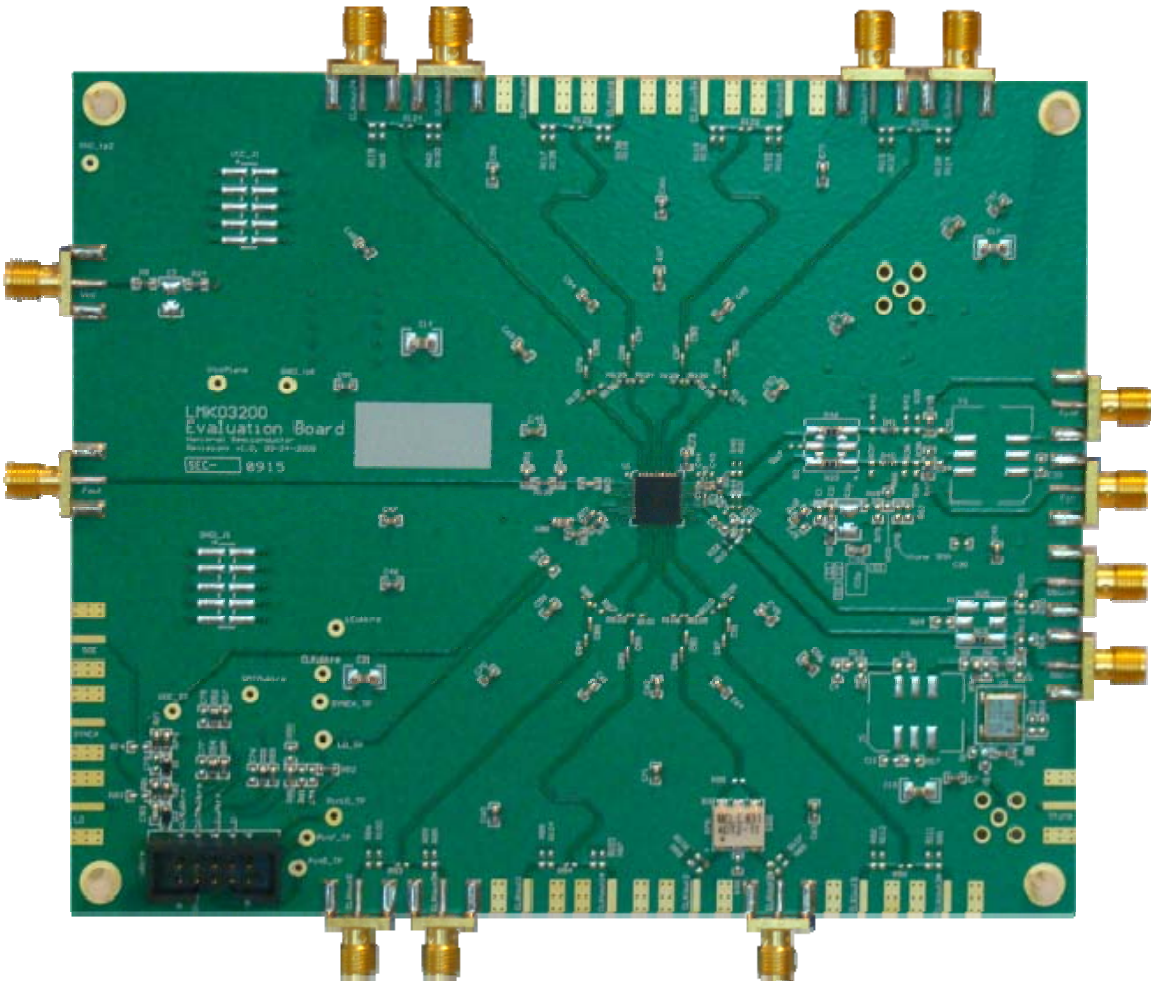
National Semiconductor

LMK03200

Precision Clock Conditioner with Integrated VCO
Evaluation Board Operating Instructions

6-16-2009



National Semiconductor Corporation
Interface

2900 Semiconductor Dr.
MS A2-600
Santa Clara, CA, 95052-8090

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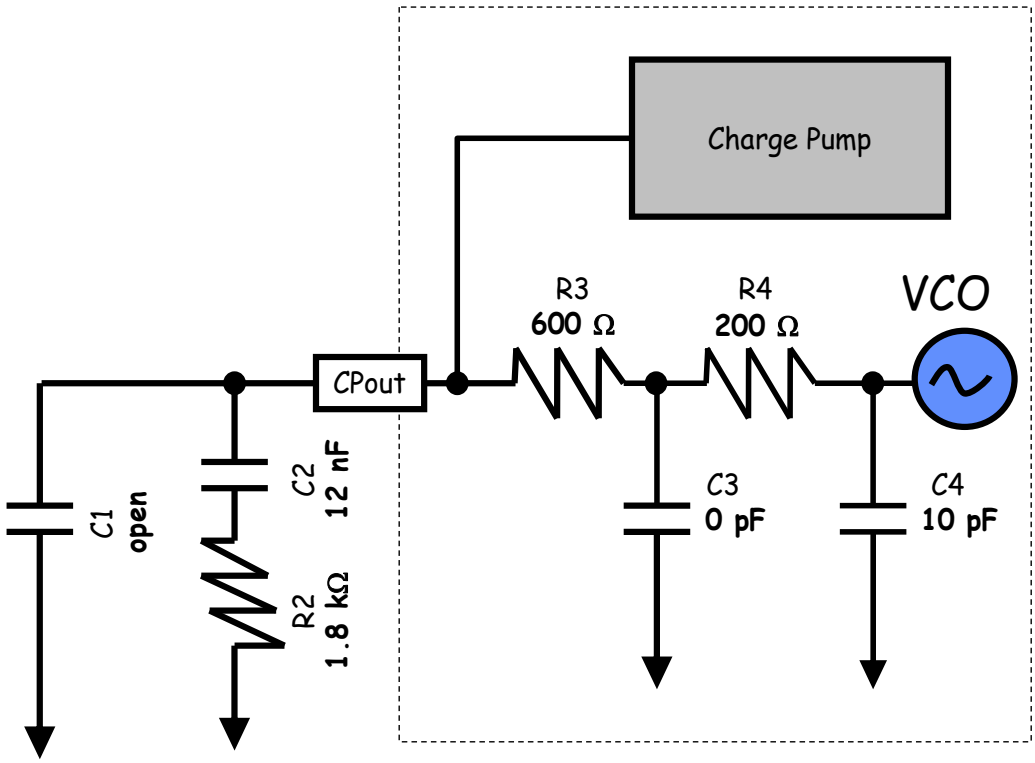
General Description

The LMK03200 Evaluation Board simplifies evaluation of the LMK03200 Precision Clock Conditioner with Integrated VCO. The package consists of an evaluation board and CodeLoader software. The *CodeLoader* software will run on a Windows 2000 or Windows XP PC. The purpose of the *CodeLoader* software is to program the internal registers of the LMK03200 device through a MICROWIRE™ interface.

CodeLoader 4 can be downloaded from: http://www.national.com/timing/software/

Loop Filter #1			
Phase Margin	82.2º	**Kϕ**	3200 uA
Loop Bandwidth	57.7 kHz	**f_{PD}**	9.72 MHz
Crystal Frequency	19.44 MHz	**Output Frequency**	1185 to 1296 MHz
Supply Voltage	3.3 Volts	**VCO Gain**	8 MHz/Volt



Loop filter #1 is selected by placing a 0 ohm resistor on pad R69.

This loop filter has been designed for optimal RMS jitter using a low noise reference.

Read first, Basic Operation

First install the CodeLoader 4 software. This can be downloaded from:
http://www.national.com/timing/software/

For basic operation…

1. Connect a low noise **3.3 V** power supply to the **Vcc** connector located at the top left of the board

2. Connect the CodeLoader cable to the **uWire** header located in the lower left.

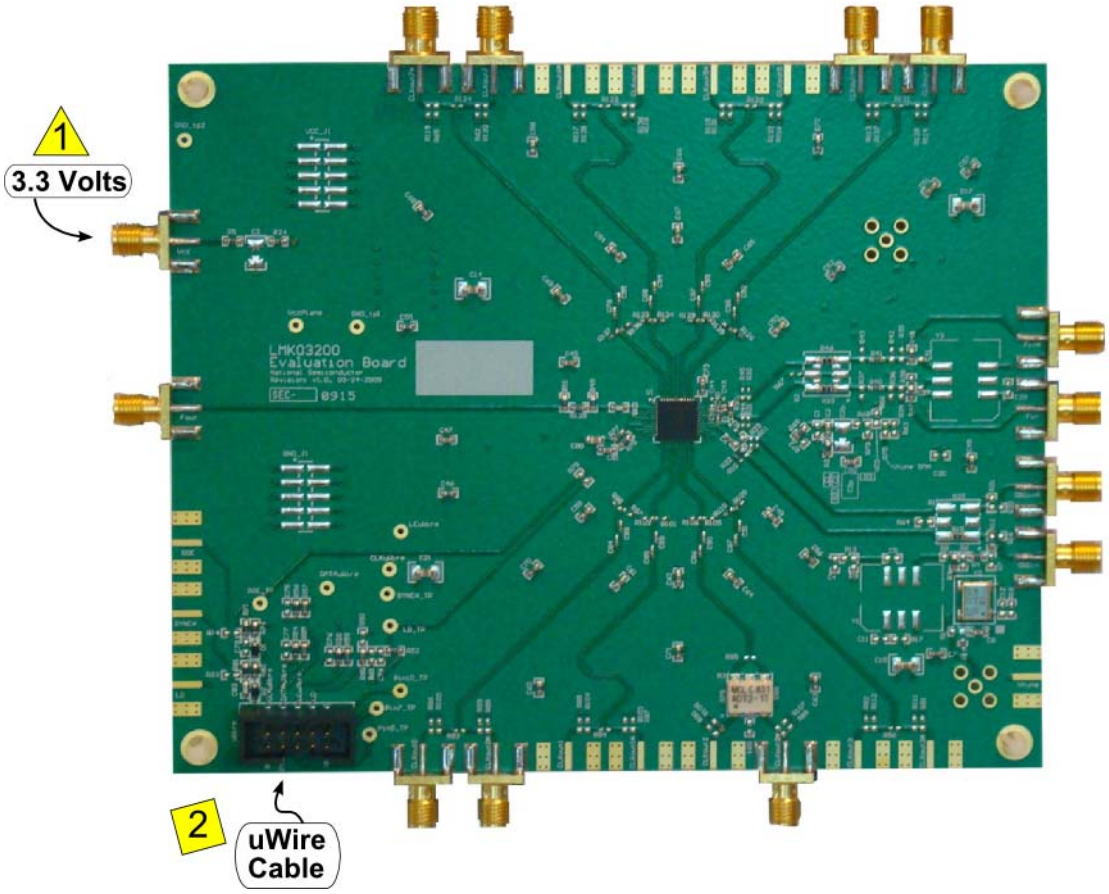


Figure 1 - Basic power and communication connections

Read first, Basic Operation (Continued)

3. Connect…
   - PC directly to the evaluation board with the LPT to uWire cable, plugging the cable into an LPT port on the computer and then the 10 pin ribbon connector to the evaluation board. This setup is shown below. **The cable can be removed after programming to minimize noise and EMI.**

   or

   - Available separately, the USB <--> uWire board to the PC with the USB cable and the USB <--> uWire board to the evaluation board with the 10 pin ribbon cable.

LPT Setup

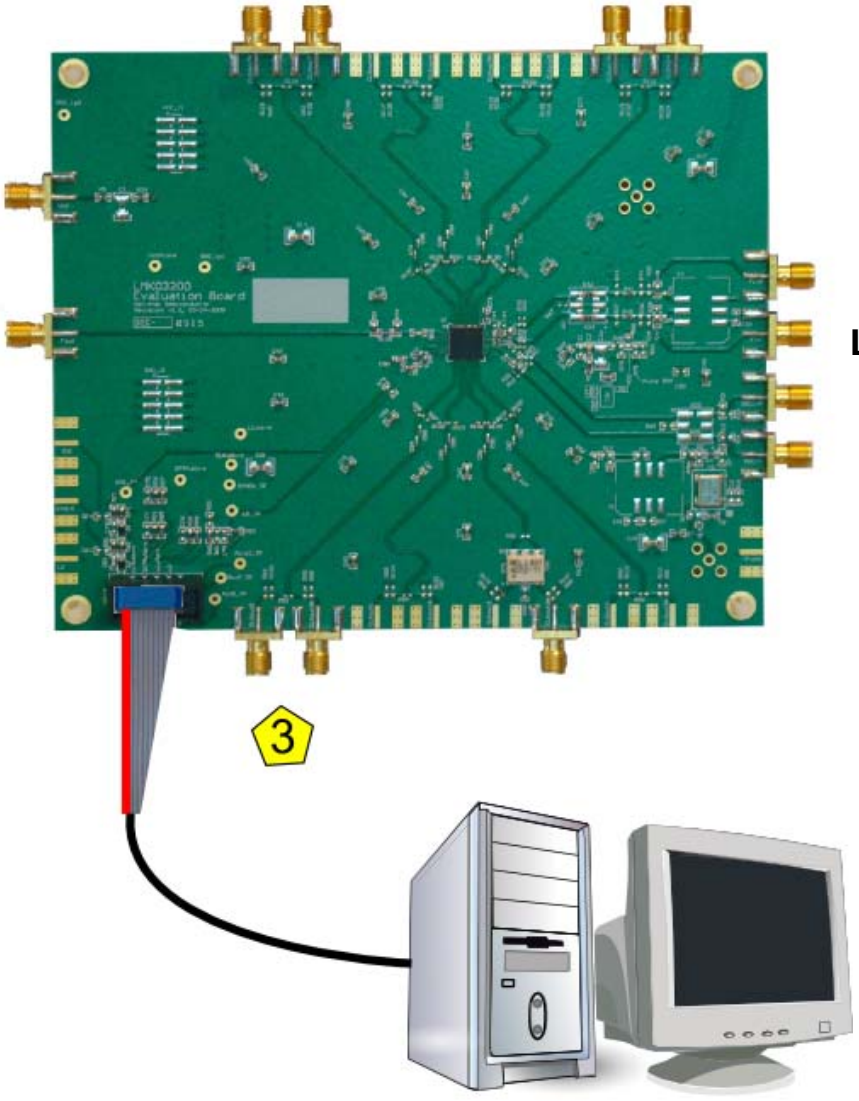


Figure 2 - Connecting communications to LPT port

Read first, Basic Operation (Continued)

4. Start CodeLoader 4.

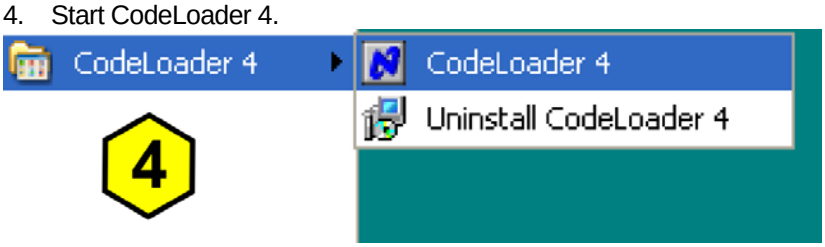


Figure 3 - Starting CodeLoader 4

5. Select the USB or LPT Communication Mode on the Port Setup tab as appropriate.

6. Select the default mode by clicking "Mode" → "19.44 MHz OSCin (default)"

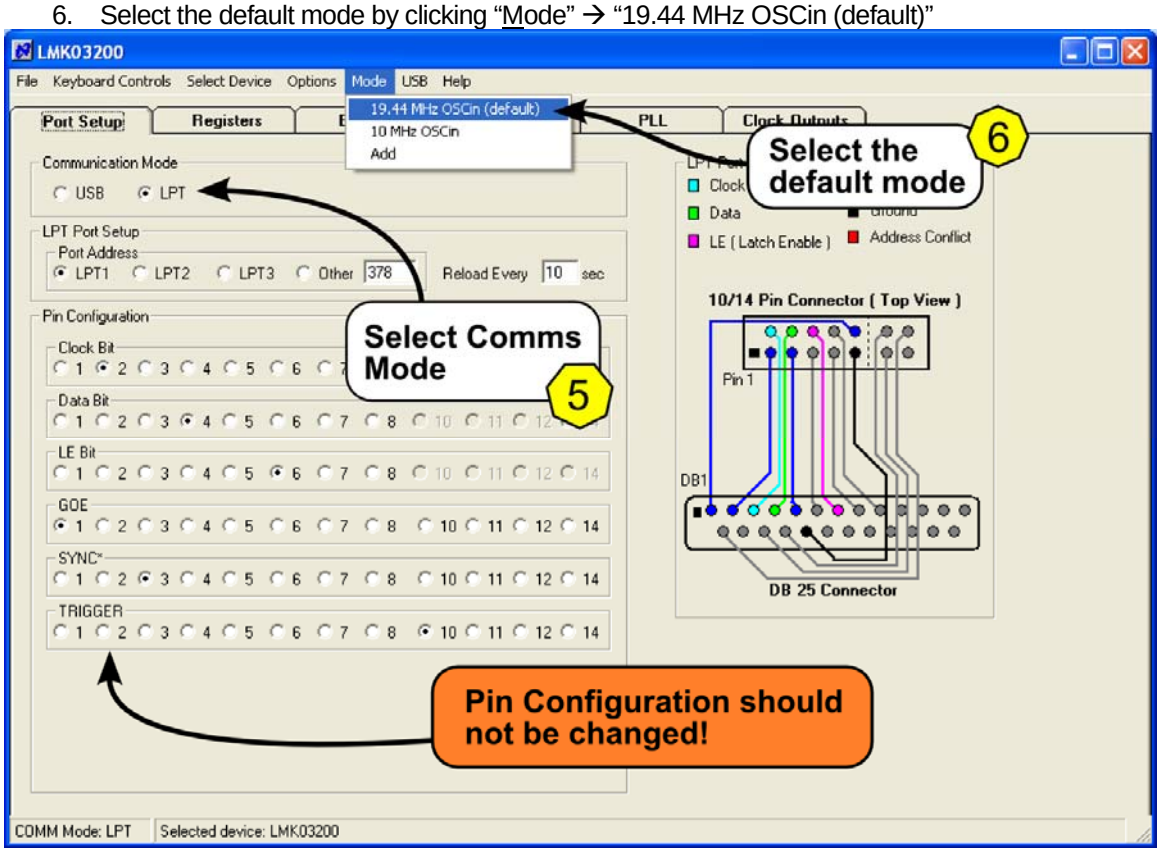


Figure 4 - Selecting default mode

Read first, Basic Operation (Continued)

7. **Enable output to be measured**, any of CLKout(0-7) or EN_Fout from either Clock Outputs or Bits/Pins tab.

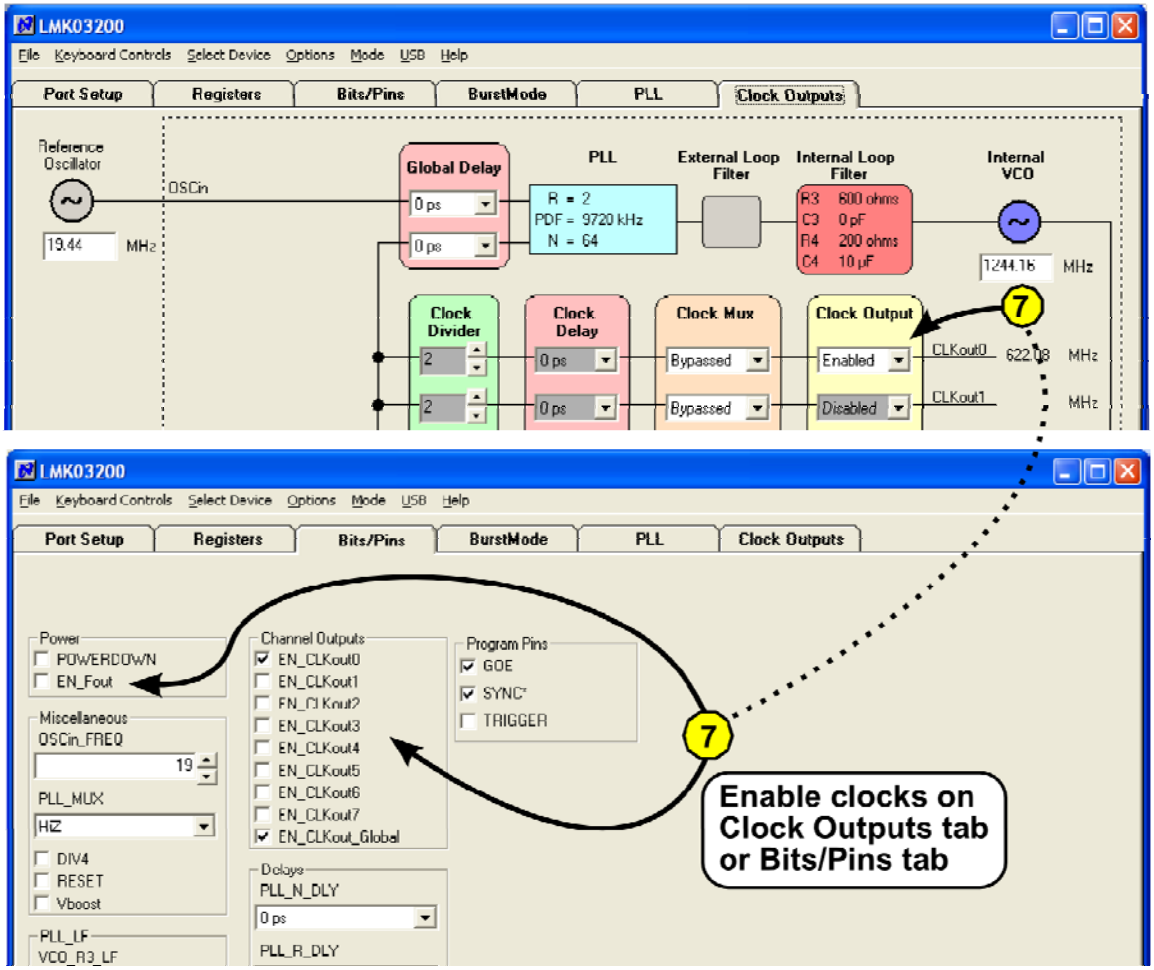


Figure 5 - Enabling outputs

8. **Program** the part by clicking "Keyboard Controls" → "Load Device" or by pressing **Ctrl+L**.

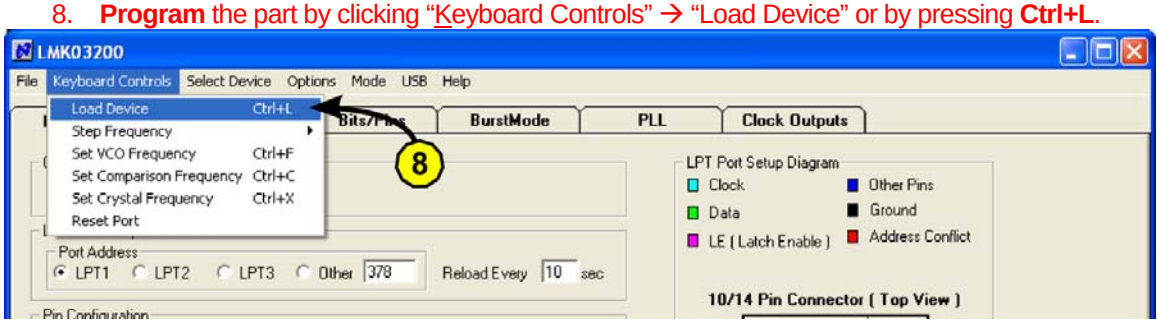


Figure 6 - Programming the device

9. Make measurements… After programming, the **uWire cable can be unplugged from the evaluation board to minimize noise and EMI.**

Engaging 0-Delay Mode

To engage 0-Delay mode a two step programming sequence is followed as described in the datasheet. Following this document's "Read first, Basic Operation" section effectively completes step 1 with the exception of setting 0-delay options in the Bits/Pins tab. When Ctrl-L is pressed all the registers listed on the registers tab from R0 (INIT), R0 to R9, R11, R13 to R15 are programmed. Then step 2 is performed and the outputs will be in 0-delay mode. The CodeLoader software simplifies step 2 by only requiring the user to check the 0_DELAY_MODE checkbox on the Bits/Pins tab as the software automatically reprograms PLL_N for the user. Clicking "Keyboard Controls" → "Load Device" is the same thing as pressing Ctrl-L.

The user must select a clock divide value which divides with no remainder into the PLL_N value of step 1 so that when 0_DELAY_MODE is enabled, the CLKout divider evenly divides into the PLL_N value. If this is not done, CodeLoader will program the PLL VCO to the closest frequency which may cause the device to loose lock. The two frequency loop equations which should result in the same VCO frequency are shown below:

OSCin Frequency / PLL_R * PLL_N = VCO Frequency
and
OSCin Frequency / PLL_R * PLL_N_New * CLKoutX_DIV = VCO Frequency

Step 1

To summarize step 1

- Load a default Mode
- On the PLL tab setup OSCin frequency, PLL R, PLL N, VCO output frequency, etc. as desired.
- On the Clock Outputs tab setup the clock outputs as desired.
    - The lowest frequency must be feed back to PLL N, so CLKout5 or CLKout6 must be programmed with the lowest frequency. If external feedback is used, the clock which generates the signal for external feedback must be programmed with the lowest frequency.
- On the Bits/Pins tab, set the 0-delay options as desired, this includes FB_MUX for selecting feedback channel, PLL_MUX to set digital lock detect, and DLD_MODE2 set for alternate digital lock detect mode. Ensure that 0_DELAY_MODE is unchecked. Ensure that OSCin_FREQ is set to the nearest MHz value of the OSCin frequency.

Press Ctrl-L (same as "Keyboard Controls" → "Load Device").

- Note, register words (like R0, R1, R15, etc.) are loaded to the device when changes are made to register bits (like PLL_N, CLKout3_EN, etc) assuming that the menu "Options" -> "AutoReload with Changes," is checked, which is its default setting. By pressing Ctrl-L manually, this ensures all registers are loaded and in the proper order.

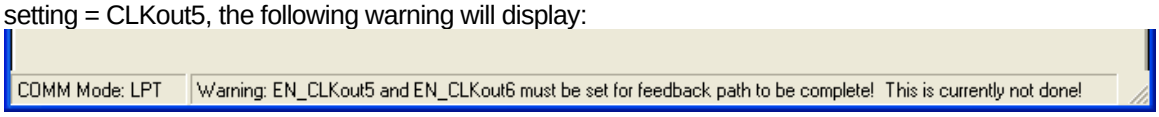
Step 2

Now that the part is operating on frequency, the second step enables the 0-delay mode.

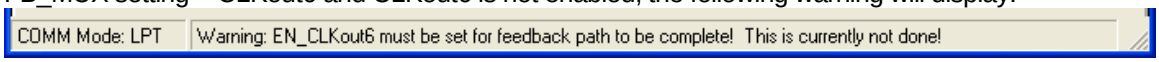
- Check 0_DELAY_MODE on Bits/Pins tab

When 0_DELAY_MODE is checked, the software will attempt to automatically re-program PLL_N with the appropriate value so that lock is achieved given the selected CLKout divide. The software will also attempt to warn the user of any errors. For example:

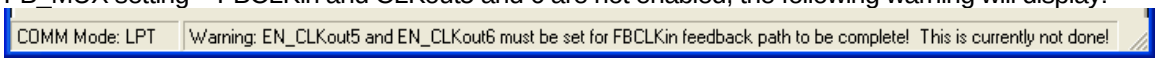
If 0_DELAY_MODE is enabled but the appropriate clock outputs are not enabled given FB_MUX setting = CLKout5, the following warning will display:



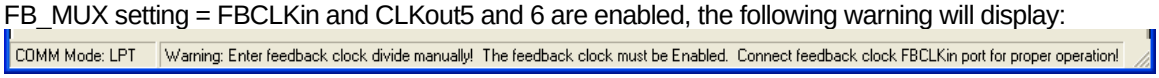
FB_MUX setting = CLKout6 and CLKout6 is not enabled, the following warning will display:



FB_MUX setting = FBCLKin and CLKout5 and 6 are not enabled, the following warning will display:



FB_MUX setting = FBCLKin and CLKout5 and 6 are enabled, the following warning will display:



Since it is possible that external divides could be encountered when using the device with external feedback via FBCLKin the actual CLKoutX_DIV * External Divide value must be entered into the manual divide entry box as shown in Figure 7.

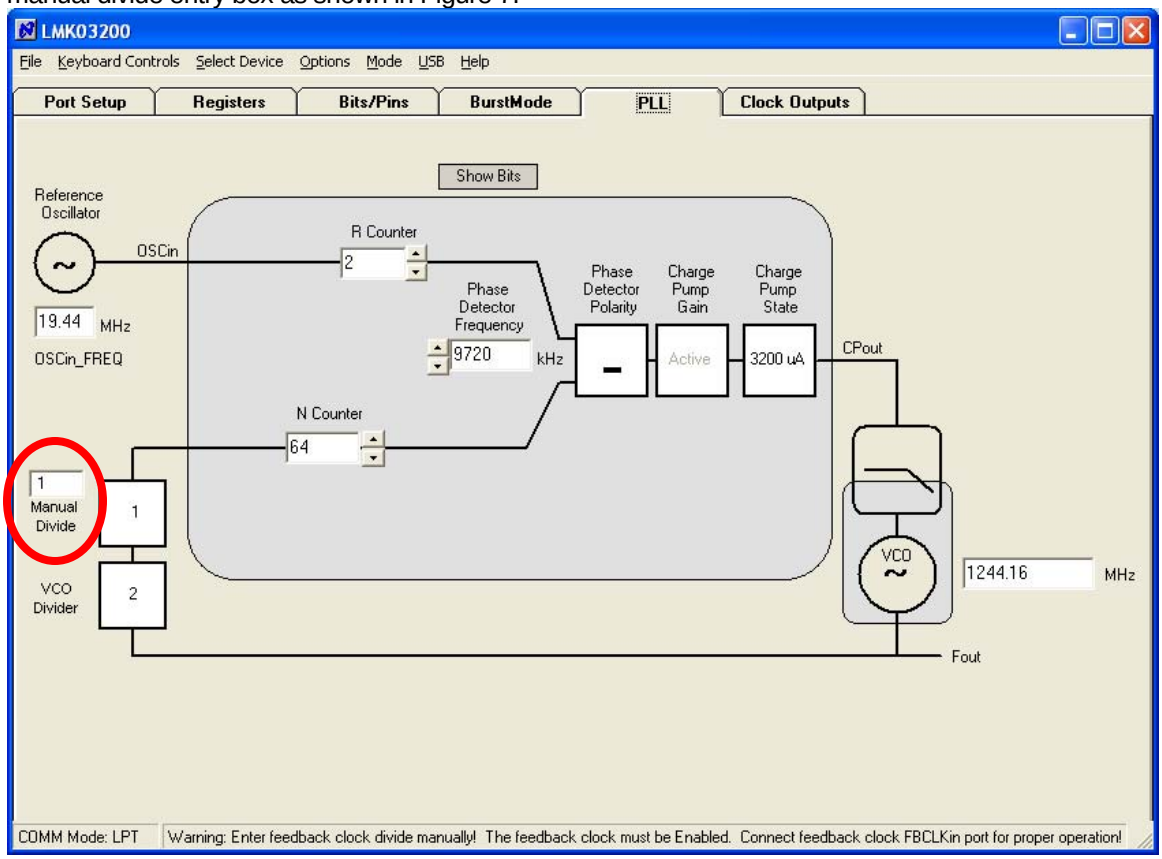


Figure 7 – Manual divide input is shown (circled in red) when CLKout5 & CLKout6 are enabled and FB_MUX = FBCLKin.

Note that pressing Ctrl-L (same as Keyboard Controls → Load Device) when 0_DELAY_MODE is activated will prevent R0 (INIT) from being programmed.

Board Information

OSCin

By default the board is configured to use the on-board crystal oscillator. It is also possible to use the board with a single ended or differential reference source at the OSCin port. Below are several possible configurations for driving OSCin.

OSCin using on board crystal oscillator [default]	
0 ohm	R4, R12, R14 [power to crystal oscillator], R15
39 ohm	R3 [can also be 0 ohm – depends on oscillator output power, 39 ohms to be a voltage divider]
51 ohm	R22
0.1 uF	C6, C10 (C9 is a 0.1 uF 0402 cap which may be moved to C10)
Open	C9 R6, R7, R8, R10, R11, R16, R19, R20, R21, R23, R25, R64

Differential OSCin setup	
0 ohm	R15, R16, R20, R25
100 ohm	R19
0.1 uF	C6, C9 (C10 is a 0.1 uF 0402 cap which may be moved to C9)
Open	C10 R10, R11, R12, R21, R22, R23 R14 [remove power from crystal oscillator for noise reasons]

Single ended OSCin setup	
0 ohm	R15, R16
51 ohm	R22
0.1 uF	C6, C10 (C9 is a 0.1 uF 0402 cap which may be moved to C10)
Open	C9 R10, R12, R19 R14 [remove power from crystal oscillator for noise reasons]

Fout

Fout allows direct access to the internal VCO before the clock distribution section. The EN_Fout bit must be selected to enable Fout. A 3 dB pad is placed on R49, R51, and R139.

Loop Filter

R69 and R72 form a “resistor switch” which allows either one of two different loop filters to be selected. The second loop filter on the bottom of the board is unpopulated by factory.

Loop Filter	**Resistor Switch**	**Loop Filter Components**	**Default Loop Bandwidth**
Loop Filter #1 [default]	R69 Shorted	C1, C2, C2p, R2	57.7 kHz
Loop Filter #2	R72 Shorted	C1_AUX, C2_AUX, C2p_AUX, R2_AUX	N/A

Features of the board

- Either one of two loop filters can be selected by shorting either R69 or R72. More info about the loop filter can be found in the General Description. The second loop filter on the bottom of the board is unpopulated for customer use.
- Test points for each of the uWire lines are scattered in the lower left corner of the board and include: GOE_TP, DATAuWire, CLKuWire, LEuWire, SYNC_TP, and LD_TP.

- **Ground** is located on the unstuffed 10 pin header on the left side of the board.
- **Ground** is located on the GND_tp2 in the upper left corner of the board and GND_tp1 located to the right of the Vcc SMA connector.
- **Ground** is located on the bottom side of the board on each pad of the unstuffed 10 pin header GND_J2.

- **Vcc** is located on the unstuffed 10 pin header on the upper left side of the board.
- **Vcc** is located on VccPlane test point located to the right of the Vcc SMA.
- **Vcc** is located on the bottom side of the board on each pad of the unstuffed 10 pin header VCC_J2

Other Important Notes

- When changing the OSCin frequency, the OSCin frequency register needs to match.
- Toggle the SYNC* pin to synchronize the clock outputs when in divided mode. If the SYNC* pin is low, divided outputs will not oscillate but the bypassed outputs will continue to oscillate.
- For both loop filters, a helper silkscreen is offset from the loop filters to help identify the components according to National Semiconductor's traditional reference designators associated with loop filters.
- The silk screen Fin/Fin* designates the FBCLKin/FBCLKin* port.

Recommended Equipment

Power Supply
The Power Supply should be a low noise power supply.

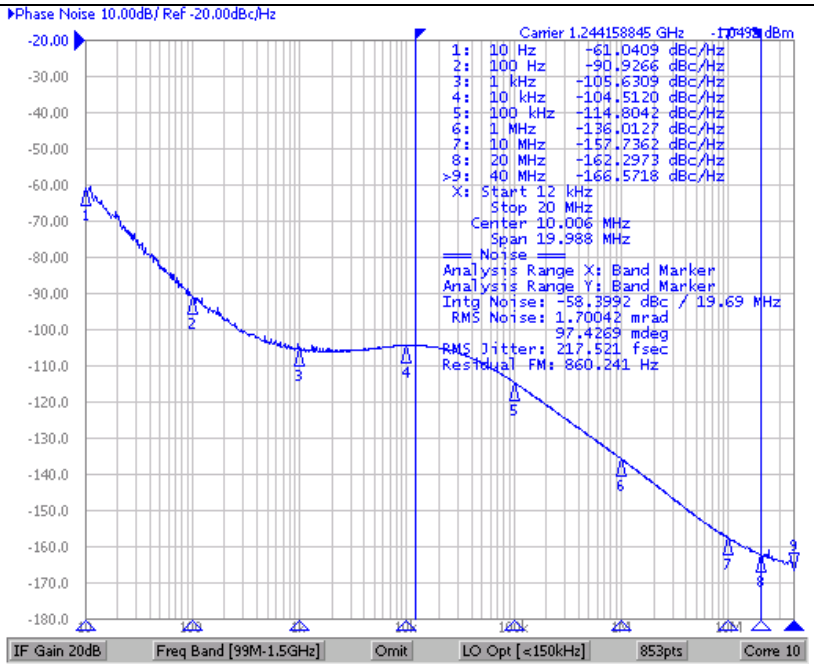
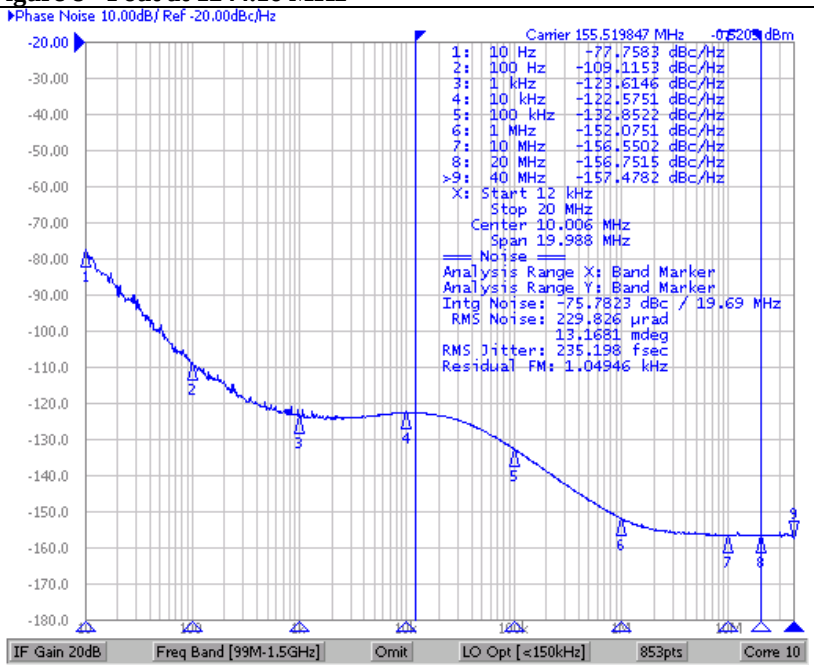
Phase Noise / Spectrum Analyzer
For measuring phase noise an Agilent E5052A is recommended. An Agilent E4445A PSA Spectrum Analyzer with the Phase Noise option is also usable although the architecture of the E5052A is superior for phase noise measurements. At frequencies less than 100 MHz the local oscillator noise of the PSA is too high and measurements will be of the local oscillator, not the device under test.

Oscilloscope
For measuring delay an Agilent Infiniium DSO81204A was used.

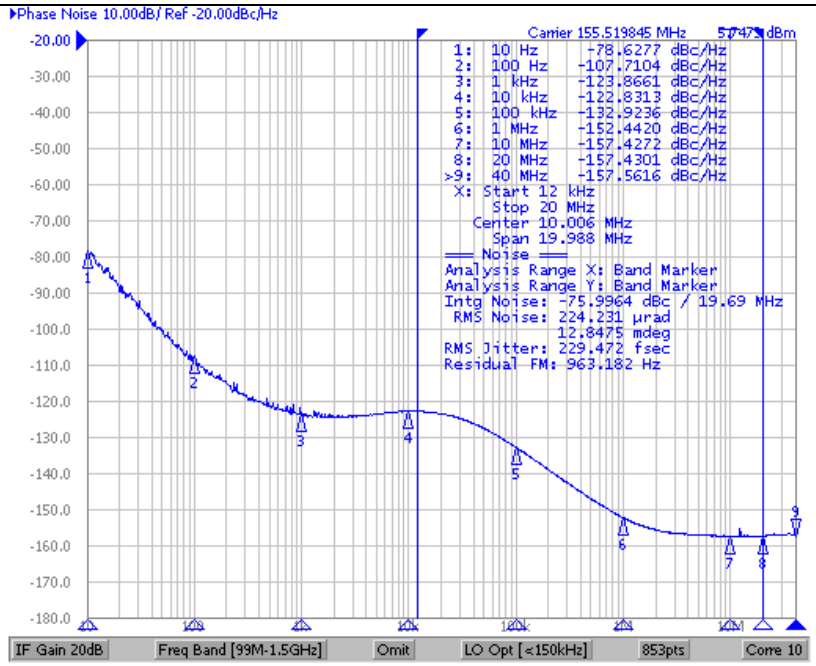
Reference Oscillator
The on board crystal oscillator will provide a low noise reference signal to the device at offsets greater than 1 kHz.

Note: The default loop filter has a loop bandwidth of ~60 kHz. Inside the loop bandwidth of a PLL the noise is greatly affected by any noise on the reference oscillator (OSCin). Therefore any noise on the oscillator less than 60 kHz will be passed through and seen on the outputs. For this reason the main output of a Signal Generator is not recommended for driving OSCin in this setup.

Phase Noise

Output Frequency = 1244.16 MHz Internal VCO, Fout output	 **Figure 8 - Fout at 1244.16 MHz**	Reference source is on board 19.44 MHz crystal Below ~1 kHz phase noise is dominated by the crystal 10 Hz – 20 MHz integrated RMS jitter = 439 fs 100 Hz – 20 MHz integrated RMS jitter = 248 fs 12 kHz – 20 MHz integrated RMS jitter = 218 fs
LVDS output CLKout2 VCO Frequency = 1244.16 MHz, VCO_DIV=2, CLKout2_div=4 LVDS output (155.52 MHz)	 **Figure 9 – LVDS output CLKout2 at 155.52 MHz**	Output is measured with a Minicircuits ADT2-1T balun. Reference source is on board 19.44 MHz crystal Below ~1 kHz phase noise is dominated by the crystal 10 Hz – 20 MHz integrated RMS jitter = 451 fs 100 Hz – 20 MHz integrated RMS jitter = 263 fs 12 kHz – 20 MHz integrated RMS jitter = 235 fs (shown)

LVPECL output CLKout4
VCO Frequency = 1244.16 MHz, VCO_DIV=2, CLKout4_div=4
LVPECL output (155.52 MHz)



Output is measured with a Minicircuits ADT2-1T balun.
Reference source is on board 19.44 MHz crystal

Below ~1 kHz phase noise is dominated by the crystal
10 Hz – 20 MHz integrated RMS jitter = 448 fs
100 Hz – 20 MHz integrated RMS jitter = 257 fs
12 kHz – 20 MHz integrated RMS jitter = 229 fs (shown)

Figure 10 – LVPECL output CLKout4 at 155.52 MHz

Reference Oscillator Phase Noise note:
The performance of the on-board crystal can be affected by noise from the power supply. Noise from the power supply can cause the phase noise of the C3391-19.440 crystal to increase between 10 Hz to 1 kHz.

Delays

These delay measurements illustrate how skew errors due to different length traces may be tuned out.
The delay may be adjusted in steps of ~150 ps.

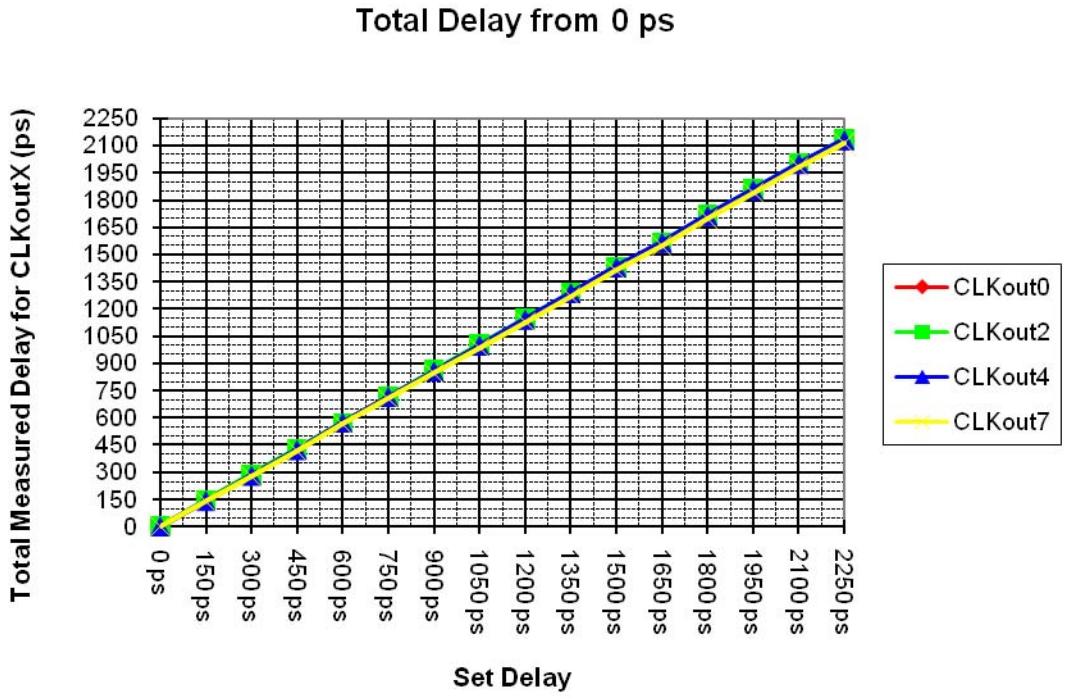


Figure 11 – Delays

Figure 11 shows as delay is added, total delay increases linearly.

Note: a small delay is incurred by placing the device into the various delay and divide modes from the bypass mode. This delay is not shown here.

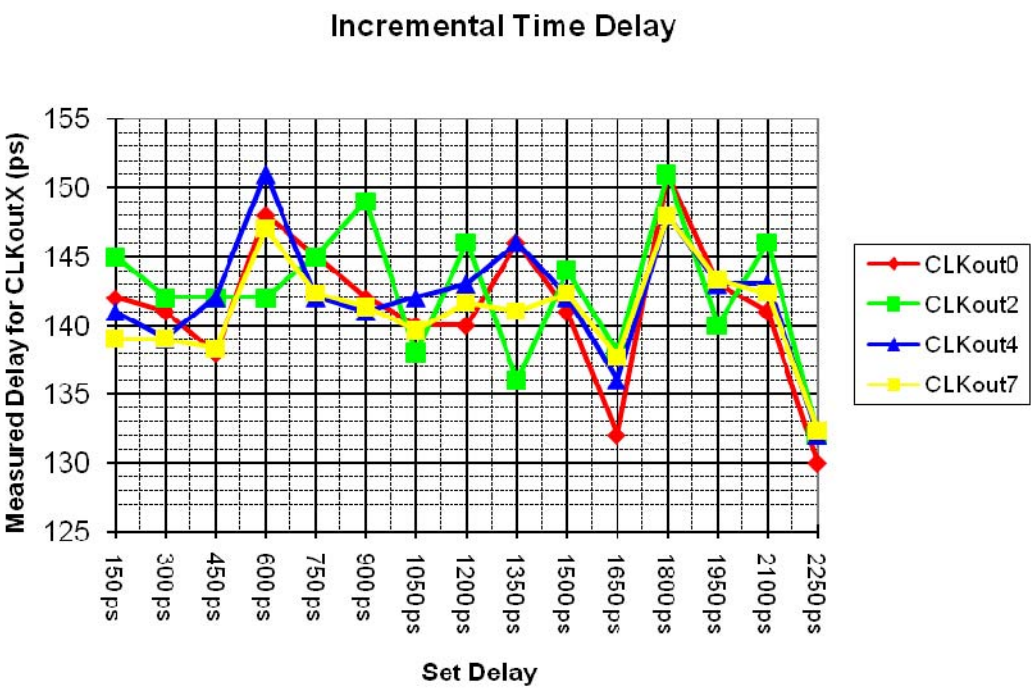


Figure 12 – Delays

Figure 12 shows that the step to step delay is not exactly 150 ps.

Note: a small delay is incurred by placing the device into the various delay and divide modes from the bypass mode. This delay is not shown here.

CodeLoader Settings

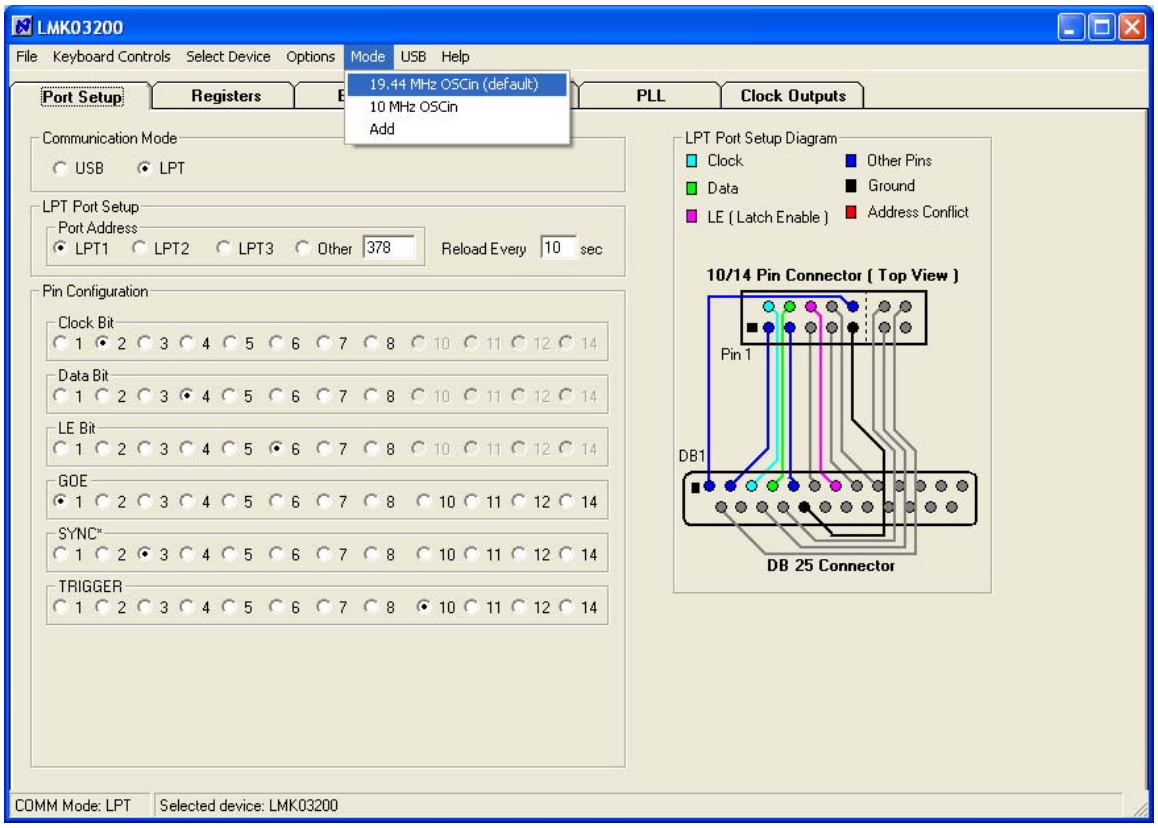


Figure 13 - Port Setup Tab & Selecting a Default Mode

The Port Setup tab tells CodeLoader what signals are assigned to which pins. If these settings are incorrect, the part will not program.

Part setup can be restored to the default state by clicking Mode → "19.44 MHz OSCin (default)." The default reference oscillator used for these instructions is 19.44 MHz and the restored mode expects a 19.44 MHz OSCin signal. **For the loaded mode to take effect the device must be loaded by pressing Ctrl+L.**

The Bits/Pins tab shows some of the internal registers which are not accessible from any of the other visual tabs like “PLL” and “Clock Outputs.” *Right click on any of the bits for description.*

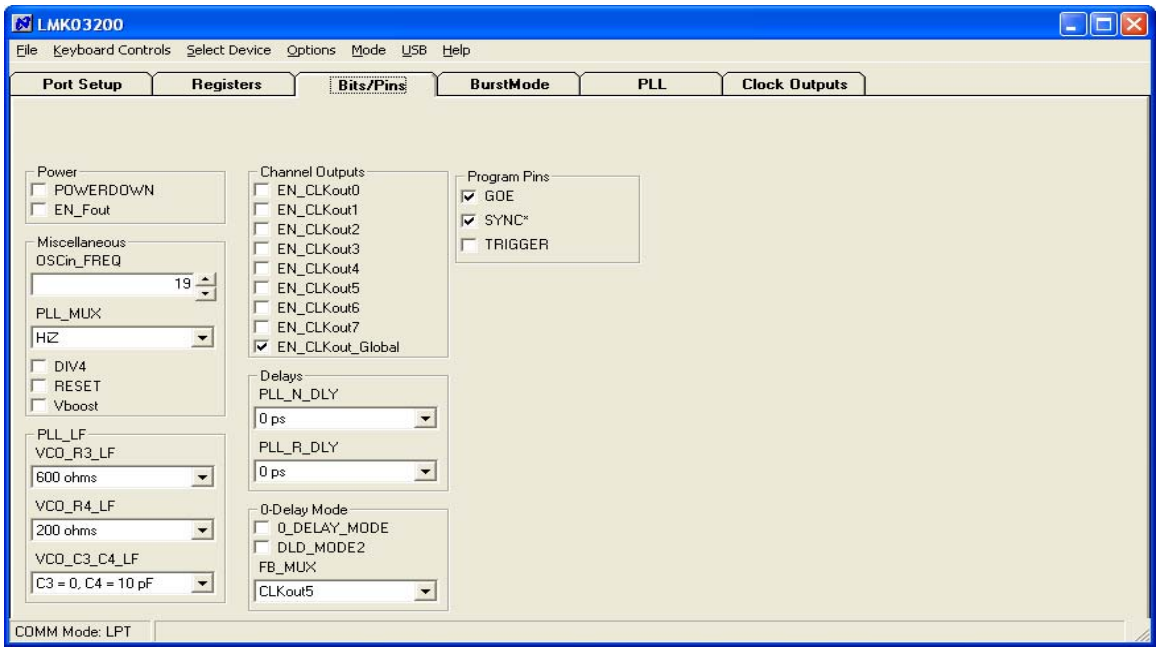


Figure 14 - Bits & Pins tab

Program Bits	
POWERDOWN	Powers the part down.
EN_Fout	Turns on the Fout pin for measuring the internal VCO.
OSCin_FREQ	Must be set to the OSCin frequency in MHz.
PLL_MUX	Programmable to many different values to support Lock Detect or aid troubleshooting.
DIV4	Shall be checked for OSCin frequencies greater than 20 MHz.
RESET	The registers can be defaulted by checking and unchecking RESET. Software bits will not reflect this.
Vboost	Increases Output Power on Clock Outputs
VCO_R3_LF VCO_R4_LF VCO_C3_C4_LF	Internal loop filter values, also accessible from Clock Outputs tab.
EN_CLKout0..7	Enable CLKout bits from CLKout0 to CLKout7. Also accessible from Clock Outputs tab.
PLL_N_DLY PLL_R_DLY	Delays for PLL N and PLL R. Also on Clock Outputs Tab
0_DELAY_MODE	Used to enable 0-Delay Mode, in the CodeLoader software, this will also cause PLL_N to be reprogrammed.
DLD_MODE2	Select alternate Digital Calibration Routine Complete mode in place of Digital Lock Detect mode. To use select Digital Lock Detect on PLL_MUX.
FB_MUX	Feedback from which clock output.
EN_CLKout_Global	Enable all clock outs. If unselected then the EN_CLKouts are overridden and the outputs are all disabled.

Program Pins	
GOE	Set Global Output Enable to high or low logic level.
SYNC*	Set SYNC* pin to high or low logic level.
TRIGGER	Set auxiliary trigger pin to high or low logic level.

The Registers tab shows the raw bits which will be programmed when device is loaded by clicking Keyboard Controls → Load Device or Ctrl+L.

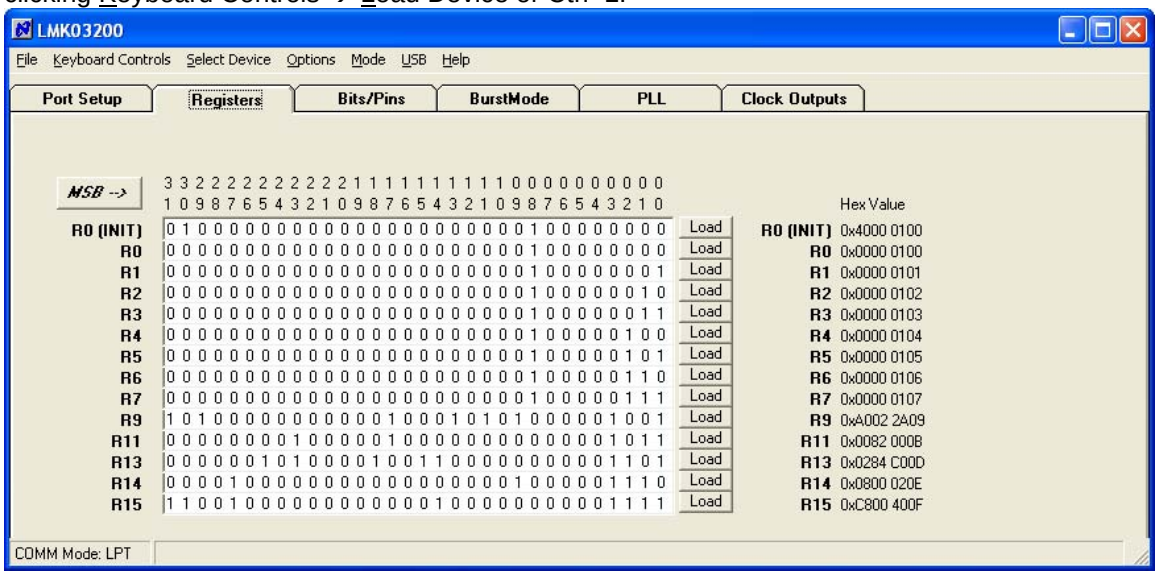


Figure 15 - Registers tab

The Clock Outputs tab allows the user to visualize the clock distribution portions of the device. From this tab the device's dividers, delays, clock output muxes, and output drivers can be programmed along with internal loop filter values. The PLL block shows the R and N divider values however to change these values either click on the PLL tab or the blue PLL box to access the PLL tab to make changes to the PLL.

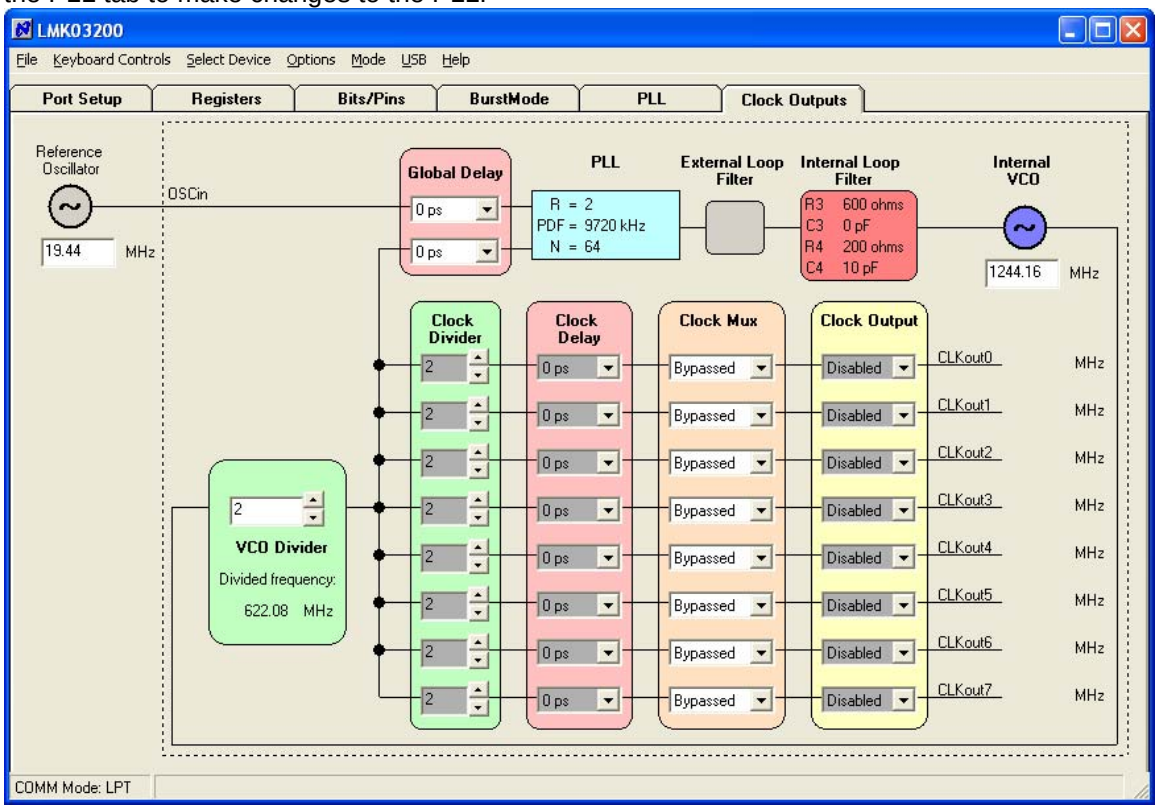


Figure 16 - Clock Outputs tab

The PLL tab shows a conventional PLL diagram along with the VCO Divider. It is important to realize that the **total effective N value is PLL N Counter * VCO Divider**. This means that the "channel spacing" is the Phase Detector Frequency * VCO Divider. Depending on the situation, this may require the R Counter multiplied up by the value of the VCO Divider to achieve desired VCO output frequencies. **When 0-delay mode is active, the total effective N value is PLL N Counter * Clock Output Divider * VCO Divider**.

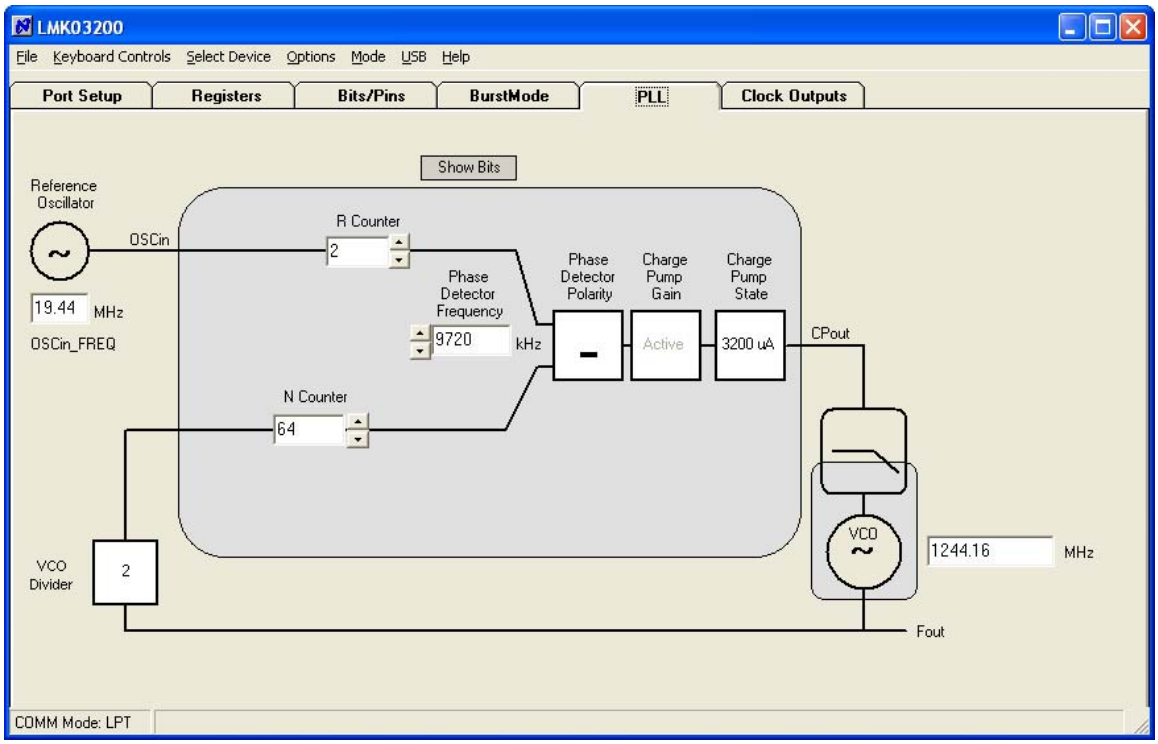


Figure 17 - PLL tab

Example: If the desired VCO output frequency was 1244.16 MHz, R would need to be increased to 2 before 1253.88 MHz could be programmed because the VCO Divider of 2 would only allow programming of 1244.16, 1263.6, 1283.04, etc. with a 9.72 MHz phase detector frequency. This is because changing the N counter from 64 to 65 changes to total N by two, 128 to 130!

When in 0-Delay Mode, then selected channel divider is added to the divide on the feedback path after VCO Divider. Refer to Figure 7 to see this illustrated.

Appendix A: Impact of Reference on Phase Noise

Inside the loop bandwidth of a PLL the phase noise is set by the quality of the reference oscillator used. For this reason it is important to select a reference oscillator suitable for the application. Power supply noise can also impact the phase noise performance of the oscillator.

Test Setup

Using the same loop filter as described in the General Description and by driving the OSCin frequency with very low jitter 100 MHz Wenzel Crystal (501-04517D) and setting R = 10 to achieve a phase detector frequency of 10 MHz. A low integrated RMS jitter of 235 fs is measured vs. the 439 ps measured in the Phase Noise section with 19.44 MHz crystal in the bandwidth of 10 Hz to 20 MHz.

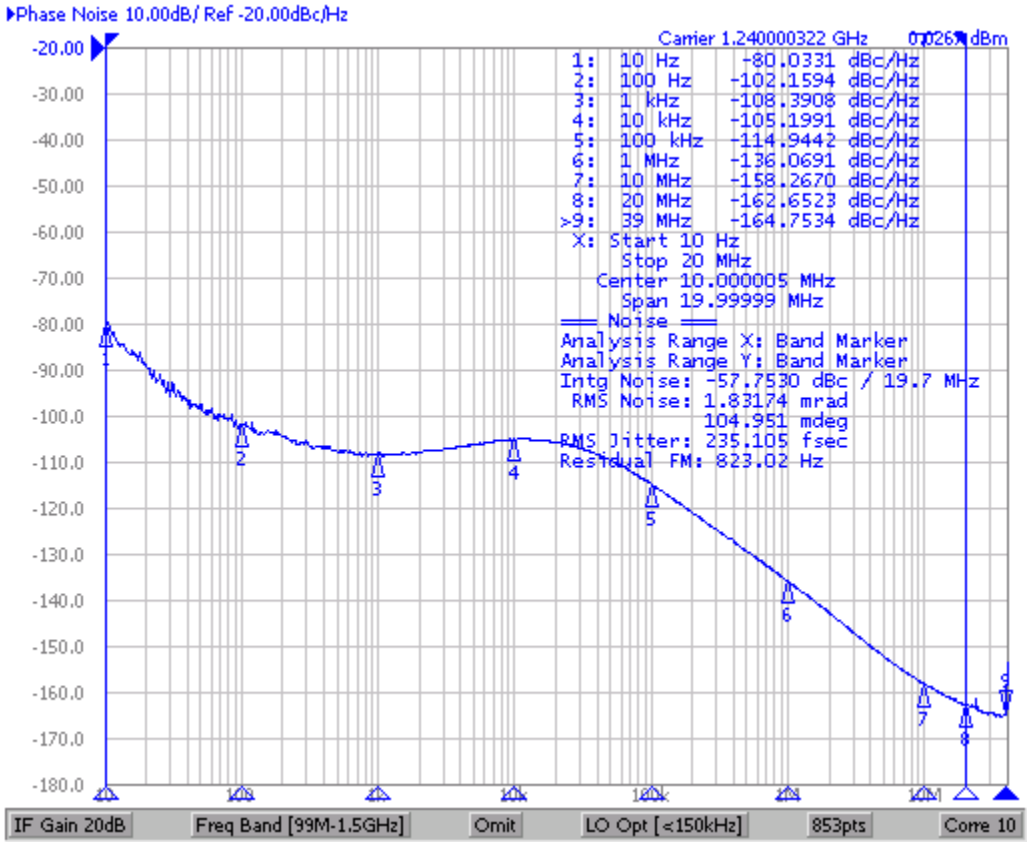


Figure 18 - Phase Noise with Clean Reference

10 Hz – 20 MHz integrated RMS jitter = 235 fs (shown)

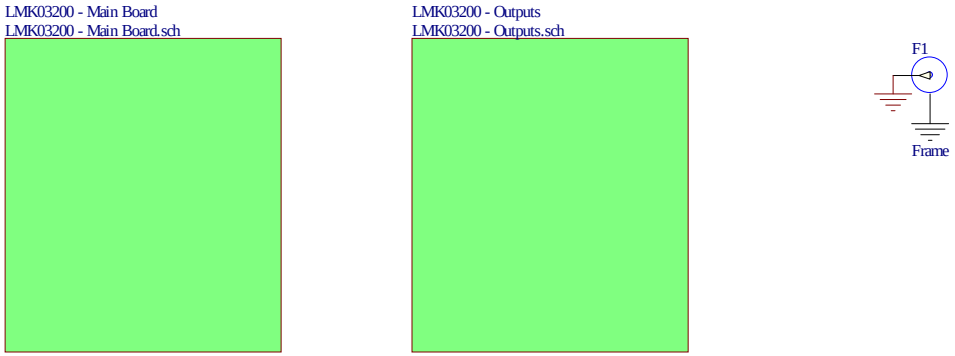
100 Hz – 20 MHz integrated RMS jitter = 232 fs

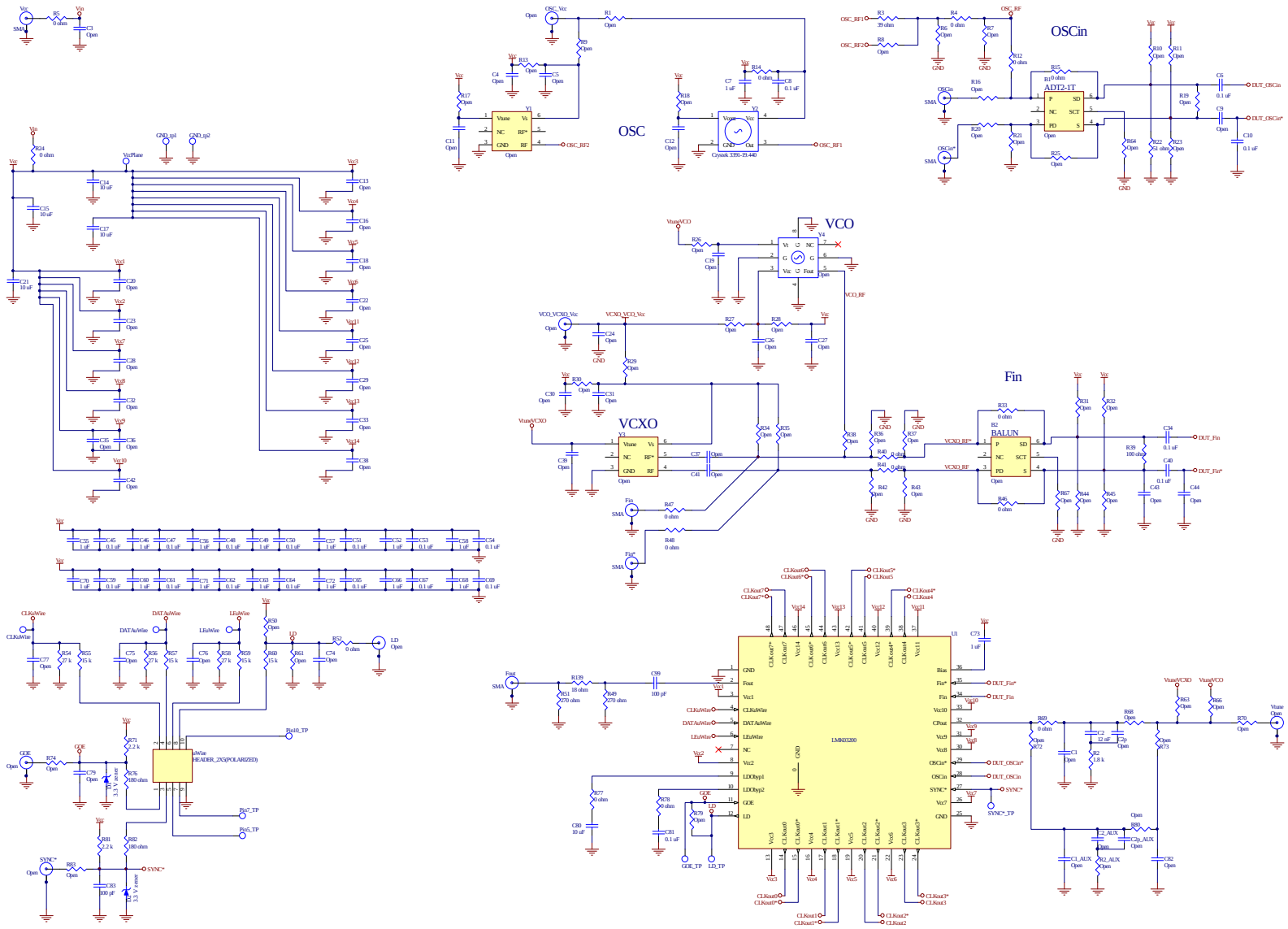
12 kHz – 20 MHz integrated RMS jitter = 210 fs

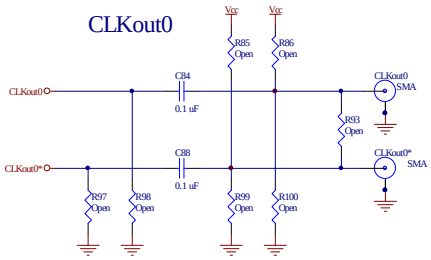
Conclusion

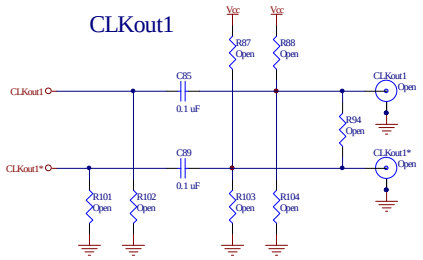
This diagram illustrates how the phase noise inside the loop bandwidth is set by the quality of the reference oscillator used. Phase noise outside the loop bandwidth is set by the VCO noise level.

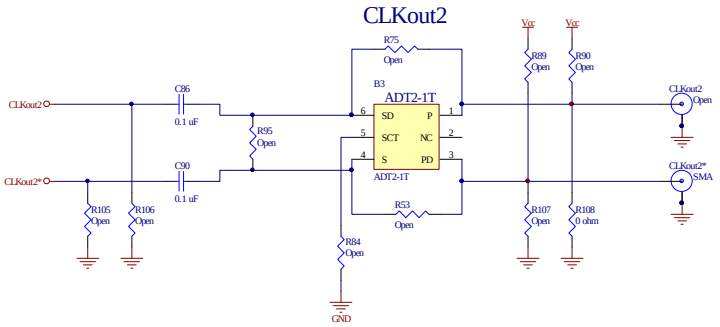
Appendix B: Schematics

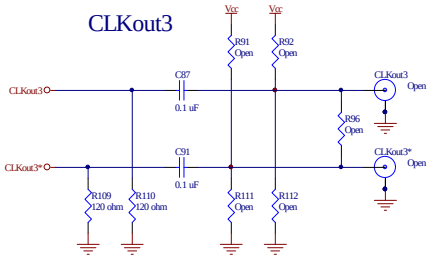


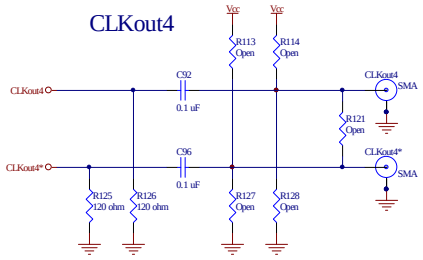

OSC
OSCin
VCO
VCXO
Fin
ADT2-1T
BALUN
LMK03200
HEADER_2X5(POLARIZED)

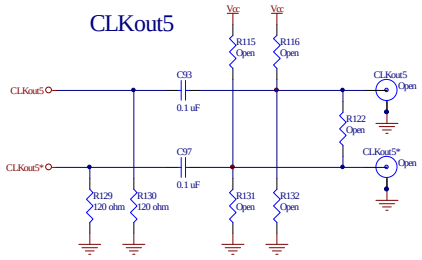

CLKout0
Vcc
Vcc
R85 Open
R86 Open
CLKout0
SMA
C84
0.1 uF
CLKout0
R93 Open
C88
0.1 uF
CLKout0*
SMA
CLKout0*
R97 Open
R98 Open
R99 Open
R100 Open

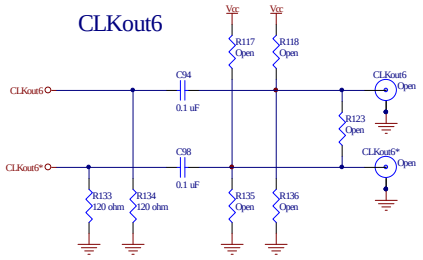

CLKout1
Vcc
Vcc
R87 Open
R88 Open
CLKout1
Open
C85
0.1 uF
CLKout1
R94 Open
C89
0.1 uF
CLKout1*
Open
CLKout1*
R101 Open
R102 Open
R103 Open
R104 Open

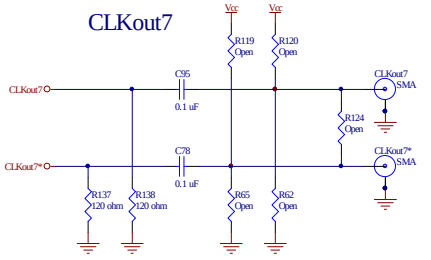

CLKout2
R75
Open
Vcc
Vcc
R89 Open
R90 Open
B3
ADT2-1T
SD
SCT
S
P
NC
PD
ADT2-1T
CLKout2
Open
C86
0.1 uF
CLKout2
R95 Open
C90
0.1 uF
CLKout2*
SMA
CLKout2*
R53
Open
R105 Open
R106 Open
R84 Open
R107 Open
R108 0 ohm
GND


CLKout3
Vcc
Vcc
R91 Open
R92 Open
CLKout3
Open
C87
0.1 uF
CLKout3
R96 Open
C91
0.1 uF
CLKout3*
Open
CLKout3*
R109 120 ohm
R110 120 ohm
R111 Open
R112 Open


CLKout4
Vcc
Vcc
R113 Open
R114 Open
CLKout4
SMA
C92
0.1 uF
CLKout4
R121 Open
C96
0.1 uF
CLKout4*
SMA
CLKout4*
R125 120 ohm
R126 120 ohm
R127 Open
R128 Open


CLKout5
Vcc
Vcc
R115 Open
R116 Open
CLKout5
Open
C93
0.1 uF
CLKout5
R122 Open
C97
0.1 uF
CLKout5*
Open
CLKout5*
R129 120 ohm
R130 120 ohm
R131 Open
R132 Open


CLKout6
Vcc
Vcc
R117 Open
R118 Open
CLKout6
Open
C94
0.1 uF
CLKout6
R123 Open
C98
0.1 uF
CLKout6*
Open
CLKout6*
R133 120 ohm
R134 120 ohm
R135 Open
R136 Open


CLKout7
Vcc
Vcc
R119 Open
R120 Open
CLKout7
SMA
C95
0.1 uF
CLKout7
R124 Open
C78
0.1 uF
CLKout7*
SMA
CLKout7*
R137 120 ohm
R138 120 ohm
R65 Open
R62 Open

Appendix C: Bill of Materials

Part	Manufacturer	Part Number	Qnt	Identifier
Capacitors				
100 pF	Kemet	C0603C101J5GAC	2	C83, C99
12 nF	Kemet	C0603C123K1RACTU	1	C2
0.1 uF	Kemet	C0402C104J4RAC	20	C6, C10, C34, C40, C78, C84, C85, C86, C87, C88, C89, C90, C91, C92, C93, C94, C95, C96, C97, C98
0.1 uF	Kemet	C0603C104J3RAC	16	C8, C45, C47, C48, C50, C51, C53, C54, C59, C61, C62, C64, C65, C67, C69, C81
1 uF	Kemet	C0603C105K8VAC	16	C7, C46, C49, C52, C55, C56, C57, C58, C60, C63, C66, C68, C70, C71, C72, C73
10 uF	Kemet	C0805C106K9PAC	4	C14, C15, C17, C21
10 uF	Kemet	C0805C106K9PAC	1	C80
Resistors				
0 ohm	Vishay/Dale	CRCW06030000Z0EA	10	R4, R5, R12, R14, R24, R47, R48, R52, R69, R78
0 ohm	Vishay/Dale	CRCW08050000Z0EA	3	R15, R33, R46
0 ohm	Vishay/Dale	CRCW06030000Z0EA	4	R40, R41, R77, R108
18 ohm	Vishay/Dale	CRCW060318R0JNEA	1	R139
39 ohm	Vishay/Dale	CRCW060339R0JNEA	1	R3
51 ohm	Vishay/Dale	CRCW040251R0FKED	1	R22
100 ohm	Vishay/Dale	CRCW0603100RJNEA	1	R39
120 ohm	Vishay/Dale	CRCW0402120RJNED	10	R109, R110, R125, R126, R129, R130, R133, R134, R137, R138
180 ohm	Vishay/Dale	CRCW0603180RJNEA	2	R76, R82
270 ohm	Vishay/Dale	CRCW0603270RJNEA	2	R49, R51
1.8 k	Vishay/Dale	CRCW06031K80JNEA	1	R2
2.2 k	Vishay/Dale	CRCW06032K20JNEA	2	R71, R81
15 k	Vishay/Dale	CRCW060315K0JNEA	4	R55, R57, R59, R60
27 k	Vishay/Dale	CRCW060327K0JNEA	3	R54, R56, R58

Other				
3.3 V zener	Comchip	CZRU52C3V3	2	D1, D2
ADT2-1T	Minicircuits	ADT2-1T	1	B3
Frame	Printed Circuits Corp	PCB_LMK0200x, 8-22-2007	1	F1
HEADER_2X5(POLARIZED)	FCI Electronics	52601-S10-8	1	uWire
LMK03200	National Semiconductor	LMK03200	1	U1
Crystek 3391-19.440	Crystek	C3391-19.440	1	Y2
SMA	Johnson Components	142-0701-851	13	CLKout0, CLKout0*, CLKout2*, CLKout4, CLKout4*, CLKout7, CLKout7*, Fin, Fin*, Fout, OSCin, OSCin*, Vcc
0.375" Standoffs	SPC Technology	SPCS-6	4	Standoffs in the four corners (insert from bottom) -- (default)
Open				
Open	-	402.0	39	C9, C13, C16, C18, C20, C22, C23, C25, C28, C29, C32, C33, C36, C38, C42, C43, C44, R10, R11, R23, R31, R32, R44, R45, R67, R93, R94, R95, R96, R97, R98, R101, R102, R105, R106, R121, R122, R123, R124
Open	-	603.0	51	C1, C2_AUX, C4, C5, C11, C12, C19, C26, C27, C30, C31, C39, C74, C75, C76, C77, C79, C82, R1, R2_AUX, R6, R7, R8, R9, R13, R16, R17, R18, R19, R20, R21, R26, R27, R28, R29, R30, R38, R50, R61, R63, R64, R66, R68, R70, R72, R73, R74, R79, R80, R83, R84
Open	-	603.0	40	C35, C37, C41, R34, R35, R36, R37, R42, R43, R62, R65, R85, R86, R87, R88, R89, R90, R91, R92, R99, R100, R103, R104,

				R107, R111, R112, R113, R114, R115, R116, R117, R118, R119, R120, R127, R128, R131, R132, R135, R136
Open	-	805.0	2	C1_AUX, C24
Open	-	Open	3	C2p, C2p_AUX, C3
Open	-	805.0	3	R25, R53, R75
Open	-	Open	1	B1
Open	-	Open	1	B2
Open	-	Open	4	GND_J1, GND_J2, VCC_J1, VCC_J2
Open	-	Open	13	CLKout1, CLKout1*, CLKout2, CLKout3, CLKout3*, CLKout5, CLKout5*, CLKout6, CLKout6*, GOE, LD, SYNC*, Vtune
Open	-	Open	2	OSC_Vcc, VCO_VCXO_Vcc
Open	-	Open	1	Y4
Open	-	Open	2	Y1, Y3

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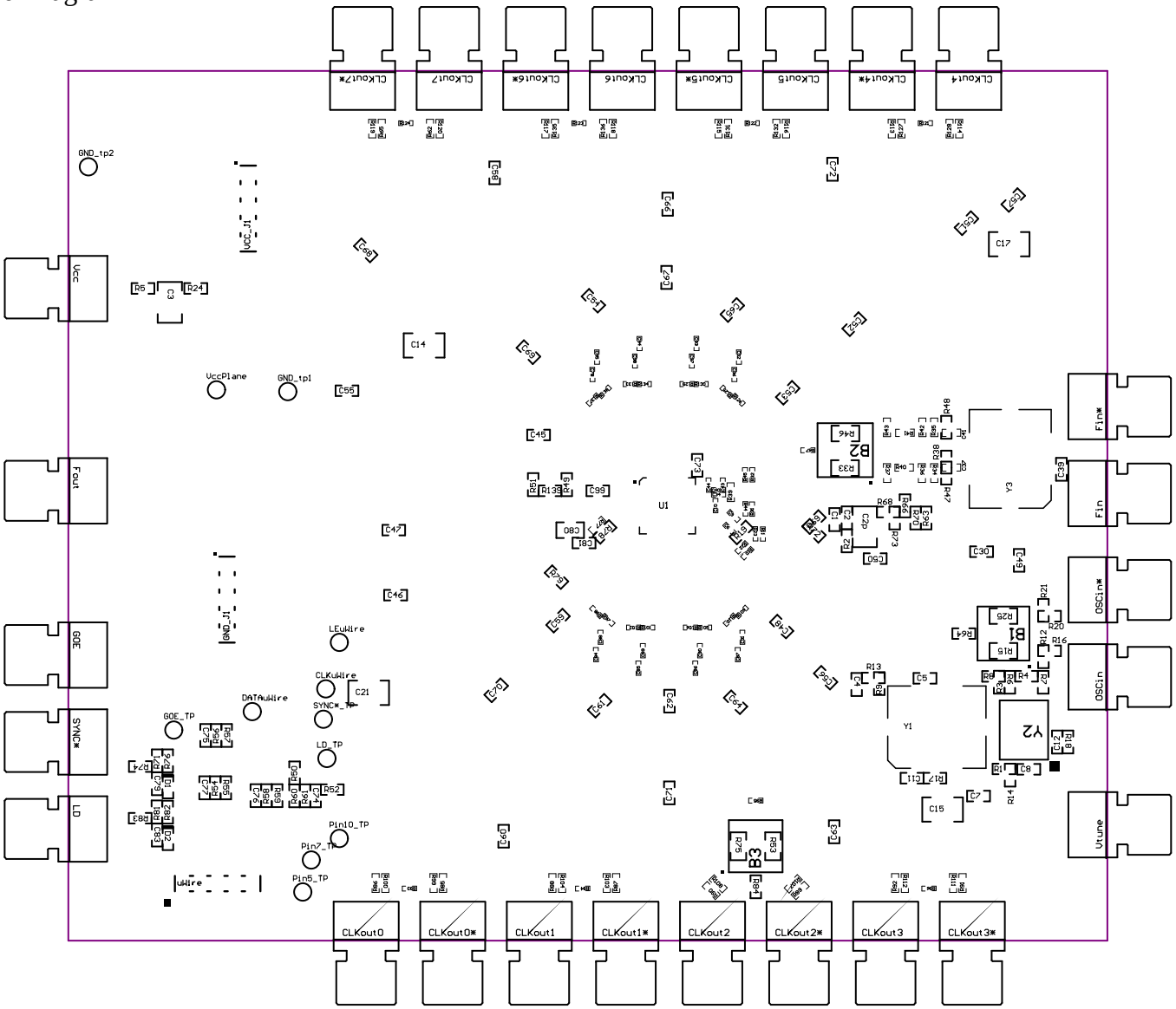
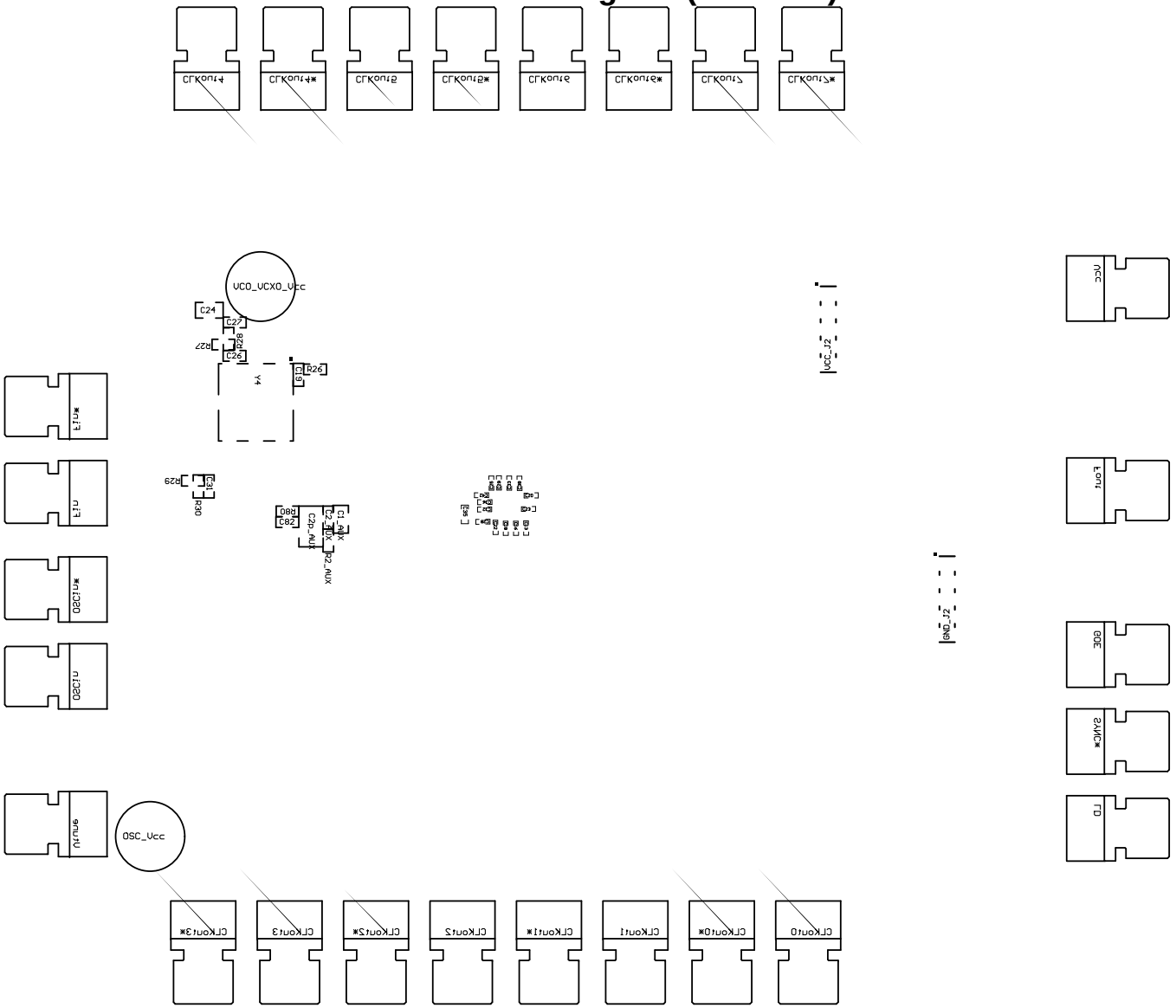
Appendix D: Build Diagram



Bottom Build Diagram (Mirrored)



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DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
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Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
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