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CAN Transceivers with Fast Loop Times for Highly Loaded Networks and Features For Functional Safety Networks

Check for Samples: SN65HVD255, SN65HVD256, SN65HVD257

FEATURES

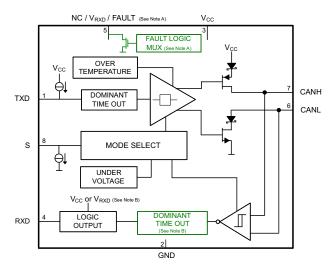
- Meets the Requirements of ISO11898-2
- 'Turbo CAN': Short Propagation Delay Times and Fast Loop Times; Higher Data Rates in Network; Enhances System Timing Margins
- I/O Voltage Range Supports 3.3V and 5V MCUs
- Ideal Passive Behavior When Unpowered
 - Bus Pins are High Impedance (no load to operating bus)
 - Logic Pins are High Impedance
 - Power Up/Down With Glitch Free Operation On Bus
- Protection Features:
 - ESD Protection of Bus Pins
 - HBM ESD Protection Exceeds ±12kV
 - Bus Fault Protection -27V to 40V
 - Undervoltage Protection on Supply Pins
 - Driver Dominant Time Out (TXD DTO)
 - SN65HVD257: Receiver Dominant Time Out (RXD DTO)
 - SN65HVD257: FAULT Output Pin
 - Thermal Shutdown Protection
- Characterized for -40°C to 125°C Operation

APPLICATIONS

- 1Mbps Operation in Highly Loaded CAN Networks Down to 10kbps Networks Using TXD DTO
- Industrial Automation, Control, Sensors and Drive Systems
- Building and Climate Control Automation
- Security Systems
- Telecom Base Station Status and Control
- SN65HVD257: Functional Safety With Redundant and Multi-topology CAN networks
- CAN Bus Standards Such as CANopen, DeviceNet, NMEA2000, ARNIC825, ISO11783, CAN Kingdom, CANaerospace

DESCRIPTION

This CAN transceiver meets the ISO1189-2 High Speed CAN (Controller Area Network) Physical Layer standard. It is designed for data rates in excess of 1 megabit per second (Mbps) in short networks, and enhanced timing margin and higher data rates in long and highly-loaded networks. The device provides many protection features to enhance device and CAN-network robustness. The SN65HVD257 adds additional features, allowing easy design of redundant and multi-topology networks with fault indication for higher levels of functional safety in the CAN system.



- A. Pin 5 function is device dependent; NC on SN65HVD255, V_{RXD} for RXD output level-shifting device on SN65HVD256, and FAULT Output on SN65HVD257
- B. RXD logic output is driven to 5V V_{CC} on 5V-only supply devices (SN65HVD255, SN65HVD257) and driven to V_{RXD} on output level-shifting device (SN65HVD256).
- C. RXD (Receiver) Dominant State Time Out is a device dependent option available only on SN65HVD257.

Figure 1. Functional Block Diagram



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

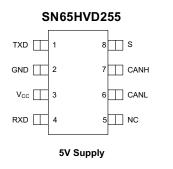
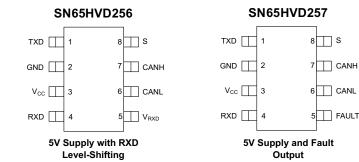


Figure 2. D PACKAGE (TOP VIEW)



DEVICE OPTIONS

PART NUMBER	I/O SUPPLY for RXD	TXD DTO	RXD DTO	FAULT Output	COMMENT	
SN65HVD255			No	'251 and '1050 functional upgrade with 'Turbo CAN' fast loop times and TXD DTO protection allowing data rates down to 10kbps		
SN65HVD256	Yes	Yes Yes No No No 1251 and '1050 functional upgrade with 'Turbo CAN' fa TXD DTO protection allowing data rates down to 10kt level shifting via RXD supply input.		'251 and '1050 functional upgrade with 'Turbo CAN' fast loop times and TXD DTO protection allowing data rates down to 10kbps. RXD output level shifting via RXD supply input.		
SN65HVD257	No	Yes	Yes	Yes	'251 and '1050 functional upgrade with 'Turbo CAN' fast loop times, TXD & RXD DTO protection allowing data rates down to 10kbps and fault output pin	

PIN FUNCTIONS

PIN		TYDE	DESCRIPTION		
NAME	NO.	ITPE	DESCRIPTION		
TXD	1	I	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)		
GND	2	GND	Bround connection		
V _{CC}	3	Supply	ansceiver 5V supply voltage		
RXD	4	0	CAN receive data output (LOW for dominant and HIGH for recessive bus states)		
NC	5	NC	SN65HVD255: No Connect		
V _{RXD}		Supply	N65HVD256: RXD output supply voltage		
FAULT		0	SN65HVD257: open drain FAULT output pin		
CANL	6	I/O	Low level CAN bus line		
CANH	7	I/O	High level CAN bus line		
S	8	I	Mode select: S (silent mode) select pin (active high)		

ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE ⁽²⁾	ORDERABLE PART NUMBER	TOP SIDE MARKING
–40°C to 125°C		SN65HVD255D and SN65HVD255DR	HVD255
	SOIC - D	SN65HVD256D and SN65HVD256DR	HVD256
40 0 10 120 0		SN65HVD257D and SN65HVD257DR (This device is in preview status)	HVD257

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



FUNCTIONAL DESCRIPTION

OPERATING MODES

The device has two main operating modes: normal mode and silent mode. Operating mode selection is made via the S input pin.

S Pin	S Pin MODE DRIVER		RECEIVER	RXD Pin			
LOW	Normal Mode	Enabled (ON)	Enabled (ON)	Mirrors Bus State ⁽¹⁾			
HIGH	Silent Mode	Disabled (OFF)	Enabled (ON)	Mirrors Bus State			

Table 1. Operating Modes

(1) Mirrors bus state: low if CAN bus is dominant, high if CAN bus is recessive.

CAN BUS STATES

The CAN bus has two states during powered operation of the device; *dominant* and *recessive*. A dominant bus state is when the bus is driven differentially, corresponding to a logic low on the TXD and RXD pin. A recessive bus state is when the bus is biased to $V_{CC}/2$ via the high-resistance internal input resistors R_{IN} of the receiver, corresponding to a logic high on the TXD and RXD pins. See Figure 3 and Figure 4.

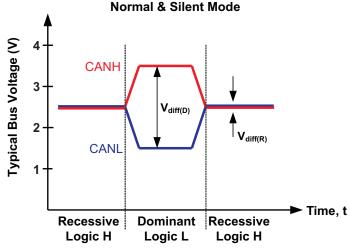


Figure 3. Bus States (Physical Bit Representation)

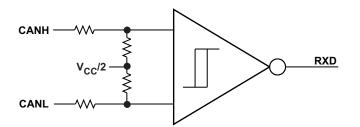


Figure 4. Simplified Recessive Common Mode Bias and Receiver

NORMAL MODE

Select the *normal mode* of device operation by setting S low. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on TXD to a differential output on CANH and CANL. The receiver is translating the differential signal from CANH and CANL to a digital output on RXD.

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SILENT MODE

Activate *silent mode* (receive only) by setting S high. The CAN driver is turned off while the receiver remains active and RXD outputs the received bus state.

APPLICATION NOTE: Silent mode may be used to implement *babbling idiot* protection, to ensure that the driver does not disrupt the network during a local fault. Silent mode may also be used in redundant systems to select or de-select the redundant transceiver (driver) when needed.

DRIVER AND RECEIVER FUNCTION TABLES

	INP	UTS	OUT	DRIVEN BUS	
DEVICE	S ⁽¹⁾⁽²⁾	TXD ⁽¹⁾⁽³⁾	CANH ⁽¹⁾	CANL ⁽¹⁾	STATE
		L	Н	L	Dominant
All Devices	L or Open	H or Open	Z	Z	Recessive
	Н	Х	Z	Z	Recessive

Table 2. Driver Function Table

(1) H = high level, L = low level, X= irrelevant, Z = common mode (recessive) bias to V_{CC} / 2. See Figure 3 and Figure 4 for bus state and common mode bias information.

(2) Devices have an internal pull down to GND on S pin. If S pin is open the pin will be pulled low and the device will be in normal mode.

(3) Devices have an internal pull up to V_{CC} on TXD pin. If the TXD pin is open the pin will be pulled high and the transmitter will remain in recessive (non-driven) state.

Table 3. Receiver Function Table

DEVICE MODE	CAN DIFFERENTIAL INPUTS V _{ID} = V _{CANH} - V _{CANL}	BUS STATE	RXD PIN ⁽¹⁾
Normal or Silent	$V_{ID} \ge 0.9 V$	Dominant	L ⁽²⁾
	0.5 V < V _{ID} < 0.9 V	?	?
	$V_{ID} \le 0.5 V$	Recessive	Н
	Open (V _{ID} ≈ 0 V)	Open	Н

(1) H = high level, L = low level, ? = indeterminate.

(2) RXD output remains dominant (low) as long as the bus is dominant. On SN65HVD257 device with RXD dominant timeout, once the bus has been dominant longer than the dominant timeout, t_{RXD_DTO}, the RXD pin will return recessive (high). See RXD Dominant Timeout (SN65HVD257) for a description of behavior during receiving a bus stuck dominant condition.

DIGITAL INPUTS AND OUTPUTS

5V V_{CC} Only Devices (SN65HVD255 and SN65HVD257):

The 5V V_{CC} device is supplied by a single 5V rail. The digital inputs are 5V and 3.3V compatible. This device has a 5V (V_{CC}) level RXD output. TXD is internally pulled up to V_{CC} and S is internally pulled down to GND.

APPLICATION NOTE: TXD is internally pulled up to V_{CC} and the S pin is internally pulled down to GND. However, the internal bias may only put the device into a known state if the pins float. The internal bias may be inadequate for system-level biasing. TXD pullup strength and CAN bit timing require special consideration when the SN65HVD25x devices are used with an open-drain TXD output on the CAN controller. An adequate external pullup resistor must be used to ensure that the CAN controller output of the μ P maintains adequate bit timing input to the SN65HVD25x.

5V V_{CC} with V_{RXD} RXD output Supply Devices (SN65HVD256):

This device is a 5V V_{CC} CAN transceiver with a separate supply for the RXD output, V_{RXD}. The digital inputs are 5V and 3.3V compatible. These devices have a V_{RXD}-level RXD output. TXD remains weakly pulled up to V_{CC}.

APPLICATION NOTE: On device versions with a V_{RXD} supply that shifts the RXD output level, the input pins of the device remain the same. TXD remains weakly pulled up to V_{CC} internally. Thus, a small I_{IH} current flows if the TXD input is used below V_{CC} levels.

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Product Folder Link(s): SN65HVD255 SN65HVD256 SN65HVD257



5V V_{cc} with FAULT Open-Drain Output Device (SN65HVD257):

This device has a FAULT output pin (open-drain). FAULT must be pulled up to V_{CC} or I/O supply level via an external resistor.

APPLICATION NOTE: Because the FAULT output pin is open-drain, it actively pulls down when there is no fault, and becomes high-impedance when a fault condition is detected. An external pullup resistor to the V_{CC} or I/O supply of the system must be used to pull the pin high to indicate a fault to the host microprocessor. The open-drain architecture makes the fault pin compatible with 3.3V and 5V I/O-level systems. The pullup current, selected by the pullup resistance value, should be as low as possible while achieving the desired voltage level output in the system with margin against noise.

PROTECTION FEATURES

TXD Dominant Timeout (DTO)

During normal mode (the only mode where the CAN driver is active), the TXD DTO circuit prevents the transceiver from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the timeout period t_{TXD_DTO} . The DTO circuit timer starts on a falling edge on TXD. The DTO circuit disables the CAN bus driver if no rising edge is seen before the timeout period expires. This frees the bus for communication between other nodes on the network. The CAN driver is re-activated when a recessive signal is seen on TXD pin, thus clearing the TXD DTO condition. The receiver and RXD pin still reflect the CAN bus, and the bus pins are biased to recessive level during a TXD dominant timeout.

APPLICATION NOTE: The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the t_{TXD_DTO} minimum, limits the minimum data rate. Calculate the minimum transmitted data rate by: Minimum Data Rate = 11/ t_{TXD_DTO} .

RXD Dominant Timeout (SN65HVD257)

The SN65HVD257 device has a RXD dominant timeout (RXD DTO) circuit that prevents a bus stuck dominant fault from permanently driving the RXD output dominant (low) when the bus is held dominant longer than the timeout period t_{RXD_DTO} . The RXD DTO timer starts on a falling edge on RXD (bus going dominant). If no rising edge (bus returning recessive) is seen before the timeout constant of the circuit expires (t_{RXD_DTO}), the RXD pin returns high (recessive). The RXD output is re-activated to mirror the bus receiver output when a recessive signal is seen on the bus, clearing the RXD dominant timeout. The CAN bus pins are biased to the recessive level during a RXD DTO.

APPLICATION NOTE: The minimum dominant RXD time allowed by the RXD DTO limits the minimum possible received data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits for the worst case transmission, where five successive dominant bits are followed immediately by an error frame. This, along with the t_{RXD_DTO} minimum, limits the minimum data rate. The minimum received data rate may be calculated by: Minimum Data Rate = 11/ t_{RXD_DTO} .

Thermal Shutdown

If the junction temperature of the device exceeds the thermal shut down threshold the device turns off the CAN driver circuits thus blocking the TXD to bus transmission path. The shutdown condition is cleared when the junction temperature drops below the thermal shutdown temperature of the device.

APPLICATION NOTE: During thermal shutdown the CAN bus drivers turn off; thus no transmission is possible from TXD to the bus. The CAN bus pins are biased to recessive level during a thermal shutdown, and the receiver to RXD path remains operational.

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Undervoltage Lockout

The supply pins have undervoltage detection that places the device in protected mode. This protects the bus during an undervoltage event on either the V_{CC} or V_{RXD} supply pins.

Table 4. Undervoltage Lockout 5V Only Devices (SN65HVD255 and SN65HVD257)

V _{cc}	DEVICE STATE	BUS OUTPUT	RXD
GOOD	Normal	Per Device State and TXD	Mirrors Bus
BAD	Protected	High Impedance	High Impedance (3-state)

Table 5. Undervoltage Lockout 5V and V_{RXD} Device (SN65HVD256)

V _{cc}	V _{RXD}	DEVICE STATE	BUS OUTPUT	RXD
GOOD	GOOD	Normal	Per Device State and TXD	Mirrors Bus
BAD	GOOD	Protected	High Impedance	High (Recessive)
GOOD	BAD	Protected	Recessive	High Impedance (3-state)
BAD	BAD	Protected	High Impedance	High Impedance (3-state)

APPLICATION NOTE: After an undervoltage condition is cleared and the supplies have returned to valid levels, the device typically resumes normal operation in 300 µs.

FAULT Pin (SN65HVD257)

If one or more of the faults (TXD-Dominant Timeout, RXD dominant Timeout, Thermal Shutdown or Undervoltage Lockout) occurs, the FAULT pin (open-drain) turns off, resulting in a high level when externally pulled up to V_{CC} or IO supply.

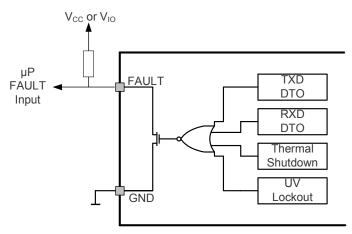


Figure 5. FAULT Pin Function Diagram and Application

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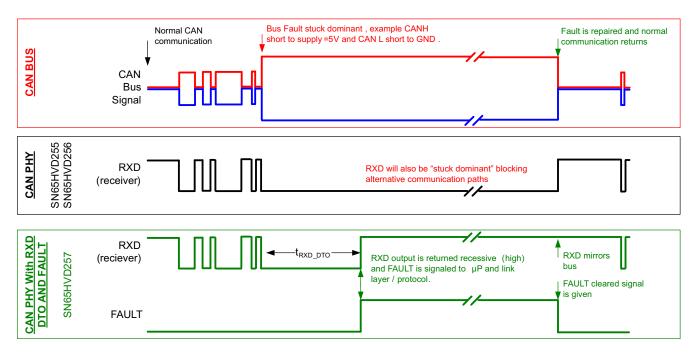


Figure 6. Example Timing Diagram for Devices With and Without RXD DTO and FAULT Pin

Unpowered Device

The device is designed to be an 'ideal passive' or 'no load' to the CAN bus if it is unpowered. The bus pins (CANH, CANL) have extremely low leakage currents when the device is unpowered so they will not load down the bus. This is critical if some nodes of the network will be unpowered while the rest of the of network remains in operation. The logic pins also have extremely low leakage currents when the device is unpowered to avoid loading down other circuits that may remain powered.

Floating Pins

The device has internal pull ups and pull downs on critical pins to place the device into known states if the pins float. The TXD pin is pulled up to V_{CC} to force a recessive input level if the pin floats. The S pin is pulled down to GND to force the device into normal mode if the pin floats.

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CAN Bus Short Circuit Current Limiting

The device has several protection features that limit the short circuit current when a CAN bus line is shorted. These include driver current limiting (dominant and recessive). The device has TXD dominant state time out to prevent permanent higher short circuit current of the dominant state during a system fault. During CAN communication the bus switches between dominant and recessive states with the data and control fields bits, thus the short circuit current may be viewed either as the instantaneous current during each bus state, or as a DC average current. For system current (power supply) and power considerations in the termination resistors and common-mode choke ratings, use the average short circuit current. Determine the ratio of dominant and recessive bits by the data in the CAN frame plus the following factors of the protocol and PHY that force either recessive or dominant at certain times:

- Control fields with set bits
- Bit stuffing
- Interframe space
- TXD dominant time out (fault case limiting)

These ensure a minimum recessive amount of time on the bus even if the data field contains a high percentage of dominant bits.

APPLICATION NOTE: The short circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short circuit currents. The average short circuit current may be calculated with the following formula:

 $I_{OS(AVG)} = \%Transmit \times [(\%REC_Bits \times I_{OS(SS)_REC}) + (\%DOM_Bits \times I_{OS(SS)_DOM})] + [\%Receive \times I_{OS(SS)_REC}]$ Where

- I_{OS(AVG)} is the average short circuit current
- %Transmit is the percentage the node is transmitting CAN messages
- %Receive is the percentage the node is receiving CAN messages
- %REC_Bits is the percentage of recessive bits in the transmitted CAN messages
- %DOM_Bits is the percentage of dominant bits in the transmitted CAN messages
- I_{OS(SS) REC} is the recessive steady state short circuit current
- I_{OS(SS)_DOM} is the dominant steady state short circuit current

APPLICATION NOTE: Consider the short circuit current and possible fault cases of the network when sizing the power ratings of the termination resistance and other network components.

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ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾

1.0				RATING	UNIT
1.1	V _{CC}	Supply voltage range		–0.3 to 6	V
1.2	V _{RXD}	RXD Output supply voltage range SN65HVD256		–0.3 to 6 and $V_{RXD} \le V_{CC} + 0.3$	V
1.3	V _{BUS}	CAN Bus I/O voltage range (CANH, CA	NL)	-27 to 40	V
1.4	V _{Logic_Input}	Logic input pin voltage range (TXD, S)		–0.3 to 6	V
1.5	V _{Logic_Output}	Logic output pin voltage range (RXD)	SN65HVD255, SN65HVD257	–0.3 to 6	V
1.6	V _{Logic_Output}	Logic output pin voltage range (RXD)	SN65HVD256	-0.3 to 6 and V _I \leq V _{RXD} + 0.3	V
1.7	I _{O(RXD)}	RXD (Receiver) output current		12	mA
1.8	I _{O(FAULT)}	FAULT output current	SN65HVD257	20	mA
1.9	TJ	Operating virtual junction temperature range (see THERMAL CHARACTERISTICS)		-40 to 150	°C
1.10	T _A	Ambient temperature range (see THER	MAL CHARACTERISTICS)	-40 to 125	°C

(1)Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

All voltage values, except differential I/O bus voltages, are with respect to ground terminal. (2)

TRANSIENT AND ELECTROSTATIC DISCHARGE PROTECTION

2.0		TE	ST CONDITIONS	RATING	UNIT
2.4	Lluman Dady Madel	All pins ⁽¹⁾	±2.5	kV	
2.1	Human-Body Model	CAN bus pins (CAN	±12	κv	
2.2	Charged-Device Model	All pins ⁽³⁾		±750	V
2.3	Machine Model	All pins ⁽⁴⁾		±250	V
2.4	IEC 61400-4-2 according to GIFT-ICT CAN EMC test spec ⁽⁵⁾	CAN bus pins (CANH, CANL) to GND		±8	kV
2.5			Pulse 1	-100	V
2.6	ISO7637 Transients according to GIFT - ICT CAN	CAN bus pins	Pulse 2	+75	V
2.7	.7 EMC test spec ⁽⁶⁾	(CANH, CANL)	Pulse 3a	-150	V
2.8			Pulse 3b	+100	V

(1) Tested in accordance to JEDEC Standard 22, Test Method A114.

Test method based upon JEDEC Standard 22 Test Method A114, CAN bus pins stressed with respect to GND. (2)

Tested in accordance to JEDEC Standard 22, Test Method C101. Tested in accordance to JEDEC Standard 22, Test Method A115. (3)

(4)

IEC 61000-4-2 is a system level ESD test. Results given here are specific to the GIFT-ICT CAN EMC Test specification conditions. (5) Different system level configurations may lead to different results.

ISO7637 is a system level transient test. Results given here are specific to the GIFT-ICT CAN EMC Test specification conditions. (6) Different system level configurations may lead to different results.

RECOMMENDED OPERATING CONDITIONS

3.0				MIN	MAX	UNIT
3.1	V _{CC}	Supply voltage		4.5	5.5	
3.2	V _{RXD}	RXD supply (SN65HVD256 only)			5.5	
3.3	$V_{I} \text{ or } V_{IC}$	CAN bus terminal voltage (separately or common mode)		-2	7	V
3.4	V _{ID}	CAN bus differential voltage		-6	6	v
3.5	V _{IH}	Logic HIGH level input (TXD, S)		2	5.5	
3.6	V _{IL}	Logic LOW level input (TXD, S)		0	0.8	
3.7	I _{OH(DRVR)}	CAN BUS Driver High level output current		-70		
3.8	I _{OL(DRVR)}	CAN BUS Driver Low level output current			70	
3.9	I _{OH(RXD)}	RXD pin HIGH level output current		-2		mA
3.10	I _{OL(RXD)}	RXD pin LOW level output current			2	
3.11	I _{O(FAULT)}	FAULT pin LOW level output current	SN65HVD257		2	
3.12	T _A	Operational free-air temperature (see THERMAL CHARACTERIST	ICS)	-40	125	°C

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ELECTRICAL CHARACTERISTICS

Overi				TEST CONDITIONS (COMMENT		TYP ⁽¹⁾		
4.0	PARAMETER SUPPLY CHARACTERISTICS		TEST CONDITIONS / COMMENT	MIN	ITP."	WAA	UNIT	
4.0	SUPPLY CH	ARACTERISTICS	No was al Marda					
4.1	-		Normal Mode (Driving Dominant)	See Figure 9, TXD = 0 V, R_L = 50- Ω , C_L = open, R_{CM} = open, S = 0V		60	85	
4.2			Normal Mode (Driving Dominant – bus fault)	See Figure 9, TXD = 0 V, S = 0V, CANH = -12V, R_L = open, C_L = open, R_{CM} = open		130	180	
4.3	I _{CC}	5-V Supply current	Normal Mode (Driving Dominant)	See Figure 9, TXD = 0 V, R_L = open (no load), C_L = open, R_{CM} = open, S = 0V		10	20	mA
4.4			Normal Mode (Recessive)	See Figure 9, TXD = V_{CC} , R_L = 50- Ω , C_L = open, R_{CM} = open, S = 0V		10	20	
4.5			Silent Mode	See Figure 9, TXD = V_{CC} , R_L = 50- Ω , C_L = open, R_{CM} = open, S = V_{CC}		2.5	5	
4.6	I _{RXD}	RXD Supply current (SN65HVD256 only)	All modes	RXD Floating, TXD = 0V			500	μΑ
4.7	UV _{VCC}	Undervoltage detect protected mode	ion on V_{CC} for		3.5		4.45	V
4.8	V _{HYS(UVVCC)}	Hysteresis voltage o	n UV _{VCC}			200		mV
4.9	UV _{RXD}	Undervoltage detect protected mode (SN			1.3		2.75	V
4.10	V _{HYS(UVRXD)}	Hysteresis voltage o (SN65HVD256 only)				80		mV
5.0	S PIN (MODI	E SELECT INPUT)						
5.1	V _{IH}	HIGH-level input vol	tage		2			V
5.2	V _{IL}	LOW-level input volt	age				0.8	V
5.3	IIH	HIGH-level input lea	kage current	$S = V_{CC} = 5.5 V$	7		100	μA
5.4	IIL	Low-level input leak	age current	S = 0 V, V _{CC} = 5.5 V	-1	0	1	μA
5.5	I _{LKG(OFF)}	Unpowered leakage	current	S = 5.5 V, V _{CC} = 0 V, V _{RXD} = 0 V	7	35	100	μA
6.0		N TRANSMIT DATA	INPUT)					
6.1	V _{IH}	HIGH level input vol	tage		2			V
6.2	V _{IL}	LOW level input volt	age				0.8	V
6.3	IIH	HIGH level input lea	kage current	$TXD = V_{CC} = 5.5 V$	-2.5	0	1	μA
6.4	IIL	Low level input leak	age current	$TXD = 0 V, V_{CC} = 5.5 V$	-100	-25	-7	μA
6.5	I _{LKG(OFF)}	Unpowered leakage	current	$TXD = 5.5 V, V_{CC} = 0 V, V_{RXD} = 0 V$	-1	0	1	μA
6.6	CI	Input Capacitance				3.5		pF
7.0			OUTPUT)					
7.1	V _{OH}	HIGH level output vo	bltage	See Figure 10, $I_0 = -2mA$. For devices with V _{RXD} supply V _{OH} = 0.8 × V _{RXD}	0.8×V _{CC}			V
7.2	V _{OL}	LOW level output vo	ltage	See Figure 10, I _O = 2mA.			0.4	V
7.3	I _{LKG(OFF)}			$RXD = 5.5 V, V_{CC} = 0 V, V_{RXD} = 0 V$	-1	0	1	μA
7.4	t _R Output signal rise time		See Receiver Rise Time					
7.5	t _F Output signal fall time		See Receiver Fall Time					

(1) All typical values are at 25°C and supply voltages of V_{CC} = 5 V and V_{RXD} = 5 V, R_L = 60 Ω .



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ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating conditions, $T_A = -40^{\circ}$ C to 125°C (unless otherwise noted). SN65HVD256 device $V_{RXD} = V_{CC}$.

		PARAMETER		125°C (unless otherwise noted). SN TEST CONDITIONS / COMMENT	MIN	TYP ⁽¹⁾	MAX	1
8.0		TCHING CHARACTE						0.01
8.1	t _{PROP(LOOP1)}	Total loop delay, driv receiver output (RXI dominant	/er input (TXD) to	See Figure 12, S = 0 V, $R_L = 60\Omega$,			150	
8.2	t _{PROP(LOOP2)}	Total loop delay, driv receiver output (RXI recessive		$C_L = 100 pF, C_{L_RXD} = 15 pF$			150	ns
8.3	I _{MODE}	Mode change time, from Normal to Silent or from Silent to Normal		See Figure 11			20	μS
9.0	DRIVER ELE	CTRICAL CHARACT	ERISTICS					
9.1	.,	Bus output voltage CANH	CANH	See Figure 3 and Figure 9, TXD = 0 V, S = 0 V, $R_L = 60\Omega$, $C_L = open$, $R_{CM} = open$	2.75		4.5	
9.2	V _{O(D)}	(dominant	CANL		0.5		2.25	V
9.3	V _{O®)}	Bus output voltage (recessive)	See Figure 3 and Figure 9, TXD = V_{CC} , $V_{RXD} = V_{CC}$, S = V_{CC} or 0 V ⁽²⁾ , R _L = open (no load), R _{CM} = open	2	0.5×V _{CC}	3	v
9.4				See Figure 3 and Figure 9, TXD = 0 V, S = 0 V, $45\Omega \le R_L \le 65\Omega$, $C_L = open$, $R_{CM} = 330\Omega$, $-2 V \le V_{CM} \le 7$ V, $4.75 V \le V_{CC} \le 5.25 V$	1.5		3	
9.5	V _{OD(D)}	Differential output vo	otage (dominant)	$ \begin{array}{l} \mbox{See Figure 3 and Figure 9, TXD = 0} \\ \mbox{V, S = 0 V, } 45\Omega \leq R_L \leq 65\Omega, \ C_L = \\ \mbox{open, } R_{CM} = 330\Omega, -2 \ V \leq V_{CM} \leq 7 \\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \$	1.25		3.2	V
9.6				See Figure 3 and Figure 9, TXD = V_{CC} , S = 0 V, R _L = 60 Ω , C _L = open, R _{CM} = open	-0.12		0.012	
9.7	V _{OD®)}	Differential output voltage (recessive)		See Figure 3 and Figure 9, TXD = V_{CC} , S = 0 V, R _L = open (no load), C _L = open, R _{CM} = open, -40°C ≤ T _A ≤ 85°C	-0.100		0.050	V
9.8	V _{SYM}	Output symmetry (dominant or recessive) $(V_{CC} - V_{O(CANH)} - V_{O(CANL)})$		See Figure 3 and Figure 9, S at 0 V, $R_L = 60\Omega$, $C_L =$ open, $R_{CM} =$ open	-0.4		0.4	v
9.9		short circuit steady-s	state output current,	See Figure 3 and Figure 14, V_{CANH} = 0 V, CANL = open, TXD = 0V	-160			~ ^
9.10	IOS(SS)_DOM	Dominant	•	See Figure 3 and Figure 14, $V_{CANL} = 32 V$, CANH = open, TXD = 0V			160	mA
9.11	I _{OS(SS)_REC}	short circuit steady-state output current, Recessive		See Figure 3 and Figure 14, -20 V \leq V _{BUS} \leq 32 V, Where V _{BUS} = CANH = CANL, TXD = V _{CC} , Normal and Silent Modes	-8		8	mA
9.12	Co	Output capacitance		See receiver input capacitance				
10.0	DRIVER SWI	TCHING CHARACTE	RISTICS					
10.1	t _{pHR}	Propagation delay ti Driver Recessive	me, HIGH TXD to			50	70	
10.2	t _{pLD}	Propagation delay ti Driver Dominant	me, LOW TXD to	See Figure 9, S = 0 V, $R_L = 60\Omega$,		40	70	
10.3	t _{sk(p)}	Pulse skew (t _{pHR} - t	_{pLD})	$C_L = 100 pF, R_{CM} = open$		10		ns
10.4	t _R	Differential output si]		10	30	1
10.5	t _F	Differential output si	onal fall time]		17	30	1

(2) For the bus output voltage (recessive) will be the same if the device is in normal mode with S pin LOW or if the device is in silent mode with the S pin is HIGH.

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ISTRUMENTS

EXAS

ELECTRICAL CHARACTERISTICS (continued)

		PARAMETER	TEST CONDITIONS / COMMENT	MIN	TYP ⁽¹⁾	MAX	UNIT
10.6	t _{R(10k)}	Differential output signal rise time, $R_L = 10k\Omega$	See Figure 9, S = 0 V, $R_L = 10k\Omega$,			35	
10.7	t _{F(10k)}	Differential output signal fall time, $R_L = 10k\Omega$	$_{CL}$ = 10pF, R_{CM} = open			100	ns
10.8	t _{TXD_DTO}	Dominant timeout ⁽³⁾	See Figure 13, $R_L = 60\Omega$, $C_L = open$	1175		3700	μs
11.0	RECEIVER	ELECTRICAL CHARACTERISTICS					
11.1	V _{IT+}	Positive-going input threshold voltage, normal mode	See Figure 10 and Table 3.			900	mV
11.2	V _{IT-}	Negative-going input threshold voltage, normal mode		500			mV
11.3	V _{HYS}	Hysteresis voltage (V _{IT+} - V _{IT-})			125		mV
11.4	I _{IOFF(LKG)}	Power-off (unpowered) bus input leakage current	$\label{eq:CANH} \begin{array}{l} CANH = CANL = 5 \ V, \ V_{CC} = 0 \ V, \\ V_{RXD} = 0 \ V \end{array}$			5.5	μA
11.5	CI	Input capacitance to ground (CANH or CANL)	$\begin{array}{l} TXD = V_{CC}, V_{RXD} = V_{CC}, V_{I} = 0.4 \sin \\ (4E6 \pi t) + 2.5 V \end{array}$		25		pF
11.6	C _{ID}	Differential input capacitance	$\begin{array}{l} TXD=V_{CC},V_{RXD}=V_{CC},V_{I}=0.4sin\\ (4E6\pit) \end{array}$		10		pF
11.7	R _{ID}	Differential input resistance		30		80	kΩ
11.8	R _{IN}	Input resistance (CANH or CANL)	$TXD = V_{CC} = V_{RXD} = 5 V, S = 0 V$	15		40	kΩ
11.9	R _{IN(M)}	Input resistance matching: [1 – ® _{IN(CANH}) / R _{IN(CANL)})] × 100%	$V_{(CANH)} = V_{(CANL)}, -40^{\circ}C \le T_A \le 85^{\circ}C$	-3%		3%	
12.0	RECEIVER	SWITCHING CHARACTERISTICS					
12.1	t _{pHR}	Propagation delay time, recessive input to high output			70	90	ns
12.2	t _{PDL}	Propagation delay time, dominant input to low output	See Figure 10, C _{L_RXD} = 15pF		70	90	ns
12.3	t _R	Output signal rise time			4	20	ns
12.4	t _F	Output signal fall time			4	20	ns
12.5	t _{RXD_DTO} ⁽⁴⁾	Receiver dominant time out (SN65HVD257 only) See Figure 7, $C_{L_RXD} = 15pF$		1380		4200	μs
13.0	FAULT Pin	(Fault Output), SN65HVD257 only					
13.1	I _{CH}	Output current high level	FAULT = V _{CC} , See Figure 8	-10		10	μA
13.2	I _{CL}	Output current low level	FAULT = 0.4 V, See Figure 8	5	12		mA

(3) The TXD dominant timeout (t_{TXD_DTO}) disables the driver of the transceiver once the TXD has been dominant longer than t_{TXD_DTO}, which releases the bus lines to recessive, preventing a local failure from locking the bus dominant. The driver may only transmit dominant again after TXD has been returned HIGH (recessive). While this protects the bus from local faults, locking the bus dominant, it limits the minimum data rate possible. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the t_{TXD_DTO} minimum, limits the minimum bit rate. The minimum bit rate may be calculated by: Minimum Bit Rate = 11/t_{TXD_DTO} = 11 bits / 1175 µs = 9.4 kbps.

(4) The RXD timeout (t_{RXD_DTO}) disables the driver of the transceiver once the RXD has been dominant longer than t_{RXD_DTO}, which releases the bus lines to recessive, preventing a local failure from locking the bus dominant. The driver may only transmit dominant again after RXD has been returned HIGH (recessive). While this protects the bus from local faults, locking the bus dominant, it limits the minimum data rate possible. The CAN protocol allows a maximum of eleven successive dominant bits (on RXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the t_{RXD_DTO} minimum, limits the minimum bit rate. The minimum bit rate may be calculated by: Minimum Bit Rate = 11/ t_{RXD_DTO} = 11 bits / 1380 µs = 8 kbps.



THERMAL CHARACTERISTICS

13.0		THERMAL METRIC ⁽¹⁾	TEST CONDITIONS		UNIT	
13.1	θ_{JA}	Junction-to-air thermal resistance	High-K thermal resistance ⁽²⁾	107.5		
13.2	θ_{JB}	Junction-to-board thermal resistance ⁽³⁾		48.9		
13.3	$\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance ⁽⁴⁾		56.7	°C/W	
13.4	Ψ_{JT}	Junction-to-top characterization parameter ⁽⁵⁾		12.1		
13.5	Ψ_{JB}	Junction-to-board characterization parameter ⁽⁶⁾		48.2	8.2	
13.6			$V_{CC} = 5 \text{ V}, V_{RXD} = 5 \text{ V}, T_J = 27^{\circ}\text{C}, R_L = 60\Omega, \text{ S at}$ 0 V, Input to TXD at 250 kHz, 25% duty cycle square wave, $C_{L_RXD} = 15 \text{ pF}$. Typical CAN operating conditions at 500kbps with 25% transmission (dominant) rate.	115		
13.7		Average power dissipation	$V_{CC} = 5.5 \text{ V}, V_{RXD} = 5.5 \text{ V}, T_J = 150^{\circ}\text{C}, R_L = 50\Omega$, S at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, $C_{L_RXD} = 15 \text{ pF}$. Typical high load CAN operating conditions at 1mbps with 50% transmission (dominant) rate and loaded network.		mW	
13.8		Thermal shutdown temperature		170	°C	
13.9		Thermal shutdown hysteresis		5	°C	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

(3) he junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

(4) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

(5) The junction-to-top characterization parameter, Ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

(6) The junction-to-board characterization parameter, Ψ_{JB} estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).



PARAMETER MEASUREMENT INFORMATION

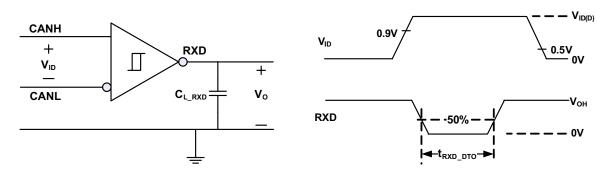


Figure 7. RXD Dominant Timeout Test Circuit and Measurement

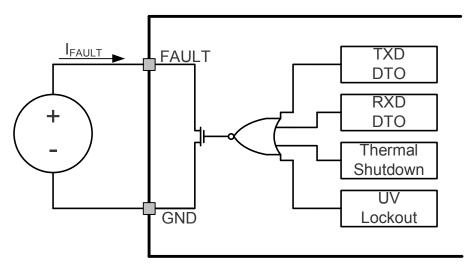


Figure 8. FAULT Test and Measurement

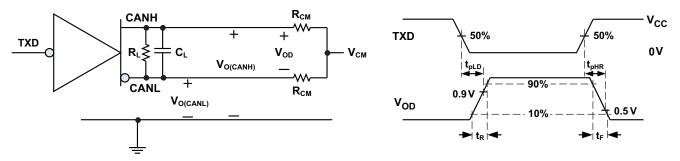


Figure 9. Driver Test Circuit and Measurement



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PARAMETER MEASUREMENT INFORMATION (continued)

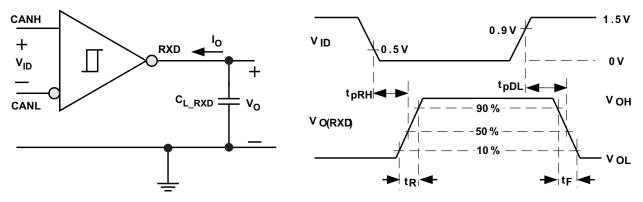


Figure 10. Receiver Test Circuit and Measurement

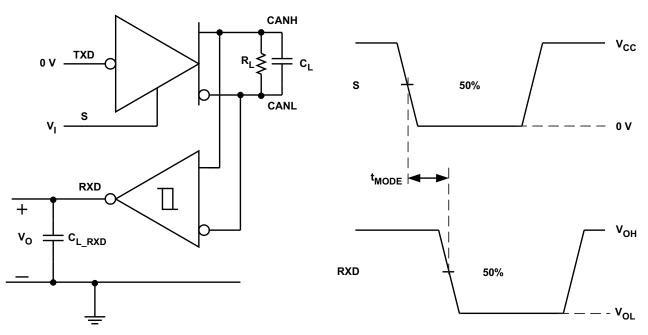
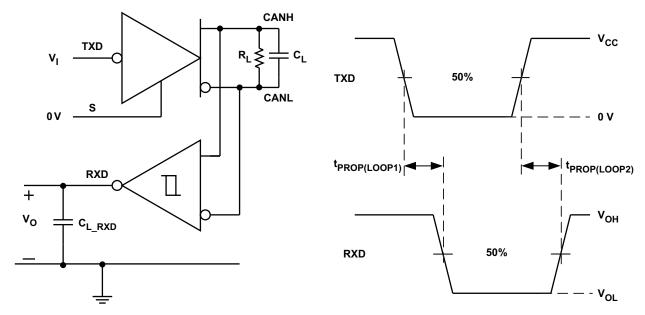


Figure 11. t_{MODE} Test Circuit and Measurement



PARAMETER MEASUREMENT INFORMATION (continued)





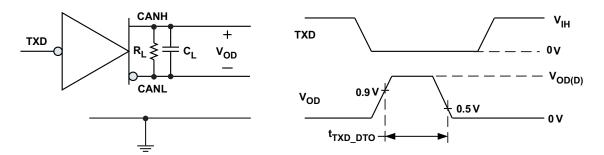


Figure 13. TXD Dominant Timeout Test Circuit and Measurement

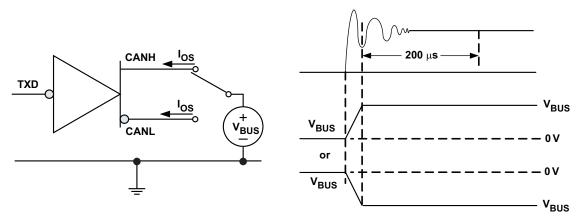


Figure 14. Driver Short Circuit Current Test and Measurement



APPLICATION INFORMATION

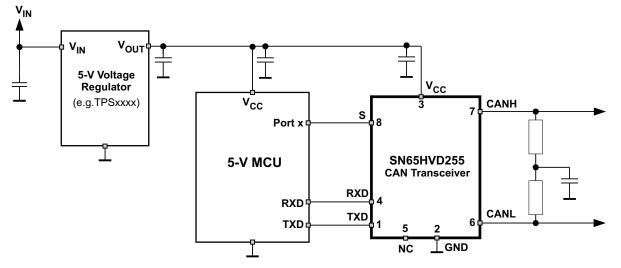


Figure 15. Typical 5V Application

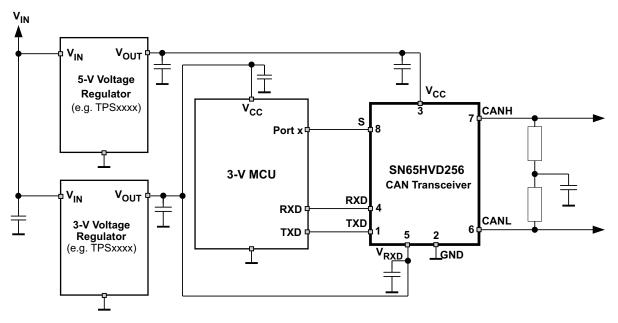


Figure 16. Typical 3.3V Application

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CAN TERMINATION

The CAN bus uses twisted pair cabling of 120Ω characteristic impedance in a bus topology. The bus requires proper termination at both ends with 120Ω resistors that match this impedance to avoid signal reflections. If nodes may be removed from the bus, the termination must be carefully placed so that it is not removed from the bus.

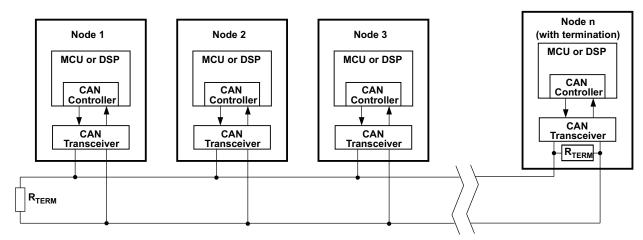
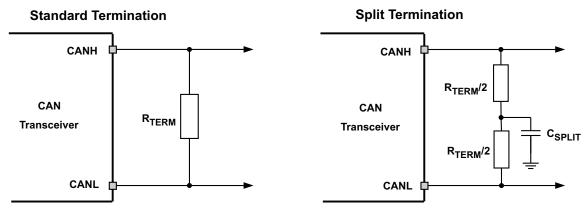


Figure 17. Typical CAN Bus

Termination may be a single 120Ω resistor at the end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common mode voltage of the bus is desired, then split termination may be used. (See Figure 18). Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltages at the start and end of message transmissions.







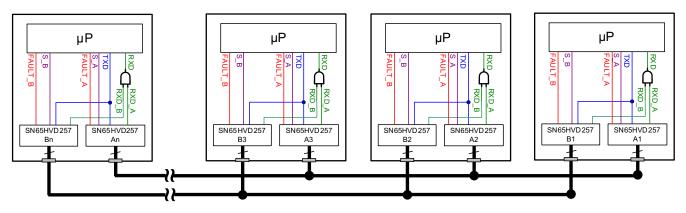
Example: Functional Safety Using the SN65HVD257 in a Redundant Physical Layer CAN Network Topology

CAN is a standard linear bus topology using 120Ω twisted pair cabling. The SN65HVD257 CAN device includes several features to use the CAN physical layer in nonstandard topologies with only one CAN link layer controller (µP) interface. This allows much greater flexibility in the physical topology of the bus while reducing the digital controller and software costs. The combination of RXD DTO and the FAULT output allows great flexibility, control and monitoring of these applications.

A simple example of this flexibility is to use two SN65HVD257 devices in parallel with an AND gate to achieve redundancy (parallel) of the physical layer (cabling & PHYs) in a CAN network.

For the CAN bit-wise arbitration to work, the RXD outputs of the transceivers must connect via AND gate logic so that a dominant bit (low) from any of the branches is received by the link layer logic (μ P), and appears to the link layer and above as a single physical network. The RXD DTO feature prevents a bus stuck dominant fault in a single branch from taking down the entire network by forcing the RXD pin for the transceivers on the branch with the fault back to the recessive after the t_{RXD_DTO} time. The remaining branch of the network continues to function. The FAULT pin of the transceivers on the branch with the fault indicates this via the FAULT output to their host processors, which diagnose the failure condition. The S pin (silent mode pin) may be used to put a branch in silent mode to check each branch for other faults. Thus it is possible to implement a robust and redundant CAN network topology in a very simple and low cost manner.

These concepts can be expanded into more complicated & flexible CAN network topologies to solve various system level challenges with a networked infrastructure.



- A. CAN nodes with termination are PHY A, PHY B, PHY An and PHY Bn.
- B. RXD DTO prevents a single branch-stuck-dominant condition from blocking the redundant branch via the AND logic on RXD. The transceivers signal a received bus stuck dominant fault via the FAULT pin. The system detects which branch is stuck dominant, and issues a system warning. Other network faults on a single branch that appear as recessive (not blocking the redundant network) may be detected through diagnostic routines, and using the Silent Mode of the PHYs to use only one branch at a time for transmission during diagnostic mode. This combination allows robust fault detection and recovery within single branches so that they may be repaired and again provide redundancy of the physical layer.

Figure 19. Typical Redundant Physical Layer Topology Using the SN65HVD257

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