



SLLS631D-MARCH 2007-REVISED DECEMBER 2008

LOW-POWER CAN TRANSCEIVER WITH BUS WAKE-UP

FEATURES

- Improved Drop-in Replacement for the TJA1040
- ±12 kV ESD Protection
- Low-Current Standby Mode with Bus Wake-up: 5 μA Typical
- Bus-Fault Protection of -27 V to 40 V
- Rugged Split-Pin Bus Stability
- Dominant Time-Out Function
- Power-Up/Down Glitch-Free Bus Inputs and Outputs
 - High Input Impedance with Low V_{CC}
 - Monotonic Outputs During Power Cycling
- DeviceNet Vendor ID # 806

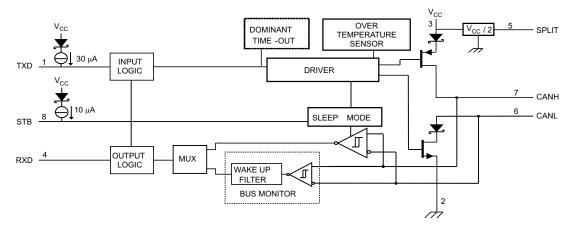
APPLICATIONS

- Battery Operated Applications
- Hand-Held Diagnostics
- Medical Scanning and Imaging
- HVAC
- Security Systems
- Telecom Base Station Status and Control
- SAE J1939 Standard Data Bus Interface
- NMEA 2000 Standard Data Bus Interface
- ISO 11783 Standard Data Bus Interface
- Industrial Automation
 - DeviceNet[™] Data Buses

DESCRIPTION

The SN65HVD1040 meets or exceeds the specifications of the ISO 11898 standard for use in applications employing a Controller Area Network (CAN). As CAN transceivers, these devices provide differential transmit and receive capability for a CAN controller at signaling rates of up to 1 megabit per second (Mbps). ⁽¹⁾

Designed for operation in especially harsh environments, the device features ± 12 kV ESD protection on the bus and split pins, cross-wire, overvoltage and loss of ground protection from -27 to 40 V, overtemperature shutdown, a -12 V to 12 V common-mode range, and will withstand voltage transients from -200 V to 200 V according to ISO 7637.



(1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (Continued)

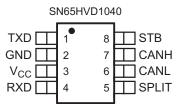
The STB input (pin 8) selects between two different modes of operation; high-speed or low-power mode. The high-speed mode of operation is selected by connecting STB to ground.

If a high logic level is applied to the STB pin of the SN65HVD1040, the device enters a low-power bus-monitor standby mode. While the SN65HVD1040 is in the low-power bus-monitor standby mode, a dominant bit greater than 5 μ s on the bus is passed by the bus-monitor circuit to the receiver output. The local protocol controller may then reactivate the device when it needs to transmit to the bus.

A dominant-time-out circuit in the SN65HVD1040 prevents the driver from blocking network communication during a hardware or software failure. The time-out circuit is triggered by a falling edge on TXD (pin 1). If no rising edge is seen before the time-out constant of the circuit expires, the driver is disabled. The circuit is then reset by the next rising edge on TXD.

The SPLIT output (pin 5) is available on the SN65HVD1040 as a $V_{CC}/2$ common-mode bus voltage bias for a split-termination network.

The SN65HVD1040 is characterized for operation from -40°C to 125°C.



ORDERING INFORMATION

PART NUMBER	DOMINANT TIME-OUT	LOW-POWER BUS MONITOR	PACKAGE ⁽¹⁾	MARKED AS	ORDERING NUMBER
SN65HVD1040	YES	YES	SOIC-8	VP1040	SN65HVD1040D (rail)
31030701040	TES	TES	3010-0	VF1040	SN65HVD1040DR (reel)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

				VALUE
V _{CC}	Supply voltage ⁽²⁾			–0.3 V to 7 V
V _{I(bus)}	Voltage range at any bu	s terminal (CANH, CANL, SPLI	Г)	–27 V to 40 V
I _{O(OUT)}	Receiver output current			-20 mA to 20 mA
	Voltage input, transient		-200 V to 200 V	
	IEC Contact Discharge	(IEC 61000-4-2)	Bus terminals vs GND	±6 kV
	Human bady model	JEDEC Standard 22,	Bus terminals vs GND	±12 kV
ESD	Human body model	Test Method A114-C.01	All pins	±4 kV
200	Field-Induced-Charged Device Model	JEDEC Standard 22, Test Method C101 All pins		±1 kV
	Machine model	ANSI/ESDS5.2-1996		±200 V
IEC			Bus terminals vs GND	±6 kV
VI	Voltage input range (TX	D, STB)		-0.5 V to 6 V
TJ	Junction temperature			–55°C to 170°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

(3) Tested in accordance with ISO 7637, test pulses 1, 2, 3a, 3b, 5, 6 & 7.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM MAX	UNIT
V _{CC}	Supply voltage		4.75	5.25	V
$V_{\text{I}} \text{ or } V_{\text{IC}}$	Voltage at any bus terminal (separately c	r common mode)	-12 ⁽¹⁾	12	V
V _{IH}	High-level input voltage	TXD, STB	2	5.25	V
V _{IL}	Low-level input voltage	170,318	0	0.8	V
V _{ID}	Differential input voltage		-6	6	V
	Lick lovel entruit entreat	Driver	-70		mA
IOH	High-level output current	Receiver	-2		
		Driver		70	
I _{OL}	Low-level output current	Receiver		2	mA
t _{SS}	Maximum pulse width to remain in standby			0.7	μs
TJ	Junction temperature		-40	150	= C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

SUPPLY CURRRENT

over operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	MIN	ТҮР	MAX	UNIT
		Dominant	$V_I = 0 V$, 60 Ω Load, STB at 0 V		50	70	~ ^
I _{CC}	Supply current, V _{CC}	Recessive	$V_I = V_{CC}$, STB at 0 V		6	10	mA
		Standby	STB at VCC, VI = VCC		5	12	μA

DEVICE SWITCHING CHARACTERISTICS

over recommended operating conditiions (unless otherwise noted)

	PARAMETER		MIN	ΤΥΡ ΜΑΧ	UNIT
t _{loop1}	Total loop delay, driver input to receiver output, Recessive to Dominant	STB at 0 V,	90	230	
t _{loop2}	Total loop delay, driver input to receiver output, Dominant to Recessive	See Figure 9	90	230	ns

INSTRUMENTS

FEXAS

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DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditiions (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT	
V _{O(D)}	Bus output voltage	CANH	$V_I = 0 V$, STB at 0 V, $R_L = 60 \Omega$, See Figure 1 and	2.9	3.4	4.5	V	
♥ O(D)	(Dominant)	CANL	Figure 2 0.8	0.8		1.75	v	
V _{O(R)}	Bus output voltage (Recessive)	$V_1 = 3 V$, STB at 0 V, See Figure 1 and Figure 2	2	2.5	3	V	
Vo	Bus output voltage (Standby)		$R_L = 60 \Omega$, STB at V _{CC} , See Figure 1 and Figure 2	-0.1		0.1	V	
V	Differential output valteres (Den	ain a nt)	$V_I = 0 V$, $R_L = 60 \Omega$, STB at 0 V, See Figure 1 and Figure 2, and Figure 3	1.5		3	V	
V _{OD(D)}	Differential output voltage (Dominant)		V_{I} = 0 V, R_{L} = 45 $\Omega,$ STB at 0 V, See Figure 1 and Figure 2	1.4		3	v	
V _{SYM}	Output symmetry (Dominant or Recessive) [V _{O(CANH)} + V _{O(CANL)}]		STB at 0 V, See Figure 2 and Figure 13	0.9×V _{CC}	V _{CC}	1.1×V _{CC}	V	
V _{OD(R)}	V _{OD(R)} Differential output voltage (Recessive)		V_{I} = 3 V, R_{L} = 60 $\Omega,$ STB at 0 V, See Figure 1 and Figure 2	-0.012		0.012	V	
- ()			V _I = 3 V, STB at 0 V, No Load	-0.5		0.05		
V _{OC(D)}	Common-mode output voltage (Dominant)		STB at 0 V. See Figure 8	2	2.3	3	V	
V _{OC(pp)}	Peak-to-peak common-mode o voltage	utput			0.3		V	
I _{IH}	High-level input current, TXD ir	nput	V _I at V _{CC}	-2		2	μA	
I _{IL}	Low-level input current, TXD in	put	V _I at 0 V	-50		-10	μA	
I _{O(off)}	Power-off TXD Leakage currer	ıt	V _{CC} at 0 V, TXD at 5 V			1	μΑ	
			V _{CANH} = -12 V, CANL Open, See Figure 12	-120	-72			
	Short-circuit steady-state output	ıt	V _{CANH} = 12 V, CANL Open, See Figure 12		0.36	1		
I _{OS(ss)}	current		V _{CANL} = -12 V, CANH Open, See Figure 12	-1	-0.5		mA	
			V _{CANL} = 12 V, CANH Open, See Figure 12		71	120		
Co	Output capacitance		See Input capacitance to ground in <i>RECEIVER</i> <i>ELECTRICAL CHARACTERISTICS</i> .					

(1) All typical values are at 25 = C with a 5-V supply.

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output		25	65	120	
t _{PHL}	Propagation delay time, high-to-low-level output		25	45	120	
t _{sk(p)}	Pulse skew (t _{PHL} - t _{PLH})	STB at 0 V, See Figure 4			25	ns
t _r	Differential output signal rise time			25		
t _f	Differential output signal fall time			50		
t _{en}	Enable time from silent mode to dominant	See Figure 7			10	μs
t _{dom}	Dominant time-out	See Figure 10	300	450	700	μs



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RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IT+}	Positive-going input threshold voltage				800	900	
V _{IT-}	Negative-going input threshold voltage	High-speed mode	STB at 0 V, See Table 1	500	650		mV
V _{hys}	Hysteresis voltage (V _{IT+} – V _{IT} –)	-	STB at V _{CC}	100	125		
VIT	Input threshold voltage	Standby mode	STB at V _{CC}	500		1150	
V _{OH}	High-level output voltage		$I_{O} = -2$ mA, See Figure 6	4	4.6		V
V _{OL}	Low-level output voltage		I _O = 2 mA, See Figure 6		0.2	0.4	V
I _{I(off)}	Power-off bus input current		CANH or CANL = 5 V, V_{CC} at 0 V, TXD at 0 V			5	μA
I _{O(off)}	Power-off RXD leakage current		V _{CC} at 0 V, RXD at 5 V			20	μA
CI	Input capacitance to ground, (CAN	IH or CANL)	TXD at 3 V, V _I = 0.4 sin (4E6πt) + 2.5 V		20		pF
C _{ID}	Differential input capacitance		TXD at 3 V, V _I = 0.4 sin (4E6πt)		10		pF
R _{ID}	Differential input resistance		TXD at 3 V, STD at 0 V	30		80	1.0
R _{IN}	Input resistance, (CANH or CANL)		TXD at 3 V, STD at 0 V	15	30	40	kΩ
R _{I(m)}	Input resistance matching [1 – (R _{IN (CANH)} / R _{IN (CANL)})] x 100	%	$V_{CANH} = V_{CANL}$	-3%	0%	3%	

(1) All typical values are at 25 = C with a 5-V supply.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditiions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{pLH}	Propagation delay time, low-to-high-level output		60	100	130	
t _{pHL}	Propagation delay time, high-to-low-level output STB at 0 V, TXD at 3 V, See		45	70	130	20
t _r	Output signal rise time	Figure 6		8		ns
t _f	Output signal fall time			8		
t _{BUS}	Dominant time required on bus for wake-up from standby ⁽¹⁾	STB at V _{CC} Figure 11	0.7		5	μs

(1) The device under test shall not signal a wake-up condition with dominant pulses shorter than t_{BUS} (min) and shall signal a wake-up condition with dominant pulses longer than t_{BUS} (max). Dominant pulses with a length between t_{BUS} (min) and t_{BUS} (max) may lead to a wake-up.

SPLIT-PIN CHARACTERISTICS

over recommended operating conditiions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Vo	Output voltage	–500 μA < I _O < 500 μA	0.3×V _{CC}	$0.5 \times V_{CC}$	$0.7 \times V_{CC}$	V
I _{O(stb)}	Standby mode leakage current	STB at 2 V, –12 V \leq V _O \leq 12 V	-5		5	μA

STB-PIN CHARACTERISTICS

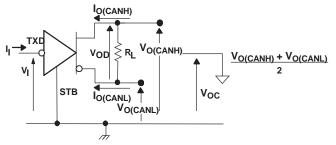
over recommended operating conditiions (unless otherwise noted)

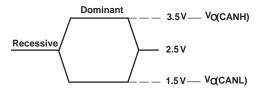
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{\rm H}$	High level input current	STB at 2 V	-10		0	μΑ
I_{IL}	Low level input current	STB at 0 V	-10		0	μΑ

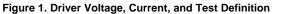


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PARAMETER MEASUREMENT INFORMATION









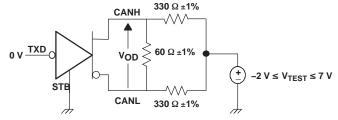


Figure 3. Driver V_{OD} Test Circuit

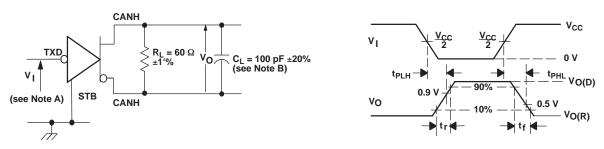


Figure 4. Driver Test Circuit and Voltage Waveforms

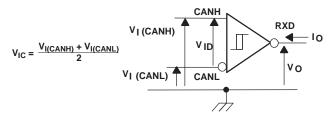


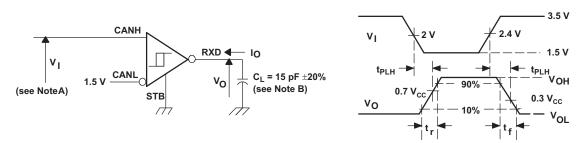
Figure 5. Receiver Voltage and Current Definitions

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PARAMETER MEASUREMENT INFORMATION (continued)



- A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 125 kHz, 50% duty cycle, t_r \leq 6 ns, t_f \leq 6ns, Z_O = 50 Ω .
- B. C_L includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 6. Receiver Test Circuit and Voltage Waveforms

	INPUT					
V _{CANH}	VCANL	V _{ID}		R		
–11.1 V	–12 V	900 mV	L	V _{OL}		
12 V	11.1 V	900 mV	L			
-6 V	–12 V	6 V	L			
12 V	6 V	6 V	L			
–11.5 V	–12 V	500 mV	Н	V _{OH}		
12 V	11.5 V	500 mV	Н			
–12 V	-6 V	6 V	Н			
6 V	12 V	6 V	Н			
Open	Open	Х	Н			

Table 1. Differential Input Voltage Threshold Test

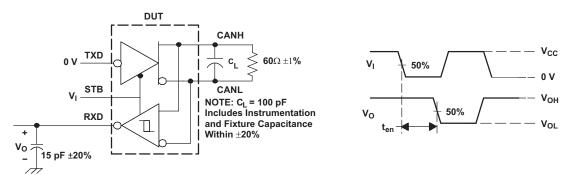
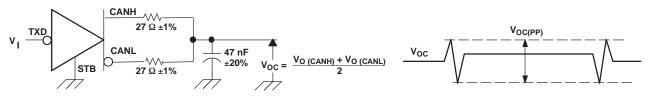


Figure 7. ten Test Circuit and Voltage Waveforms



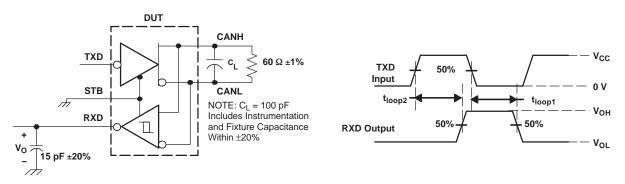
A. All V₁ input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or $t_f \le 6$ ns. Pulse Repetition Rate (PRR) = 125 kHz, 50% duty cycle.

Figure 8. Peak-to-Peak Common Mode Output Voltage Test and Waveform

TEXAS INSTRUMENTS

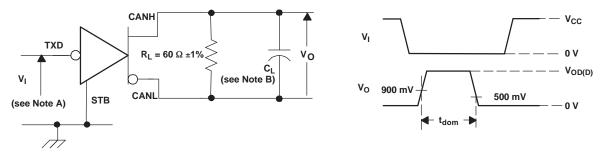
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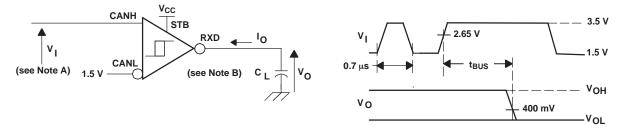
A. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator with the following characteristics: t_r or $t_f \le 6$ ns. Pulse Repetition Rate (PRR) = 125 kHz, 50% duty cycle.

Figure 9. t_{loop} Test Circuit and Voltage Waveforms



- A. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator with the following characteristics: t_r or $t_f \le 6$ ns. Pulse Repetition Rate (PRR) = 500 Hz, 50% duty cycle.
- B. $C_L = 100 \text{ pF}$ includes instrumentation and fixture capacitance within ±20%.

Figure 10. Dominant Time-Out Test Circuit and Waveform



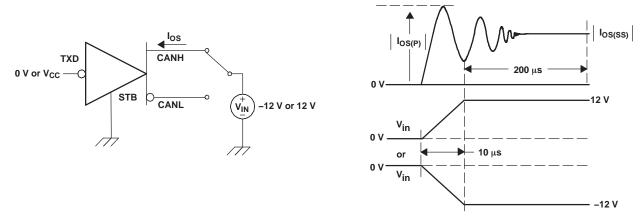
- A. For V_I bit width $\leq 0.7 \mu$ s, V₀ = V_{0H}. For V_II bit width $\geq 5 \mu$ s, V₀ = V_{0L}. V_I input pulses are supplied from a generator with the following characteristics; t_r or t_f ≤ 6 ns. Pulse Repetition Rate (PRR) = 50 Hz, 30% duty cycle.
- B. $C_L = 15 \text{ pF}$ includes instrumentation and fixture capacitance within ±20%.

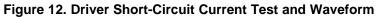
Figure 11. t_{BUS} Test Circuit and Waveform

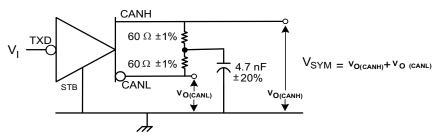


SN65HVD1040

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DEVICE INFORMATION

INP	UTS	OUTI	PUTS	BUS STATE
TXD	STB	CANH	CANL	
L	L	Н	L	DOMINANT
Н	L	Z	Z	RECESSIVE
Open	Х	Z	Z	RECESSIVE
Х	H or Open	Z	Z	RECESSIVE

Table 2. DRIVER FUNCTION TABLE⁽¹⁾

(1) H = high level; L = low level; X = irrelevant; Z = high impedance

Table 3. RECEIVER FUNCTION TABLE⁽¹⁾

DIFFERENTIAL INPUTS V _{ID} = CANH - CANL	STB	OUTPUT RXD	BUS STATE
$V_{ID} \ge 0.9 V$	L	L	DOMINANT
V _{ID} ≥ 1.15 V	H or Open	L	DOMINANT
$0.5 \text{ V} < \text{V}_{\text{ID}} < 0.9 \text{ V}$	Х	?	?
$V_{ID} \le 0.5 V$	Х	Н	RECESSIVE
Open	Х	Н	RECESSIVE

(1) H = high level; L = low level; X = irrelevant; ? = indeterminate; Z = high impedance

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
0	Thermel Desistance Junction to Air	Low-K Thermal Resistance ⁽¹⁾		211		°C/W
θ_{JA}	Thermal Resistance, Junction-to-Air	High-K Thermal Resistance		131		°C/W
θ_{JB}	Thermal Resistance, Junction-to-Board			53		°C/W
θ_{JC}	Thermal Resistance, Junction-to-Case			79		
P _D	Device Power Dissipation	$R_L = 60 \Omega$, S at 0 V, Input to TXD a 500kHz 50% duty-cycle square wave		112	170	mW
T_{JS}	Junction Temperature, Thermal Shutdo		190		°C	

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.

(2) Extended operation in thermal shutdown may affect device reliability, see the Application Information section.

TEXAS INSTRUMENTS

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DEVICE INFORMATION

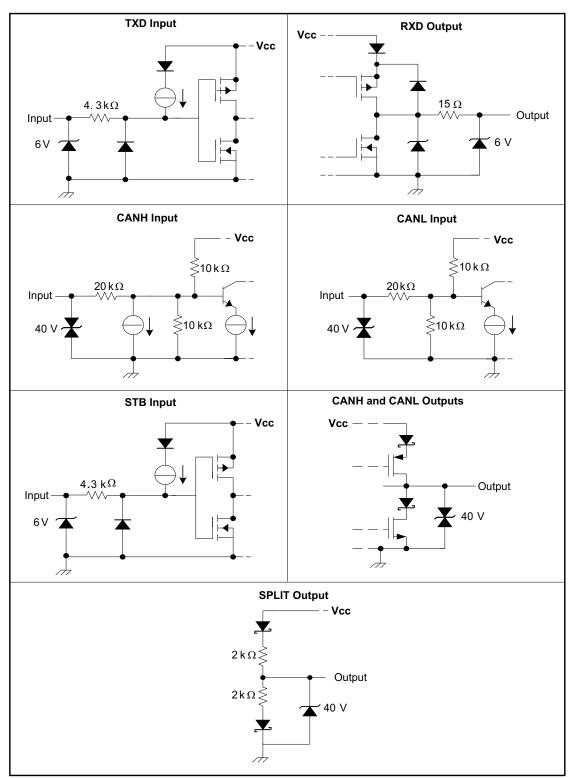
TJA1040 ⁽¹⁾	PARAMETER	HVD10xx							
	TJA1040 DRIVER SECTION								
V _{IH}	High-level input voltage	Recommended V _{IH}							
V _{IL}	Low-level input voltage	Recommended V _{IL}							
IIH	High-level input current	Driver I _{IH}							
IIL	Low-level input current	Driver I _{IL}							
	TJA1040 BUS SECTION								
V _{th(dif)}	Differential input voltage	Receiver V_{IT} and recommended V_{ID}							
V _{hys(dif)}	Differential input hysteresis	Receiver V _{hys}							
V _{O(dom)}	Dominant output voltage	Driver V _{O(D)}							
V _{O(reces)}	Recessive output voltage	Driver V _{O(R)}							
V _{i(dif)(th)}	Differential input voltage	Receiver V_{IT} and recommended V_{ID}							
V _{O(dif0(bus)}	Differential bus voltage	Driver $V_{OD(D)}$ and $V_{OD(R)}$							
I _{LI}	Power-off bus input current	Receiver I _{I(off)}							
I _{O(SC)}	Short-circuit output current	Driver I _{OS(SS)}							
R _{i(cm)}	CANH, CANL input resistance	Receiver R _{IN}							
R _{i(def)}	Differential input resistance	Receiver R _{ID}							
R _{i(cm) (m)}	Input resistance matching	Receiver R _{I (m)}							
C _{i(cm)}	Input capacitance to ground	Receiver C _I							
C _{i(dif)}	Differential input capacitance	Receiver C _{ID}							
	TJA1040 RECEIVER SECTI	ON							
I _{OH}	High-level output current	Recommended I _{OH}							
I _{OL}	Low-level output current	Recommended I _{OL}							
	TJA1040 SPLIT PIN SECTION	ON							
Vo	Reference output voltage	Vo							
	TJA1040 TIMING SECTIO	<u>N</u>							
t _{d(TXD-BUSon)}	Delay TXD to bus active	Driver t _{PLH}							
$t_{d(TXD-BUSoff)}$	Delay TXD to bus inactive	Driver t _{PHL}							
t _{d(BUSon-RXD)}	Delay bus active to RXD	Receiver t _{PHL}							
t _{d(BUSoff-RXD)}	Delay bus inactive to RXD	Receiver t _{PLH}							
t _{PD(TXD-RXD)}	Prop delay TXD to RXD	Device t_{LOOP1} and t_{LOOP2}							
t _{d(stb-norm)}	Enable time from standby to dominant	Driver t _{en}							
	TJA1040 STB PIN SECTIO	DN							
V _{IH}	High-level input voltage	Recommended V _{IH}							
VIL	Low-level input voltage	Recommended V _{IL}							
IIH	High-level input current	I _{IH}							
IIL	Low-level input current	IIL							

Table 4. Parametric Cross Reference With the TJA1040

(1) From TJA1040 Product Specification, Philips Semiconductors, 2003 February 19.



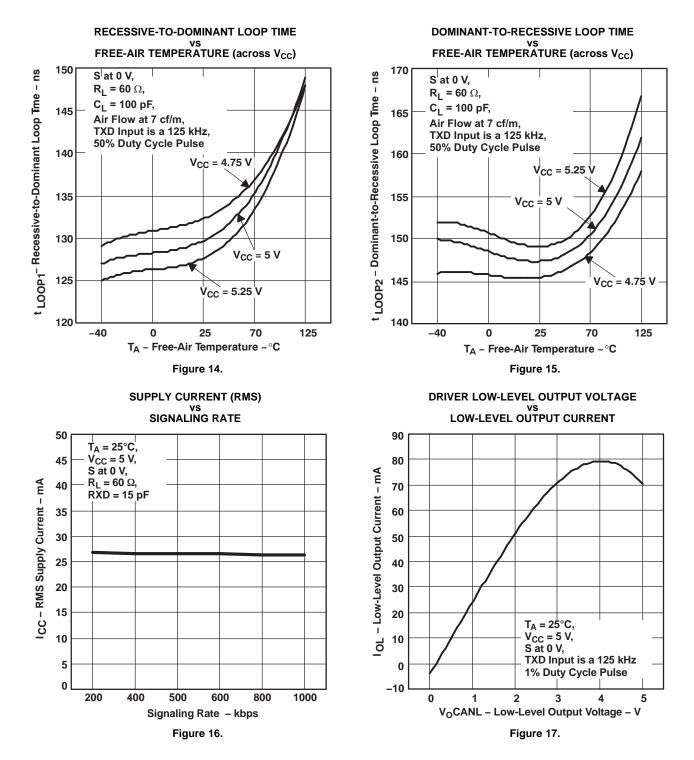
Equivalent Input and Output Schematic Diagrams





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TYPICAL CHARACTERISTICS



-80

-70

-60

-50

-40

-30

-20

-10

-0

50

45

40

35

30

25

20

15

10

<u>_</u> 5 0

Differential Driver Output Current – mA

0

T_A = 25°C. $V_{CC} = 5 V,$

S at 0 V,

R_L = 60 Ω,

2

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1

I OH – High-Level Output Current – mA

DRIVER HIGH-LEVEL OUTPUT VOLTAGE DRIVER DIFFERENTIAL OUTPUT VOLTAGE VS HIGH-LEVEL OUTPUT CURRENT vs FREE-AIR TEMPERATURE (across V_{CC}) 3 $T_{A} = 25 C,$ $V_{CC} = 5 V,$ Dominant Driver Differential Output Voltage – V $V_{CC} = 5V$ S at 0 V, $V_{CC} = 5.25 V$ 2.5 TXD Input is a 125 kHz 1% Duty Cycle Pulse 2 $V_{CC} = 4.75 V$ 1.5 1 S at 0 V, $R_{L} = 60 \Omega$, Air Flow at 7 cf/m, 0.5 TXD Input is a 125 kHz 1% Duty Cycle Pulse 0 3 1 2 4 5 -40 70 125 0 25 V_OCANH - High-Level Output Voltage - V T_A – Free-Air Temperature – °C Figure 18. Figure 19. DRIVER OUTPUT CURRENT **RECEIVER OUTPUT VOLTAGE** vs SUPPLY VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE 6 V_{IT+} VIT-5 V_O- Receiver Output Voltage - V V_{CM} = 12 V TXD Input is a 125 kHz 1% Duty Cycle Pulse V_{CM} = 2.5 V 3 _{СМ} = –12 V 2 T_A = 25°C, $V_{CC} = 5 V,$ S at 0 V, RXD = 15 pF0 0.60 0.65 0.70 0.75 0.80 0.85 0.85 0.80 0.75 0.70 0.65 0.60 4 4.5 5 3 3.5 5.25 V_{CC} – Supply Voltage – V

TYPICAL CHARACTERISTICS (continued)



V_{ID} – Differential Input Voltage – V

Figure 21.

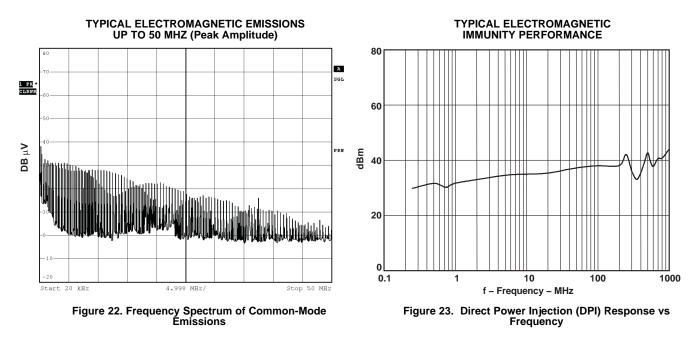


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TYPICAL CHARACTERISTICS (continued)





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APPLICATION INFORMATION

CAN Basics

The basics of arbitration require that the receiver at the sending node designate the first bit as dominant or recessive after the initial wave of the first bit of a message travels to the most remote node on a network and back again. Typically, this "sample" is made at 75% of the bit width, and within this limitation, the maximum allowable signal distortion in a CAN network is determined by network electrical parameters.

Factors to be considered in network design include the approximately 5 ns/m propagation delay of typical twisted-pair bus cable; signal amplitude loss due to the loss mechanisms of the cable; and the number, length, and spacing of drop-lines (stubs) on a network. Under strict analysis, variations among the different oscillators in a system also need to be accounted for with adjustments in signaling rate and stub and bus length. Table 5 lists the maximum signaling rates achieved with the SN65HVD1040 with several bus lengths of category 5, shielded twisted pair (CAT 5 STP) cable.

Bus Length (m)	Signaling Rate (kbps)
30	1000
100	500
250	250
500	125
1000	62.5

Table 5. Maximum Signaling Rates for Various Cable Lengths

The ISO 11898 Standard specifies a maximum bus length of 40 m and maximum stub length of 0.3 m with a maximum of 30 nodes. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. (Note: Non-standard application may come with a trade-off in signaling rate.) A large number of nodes requires a transceiver with high input impedance such as the HVD1040.

The Standard specifies the interconnect to be a single twisted-pair cable (shielded or unshielded) with 120 Ω characteristic impedance (Z₀). Resistors equal to the characteristic impedance of the line terminate both ends of the cable to prevent signal reflections. Unterminated drop-lines connect nodes to the bus and should be kept as short as possible to minimize signal reflections.

Connectors, while not specified by the standard should have as little effect as possible on standard operating parameters such as capacitive loading. Although unshielded cable is used in many applications, data transmission circuits employing CAN transceivers are usually used in applications requiring a rugged interconnection with a wide common-mode voltage range. Therefore, shielded cable is recommended in these electronically harsh environments, and when coupled with the Standard's –2-V to 7-V common-mode range of tolerable ground noise, helps to ensure data integrity. The HVD1040 enhances the Standard's insurance of data integrity with an extended –12 V to 12 V range of common-mode operation.



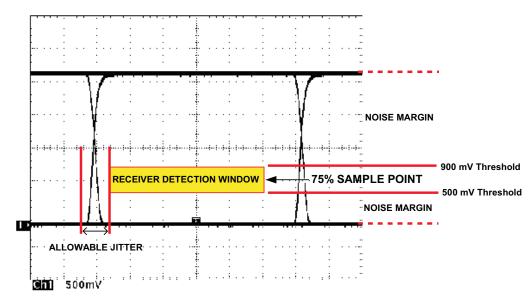


Figure 24. Typical CAN Differential Signal Eye-Pattern

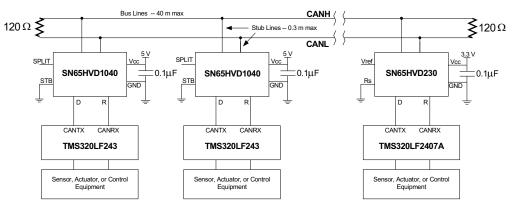
An eye pattern is a useful tool for measuring overall signal quality. As displayed in Figure 25, the differential signal changes logic states in two places on the display, producing an "eye." Instead of viewing only one logic crossing on the scope, an entire "bit" of data is brought into view. The resulting eye pattern includes all of the effects of systemic and random distortion, and displays the time during which a signal may be considered valid.

The height of the eye above or below the receiver threshold voltage level at the sampling point is the noise margin of the system. Jitter is typically measured at the differential voltage zero-crossing during the logic state transition of a signal. Note that jitter present at the receiver threshold voltage level is considered by some to be a more effective representation of the jitter at the input of a receiver.

As the sum of skew and noise increases, the eye closes and data is corrupted. Closing the width decreases the time available for accurate sampling, and lowering the height enters the 900 mV or 500 mV threshold of a receiver.

Different sources induce noise onto a signal. The more obvious noise sources are the components of a transmission circuit themselves; the signal transmitter, traces and cables, connectors, and the receiver. Beyond that, there is a termination dependency, cross-talk from clock traces and other proximity effects, V_{CC} and ground bounce, and electromagnetic interference from near-by electrical equipment.

The balanced receiver inputs of the HVD1040 mitigate most all sources of signal corruption, and when used with a quality shielded twisted-pair cable, help insure data integrity.







Thermal Shutdown

The SN65HVD1040 has a thermal shutdown that turns off the driver outputs when the junction temperature nears 190°C. This shutdown prevents catastrophic failure from bus shorts, but does not protect the circuit from possible damage. The user should strive to maintain recommended operating conditions, and not exceed absolute maximum ratings at all times. If the SN65HVD1040 is subjected to many or long durations faults that can put the device into thermal shutdown, it should be replaced.



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN65HVD1040D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Add to cart
SN65HVD1040DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Add to cart
SN65HVD1040DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Add to cart
SN65HVD1040DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Add to cart

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN65HVD1040 :

PACKAGE OPTION ADDENDUM



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10-Nov-2011

• Automotive: SN65HVD1040-Q1

NOTE: Qualified Version Definitions:

• Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal	
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Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD1040DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1



PACKAGE MATERIALS INFORMATION

17-Dec-2008



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD1040DR	SOIC	D	8	2500	346.0	346.0	29.0

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE

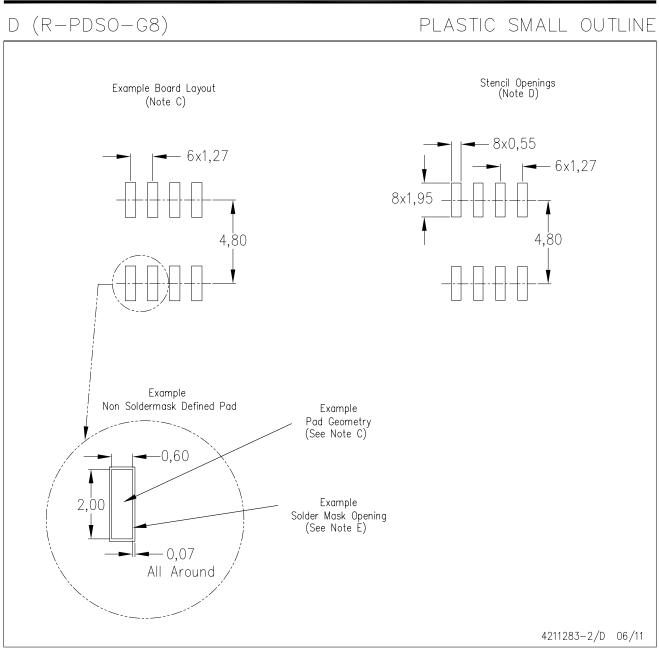


NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.



LAND PATTERN DATA



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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