



3.3-V CAN TRANSCEIVER

FEATURES

- Bus-Pin Fault Protection Exceeds ±36 V
- Bus-Pin ESD Protection Exceeds 16-kV HBM
- Compatible With ISO 11898
- Signaling Rates⁽¹⁾ up to 1 Mbps
- Extended -7-V to 12-V Common-Mode Range
- High-Input Impedance Allows for 120 Nodes
- LVTTL I/Os Are 5-V Tolerant
- Adjustable Driver Transition Times for Improved Signal Quality
- Unpowered Node Does Not Disturb the Bus
- Low-Current Standby Mode . . . 200-μA Typical
- Thermal Shutdown Protection
- Power-Up/Down Glitch-Free Bus Inputs and Outputs
 - High Input Impedance With Low V_{CC}
 - Monolithic Output During Power Cycling
- Loopback for Diagnostic Functions Available
- DeviceNet Vendor ID #806
- (1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Available in Military (-55°C/125°C)
 Temperature Range⁽¹⁾
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability
- (1) Additional temperature ranges available contact factory

APPLICATIONS

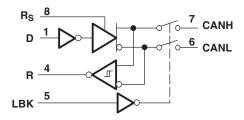
- CAN Data Bus
- Industrial Automation
 - DeviceNet[™] Data Buses
 - Smart Distributed Systems (SDS™)
- SAE J1939 Standard Data Bus Interface
- NMEA 2000 Standard Data Bus Interface
- ISO 11783 Standard Data Bus Interface

DESCRIPTION

The SN65HVD233 is used in applications employing the controller area network (CAN) serial communication physical layer in accordance with the ISO 11898 standard. As a CAN transceiver, it provides transmit and receive capability between the differential CAN bus and a CAN controller, with signaling rates up to 1 Mbps.

Designed for operation in especially harsh environments, the device features cross-wire, overvoltage and loss of ground protection to ± 36 V, with overtemperature protection and common-mode transient protection of ± 100 V. This device operates over a -7-V to 12-V common-mode range with a maximum of 60 nodes on a bus.

FUNCTIONAL BLOCK DIAGRAM



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This device has limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

If the common-mode range is restricted to the ISO-11898 Standard range of -2 V to 7 V, up to 120 nodes may be connected on a bus. This transceiver interfaces the single-ended CAN controller with the differential CAN bus found in industrial, building automation, and automotive applications.

The R_S (pin 8) of the SN65HVD233 provides for three modes of operation: high-speed, slope control, or low-power standby mode. The high-speed mode of operation is selected by connecting R_S directly to ground, allowing the driver output transistors to switch on and off as fast as possible with no limitation on the rise and fall slope. The rise and fall slope can be adjusted by connecting a resistor to ground at R_S , since the slope is proportional to the pin's output current. Slope control is implemented with a resistor value of 10 k Ω to achieve a slew rate of \approx 15 V/ μ s and a value of 100 k Ω to achieve \approx 2.0 V/ μ s slew rate. For more information about slope control, refer to the application information section.

The SN65HVD233 enters a low-current standby mode during which the driver is switched off and the receiver remains active if a high logic level is applied to R_S. The local protocol controller reverses this low-current standby mode when it needs to transmit to the bus.

A logic high on the loopback LBK (pin 5) of the SN65HVD233 places the bus output and bus input in a high-impedance state. The remaining circuit remains active and available for driver to receiver loopback, self-diagnostic node functions without disturbing the bus.

AVAILABLE OPTIONS

PART NUMBER			DIAGNOSTIC LOOPBACK	AUTOBAUD LOOPBACK
SN65HVD233	200-μA standby mode	Adjustable	Yes	No

ORDERING INFORMATION(1)

T _A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C	SOIC - D	Reel of 2500	SN65HVD233MDREP	H233EP

⁽¹⁾ For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

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⁽²⁾ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



POWER DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD	T _A ≤ 25°C POWER RATING	DERATING FACTOR ⁽¹⁾ ABOVE T _A = 25°C	T _A = 85°C POWER RATING	T _A = 125°C POWER RATING
D	Low-K	596.6 mW	5.7 mW/°C	255.7 mW	28.4 mW
D	High-K	1076.9 mW	10.3 mW/°C	461.5 mW	51.3 mW

⁽¹⁾ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

ABSOLUTE MAXIMUM RATINGS(1) (2)

over operating free-air temperature range (unless otherwise noted)

				VALUE	UNIT
V_{CC}	Supply voltage range			-0.3 to 7	V
	Voltage range at any bu	ge range at any bus terminal (CANH or CANL)		-36 to 36	V
	Voltage input range, trai	nsient pulse, CANH and CANL	-100 to 100	V	
VI	Input voltage range, (D,	R, R _S , LBK)		-0.5 to 7	V
Io	Receiver output current			-10 to 10	mA
	Electrostatic discharge	Human Body Model (3)	CANH, CANL and GND	16	kV
		Human Body Model (3)	All pins	3	kV
	Electrostatic discharge	Charged-Device Mode (4)	All pins	1	kV
	Continuous total power	dissipation	See Dissipation Rating Table		
T_{J}	Operating junction temp	erature		150	°C

⁽¹⁾ Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

			MIN	TYP MAX	UNIT
V_{CC}	Supply voltage		3	3.6	
	Voltage at any bus terminal (separat	ely or common mode)	-7	12	
V_{IH}	High-level input voltage	D, LBK	2	3.6 12 5.5 0.8 6 100 5.5	V
V_{IL}	Low-level input voltage	D, LBK	0	0.8	
V_{ID}	Differential input voltage		-6	6	
	Resistance from R _S to ground		0	100	kΩ
$V_{I(Rs)}$	Input Voltage at R _S for standby			5.5	V
	Lligh lovel output ourrent	Driver	-50		A
Іон	High-level output current	Receiver	-10		mA
	Low lovel output ourrent	Driver		50	A
I _{OL}	Low-level output current	Receiver		10	mA
T_{J}	Operating junction temperature			150	°C
T _A	Operating free-air temperature ⁽¹⁾		-55	125	°C

⁽¹⁾ Maximum free-air temperature operation is allowed as long as the device maximum junction temperature is not exceeded.

⁽²⁾ All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

⁽³⁾ Tested in accordance with JEDEC Standard 22, Test Method A114-A.

⁽⁴⁾ Tested in accordance with JEDEC Standard 22, Test Method C101.

DRIVER ELECTRICAL CHARACTERISTICS

	PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT				
.,	Bus output voltage	(CANH	D. O.V. D. O.V. Coo Figure 4 and Figure 2	2.45		V_{CC}	V			
$V_{O(D)}$	(Dominant)	(CANL	$D = 0 \text{ V}, R_S = 0 \text{ V}, \text{ See Figure 1 and Figure 2}$	0.5		1.25	V			
	Bus output voltage	(CANH	D. 21/ B. O.V. See Figure 1 and Figure 2		2.3		V			
Vo	(Recessive)	(CANL	D = 3 V, R _S = 0 V, See Figure 1 and Figure 2		2.3		V			
	Differential autout ve	oltogo (Dom	nin ant\	D = 0 V, R _S = 0 V, See Figure 1 and Figure 2	1.5	2	3	V			
$V_{OD(D)}$	Differential output vo	ollage (Doll	imani)	D = 0 V, R _S = 0 V, See Figure 2 and Figure 3	1.2	2	3	V			
	Differential autoutus	oltono (Doo	:	D = 3 V, R _S = 0 V, See Figure 1 and Figure 2	-120		12	mV			
V _{OD}	Differential output vo	oltage (Rec	essive)	D = 3 V, R _S = 0 V, No load	-0.5		0.05	V			
V _{OC(pp)}	Peak-to-peak comm	ion-mode oi	utput voltage	See Figure 9		1		V			
I _{IH}	High-level input curr	ent [D,LBK	D = 2 V	-30		30	μΑ			
I _{IL}	Low-level input curre	ent [D, LBK	D = 0.8 V	-30		30	μΑ			
	-			V _{CANH} = -7 V, CANL Open, See Figure 12	-250						
	Chart aireasit autaut	0rant		V _{CANH} = 12 V, CANL Open, See Figure 12			1	A			
I _{OS}	Short-circuit output of	current		V _{CANL} = -7 V, CANH Open, See Figure 12	-1			mA			
				V _{CANL} = 12 V, CANH Open, See Figure 12			250				
Co	Output capacitance			See receiver input capacitance							
I _{IRs(s)}	R _S input current for	standby		$R_{S} = 0.75 V_{CC}$	-10			μΑ			
		Standby		$R_S = V_{CC}$, $D = V_{CC}$, LBK = 0 V		200	600	μΑ			
I _{CC}	Supply current	Supply current	Supply current	Supply current	Dominant		$D = 0 \text{ V}$, No load, LBK = 0 V, $R_S = 0 \text{ V}$			6	A
	Recessive		•	$D = V_{CC}$, No load, LBK = 0 V, $R_S = 0 \text{ V}$			6	mA			

⁽¹⁾ All typical values are at 25°C and with a 3.3 V supply.



DRIVER SWITCHING CHARACTERISTICS

	PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
		R _S = 0 V, See Figure 4		35	95	
t _{PLH}	Propagation delay time, low-to-high-level output	R_S with 10 k Ω to ground, See Figure 4		70	125	ns
	ion to high level earpar	R_S with 100 k Ω to ground, See Figure 4		500	870	
		R _S = 0 V, See Figure 4		70	120	
t _{PHL}	Propagation delay time, high-to-low-level output	R_S with 10 k Ω to ground, See Figure 4		130	180	ns
	riigit to low level output	R_S with 100 k Ω to ground, SeeFigure 4		870	1200	
		R _S = 0 V, See Figure 4		35		
t _{sk(p)}	Pulse skew (t _{PHL} - t _{PLH})	R_S with 10 k Ω to ground, See Figure 4		60		ns
		R_S with 100 k Ω to ground, SeeFigure 4		370		
t _r	Differential output signal rise time	D OV See Figure 4	20		70	
t _f	Differential output signal fall time	R _S = 0 V, See Figure 4	20		70	ns
t _r	Differential output signal rise time	D. with 40 kO to ground Coo Figure 4	30		135	
t _f	Differential output signal fall time	R_S with 10 kΩ to ground, See Figure 4	30		135	ns
t _r	Differential output signal rise time	D with 100 kO to ground See Figure 1	300		1400	20
t _f	Differential output signal fall time	R_S with 100 kΩ to ground, See Figure 4	300		1400	ns
t _{en(s)}	Enable time from standby to dominant	See Figure 8		0.6	1.5	μs

⁽¹⁾ All typical values are at 25°C and with a 3.3 V supply. Timing parameters are characterized but not production tested.

RECEIVER ELECTRICAL CHARACTERISTICS

	PARAMI	ETER	TEST CO	NDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IT+}	Positive-going inp	out threshold voltage (2)				750	900	
V _{IT}	Negative-going in voltage (2)	put threshold	LBK = 0 V, See Table 1		500	650		mV
V _{hys}	Hysteresis voltag	e (V _{IT+} – V _{IT})				100		
V_{OH}	High-level output	voltage	I _O = -4 mA, See Figure 6		2.4			V
V_{OL}	Low-level output	voltage	I _O = 4 mA, See Figure 6				0.4	V
			CANH or CANL = 12 V		150		500	
	Bus input current		$V_{CC} = 0 \text{ V}$ Other bus pin = 0 V,	200		600		
II			CANH or CANL = -7 V		-610		-150	μΑ
		-450		-130				
Cı	Input capacitance	e (CANH or CANL)	Pin-to-ground, V _I = 0.4 sin LBK = 0 V	$(4E6\pi t) + 0.5V, D = 3 V,$		40		
C _{ID}	Differential input	capacitance	Pin-to-pin, $V_I = 0.4 \sin (4E6 LBK = 0 V)$	6πt) + 0.5V, D = 3 V,		20		pF
R_{ID}	Differential input	resistance	D 2V I DK 2V		40		100	1.0
R _{IN}	Input resistance ((CANH or CANL)	D = 3 V, LBK = 0 V		20		50	kΩ
		Sleep	$D = V_{CC}$, $R_S = 0 V or V_{CC}$			0.05	2	
	Cupply ourront	Standby	$R_S = V_{CC}$, $D = V_{CC}$, LBK =	0 V		200	600	μΑ
I _{CC}	Supply current	pply current Dominant	$D = 0 \text{ V}$, No load, $R_S = 0 \text{ V}$, LBK = 0 V			6	A
		Recessive	$D = V_{CC}$, No load, $R_S = 0 V$	/, LBK = 0 V			6	mA

All typical values are at 25°C and with a 3.3 V supply. Characterized but not production tested.



RECEIVER SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN TYP ⁽¹⁾	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output		35	60	
t _{PHL}	Propagation delay time, high-to-low-level output		35	60	
t _{sk(p)}	Pulse skew (t _{PHL} - t _{PLH})	See Figure 6	7		ns
t _r	Output signal rise time		2	6.5	
t _f	Output signal fall time		2	6.5	

⁽¹⁾ All typical values are at 25°C and with a 3.3 V supply. Timing parameters are characterized but not production tested.

DEVICE SWITCHING CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN TYP(1)	MAX	UNIT	
t _(LBK)	Loopback delay, driver input to receiver output	HVD233	See Figure 11	7.5	13	ns
		R _S = 0 V, See Figure 10	70	135		
t _(loop1)	Total loop delay, driver input to receiver output, recessive to dominant	R_S with 10 k Ω to ground, See Figure 10	105	190	ns	
	recessive to definition.		R_S with 100 k Ω to ground, See Figure 10	535	1000	
			R _S = 0 V, See Figure 10	70	135	
t _(loop2)	Total loop delay, driver input to r dominant to recessive	eceiver output,	R_S with 10 k Ω to ground, See Figure 10	105	190	ns
	dominant to recessive		R_S with 100 k Ω to ground, See Figure 10	535	1100	

 $^{(1) \}quad \text{All typical values are at } 25^{\circ}\text{C and with a } 3.3 \text{ V supply. Timing parameters are characterized but not production tested.}$



PARAMETER MEASUREMENT INFORMATION

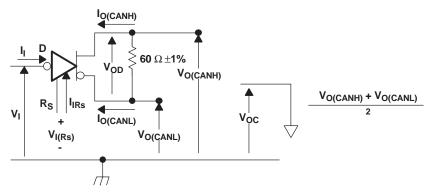


Figure 1. Driver Voltage, Current, and Test Definition

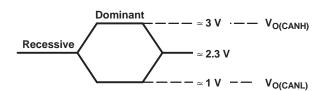


Figure 2. Bus Logic State Voltage Definitions

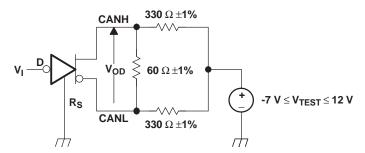
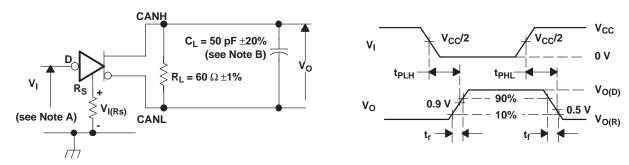


Figure 3. Driver V_{OD}



- A. The input pulse is supplied by a generator having the following characteristics: Pulse repetition rate (PRR) \leq 125 kHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_O =$ 50 Ω .
- B. C_L includes fixture and instrumentation capacitance.

Figure 4. Driver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

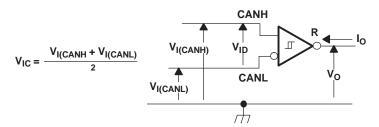
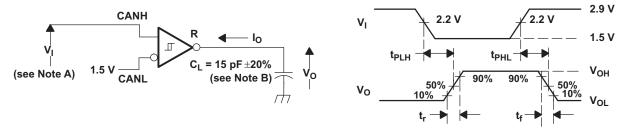


Figure 5. Receiver Voltage and Current Definitions

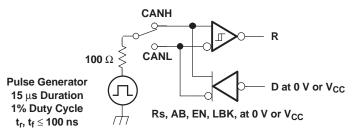


- A. The input pulse is supplied by a generator having the following characteristics: Pulse repetition rate (PRR) \leq 125 kHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_O =$ 50 Ω .
- B. C_L includes fixture and instrumentation capacitance.

Figure 6. Receiver Test Circuit and Voltage Waveforms

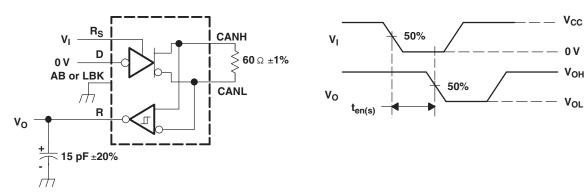
INPUT OUTPUT **MEASURED V_{CANH}** R VCANL $|V_{ID}|$ -6.1 V -7 V L 900 mV 12 V 11.1 V L 900 mV V_{OL} -1 V -7 V L 6 V 12 V 6 V L 6 V -6.5 V -7 V Н 500 mV 12 V 11.5 V Н 500 mV -7 V -1 V Н 6 V V_{OH} 6 V 12 V Н 6 V Open Open Н Χ

Table 1. Differential Input Voltage Threshold Test



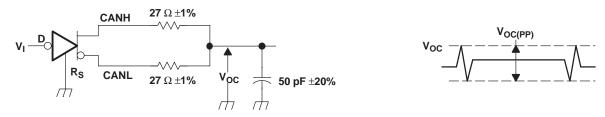
NOTE: This test is conducted to test survivability only. Data stability at the R output is not specified.

Figure 7. Test Circuit, Transient Over Voltage Test



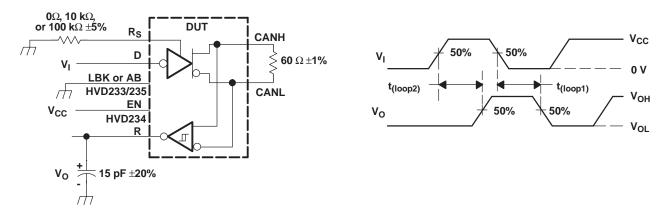
NOTE: All V_1 input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 6$ ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 8. t_{en(s)} Test Circuit and Voltage Waveforms



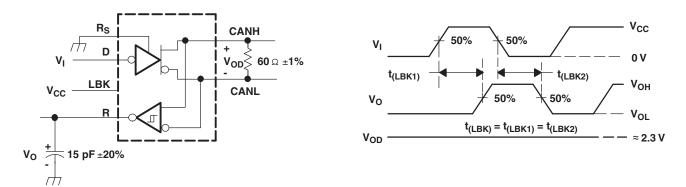
NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 6$ ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 9. V_{OC(pp)} Test Circuit and Voltage Waveforms



NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 6$ ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 10. t_(loop) Test Circuit and Voltage Waveforms



NOTE: All V_I input pulses are supplied by agenerator having the following characteristics: t_r or $t_f \le 6$ ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 11. t_(LBK) Test Circuit and Voltage Waveforms

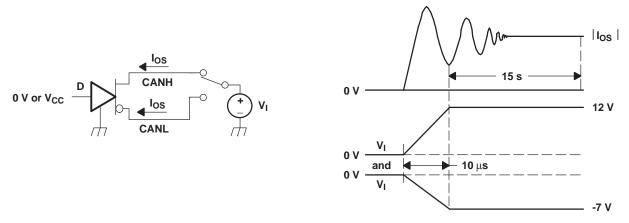
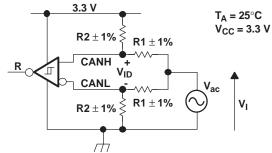


Figure 12. I_{OS} Test Circuit and Waveforms



The R Output State Does Not Change During Application of the Input Waveform.

V_{ID}	R1	R2
500 mV	50 Ω	280 Ω
900 mV	50 Ω	130 Ω

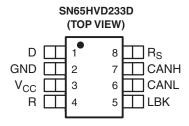


NOTE: All input pulses are supplied by a generator with f \leq 1.5 MHz.

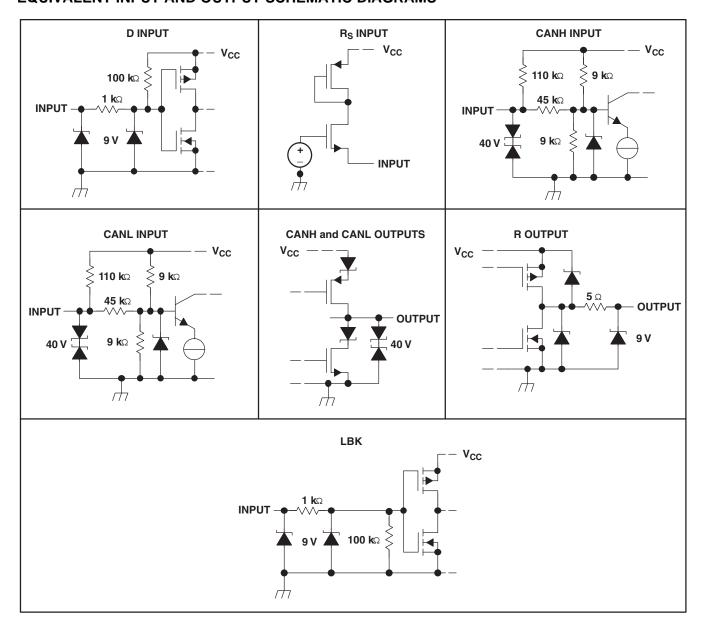
Figure 13. Common-Mode Voltage Rejection



DEVICE INFORMATION



EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



TEXAS INSTRUMENTS

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Table 2. Thermal Characteristics

	PARAMETERS	TEST CONDITIONS	VALUE	UNIT
0	Junction-to-ambient thermal resistance ⁽¹⁾	Low-K ⁽²⁾ board, no air flow	185	°C/W
θ_{JA}	Junction-to-ambient thermal resistance	High-K ⁽³⁾ board, no air flow	101	C/VV
θ_{JB}	Junction-to-board thermal resistance	High-K ⁽³⁾ board, no air flow	82.8	°C/W
θ_{JC}	Junction-to-case thermal resistance		26.5	°C/W
P _(AVG)	Average power dissipation	R_L = 60 Ω, R_S at 0 V, input to D a 1-MHz 50% duty cycle square wave V_{CC} at 3.3 V, T_A = 25°C	36.4	mW
T _(SD)	Thermal shutdown junction temperature		170	°C

- (1) See TI literature number SZZA003 for an explanation of this parameter.
- (2) JESD51-3 low effective thermal conductivity test board for leaded surface mount packages.
- (3) JESD51-7 high effective thermal conductivity test board for leaded surface mount packages.

FUNCTION TABLES

DRIVER ⁽¹⁾						
	INPUTS		OUTPUTS			
D	LBK/AB	R _s	CANH	CANL	BUS STATE	
Х	X	> 0.75 V _{CC}	Z	Z	Recessive	
L	L or open	< 0.22 \/	Н	L	Dominant	
H or open	X	≤ 0.33 V _{CC}	Z	Z	Recessive	
Х	Н	≤ 0.33 V _{CC}	Z	Z	Recessive	

(1) H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

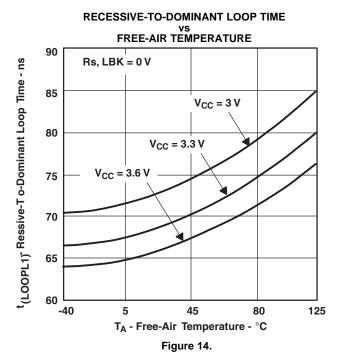
RECEIVER ⁽¹⁾						
	OUTPUT					
BUS STATE	$V_{ID} = V_{(CANH)} - V_{(CANL)}$	LBK	D	R		
Dominant	V _{ID} ≥ 0.9 V	L or open	X	L		
Recessive	V _{ID} ≤ 0.5 V or open	L or open	H or open	Н		
?	$0.5 \text{ V} < \text{V}_{\text{ID}} < 0.9 \text{ V}$	L or open	H or open	?		
X	X	Н	L	L		
X	Х	П	Н	Н		

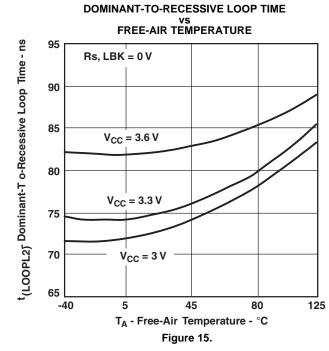
(1) H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

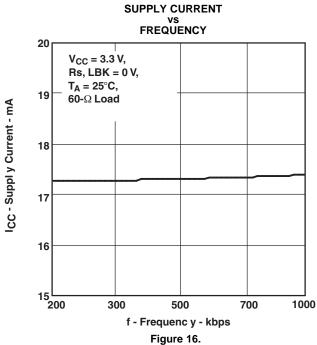
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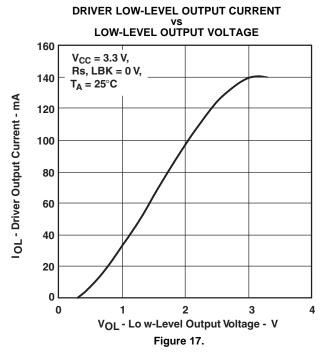


TYPICAL CHARACTERISTICS









0.12

0 0

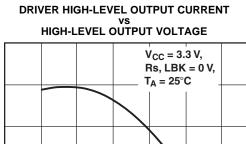
0.5



TYPICAL CHARACTERISTICS (continued)

3.5

tpHL- Receiver High-To-Low Propagation Delay - ns



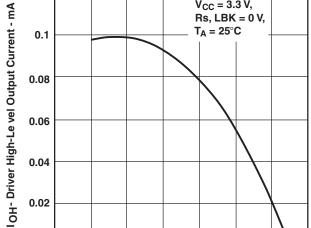
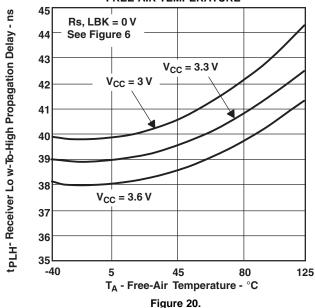


Figure 18.

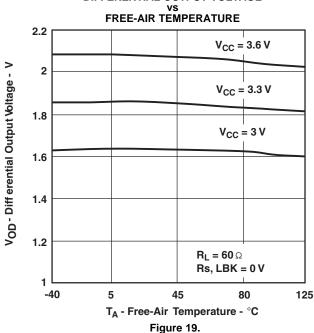
VOH- High-Le vel Output Voltage - V

RECEIVER LOW-TO-HIGH PROPAGATION DELAY vs FREE-AIR TEMPERATURE

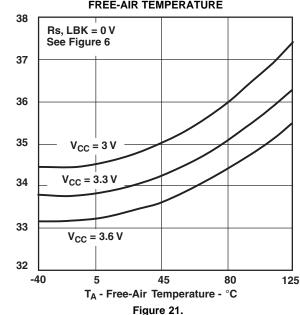
1.5



DIFFERENTIAL OUTPUT VOLTAGE



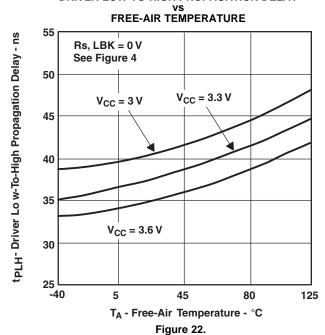
RECEIVER HIGH-TO-LOW PROPAGATION DELAY vs FREE-AIR TEMPERATURE





TYPICAL CHARACTERISTICS (continued)

DRIVER LOW-TO-HIGH PROPAGATION DELAY



DRIVER HIGH-TO-LOW PROPAGATION DELAY

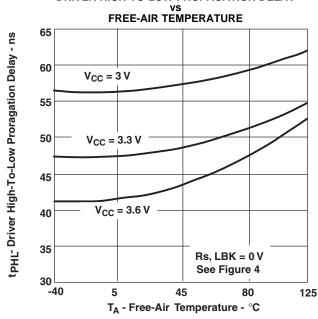
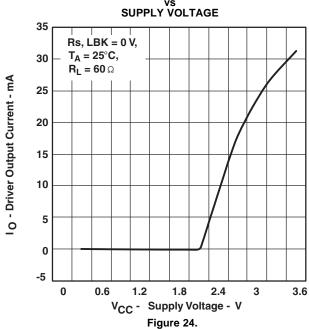


Figure 23.

DRIVER OUTPUT CURRENT





APPLICATION INFORMATION

DIAGNOSTIC LOOPBACK (SN65HVD233)

The loopback function of the SN65HVD233 is enabled with a high-level input to LBK. This forces the driver into a recessive state and redirects the data (D) input at pin 1 to the received-data output (R) at pin 4. This allows the host controller to input and read back a bit sequence to perform diagnostic routines without disturbing the CAN bus. A typical CAN bus application is displayed in Figure 25.

If the LBK pin is not used it may be tied to ground (GND). However, it is pulled low internally (defaults to a low-level input) and may be left open if not in use.

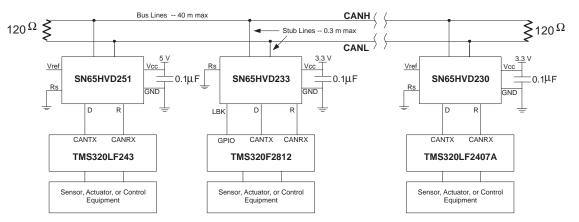


Figure 25. Typical HVD233 Application

ISO 11898 COMPLIANCE OF SN65HVD230 FAMILY OF 3.3-V CAN TRANSCEIVERS

Introduction

Many users value the low power consumption of operating their CAN transceivers from a 3.3 V supply. However, some are concerned about the interoperability with 5-V supplied transceivers on the same bus. This report analyzes this situation to address those concerns.

Differential Signal

CAN is a differential bus where complementary signals are sent over two wires and the voltage difference between the two wires defines the logical state of the bus. The differential CAN receiver monitors this voltage difference and outputs the bus state with a single-ended output signal.

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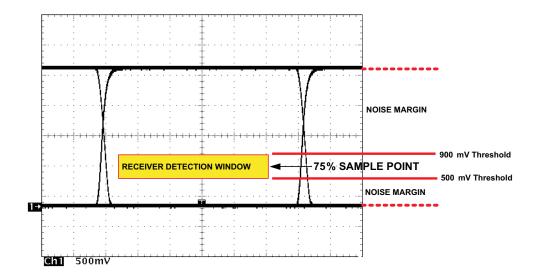


Figure 26. Typical SN65HVD230 Differential Output Voltage Waveform

The CAN driver creates the difference voltage between CANH and CANL in the dominant state. The dominant differential output of the SN65HVD230 is greater than 1.5 V and less than 3 V across a 60-ohm load. The minimum required by ISO 11898 is 1.5 V and maximum is 3 V. These are the same limiting values for 5-V supplied CAN transceivers. The bus termination resistors drive the recessive bus state and not the CAN driver.

A CAN receiver is required to output a recessive state with less than 500 mV and a dominant state with more than 900 mV difference voltage on its bus inputs. The CAN receiver must do this with common-mode input voltages from -2 V to 7 V. The SN65HVD230 family receivers meet these same input specifications as 5-V supplied receivers.

Common-Mode Signal

A common-mode signal is an average voltage of the two signal wires that the differential receiver rejects. The common-mode signal comes from the CAN driver, ground noise, and coupled bus noise. Obviously, the supply voltage of the CAN transceiver has nothing to do with noise. The SN65HVD230 family driver lowers the common-mode output in a dominant bit by a couple hundred millivolts from that of most 5-V drivers. While this does not fully comply with ISO 11898, this small variation in the driver common-mode output is rejected by differential receivers and does not effect data, signal noise margins or error rates.

Interoperability of 3.3-V CAN in 5-V CAN Systems

The 3.3-V supplied SN65HVD23x family of CAN transceivers are electrically interchangeable with 5-V CAN transceivers. The differential output is the same. The recessive common-mode output is the same. The dominant common-mode output voltage is a couple hundred millivolts lower than 5-V supplied drivers, while the receivers exhibit identical specifications as 5-V devices.

Electrical interoperability does not assure interchangeability however. Most implementers of CAN buses recognize that ISO 11898 does not sufficiently specify the electrical layer and that strict standard compliance alone does not ensure interchangeability. This comes only with thorough equipment testing.

BUS CABLE

The ISO-11898 Standard specifies a maximum bus length of 40 m and maximum stub length of 0.3 m with a maximum of 30 nodes. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A large number of nodes requires a transceiver with high input impedance such as the SN65HVD233.



The standard specifies the interconnect to be a single twisted-pair cable (shielded or unshielded) with $120-\Omega$ characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line terminate both ends of the cable to prevent signal reflections. Unterminated drop-lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections.

SLOPE CONTROL

The rise and fall slope of the SN65HVD233 driver output can be adjusted by connecting a resistor from R_s (pin 8) to ground (GND), or to a low-level input voltage as shown in Figure 27.

The slope of the driver output signal is proportional to the pin's output current. This slope control is implemented with an external resistor value of 10 k Ω to achieve a \approx 15 V/ μ s slew rate, and up to 100 k Ω to achieve a \approx 2.0 V/ μ s slew rate as displayed in Figure 28. Typical driver output waveforms with slope control are displayed in Figure 29.

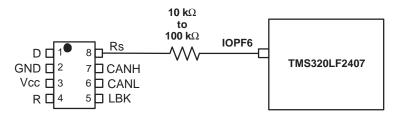


Figure 27. Slope Control/Standby Connection to a DSP

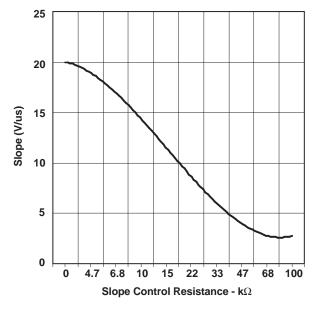


Figure 28. SN65HVD233 Driver Output Signal Slope vs Slope Control Resistance Value

20

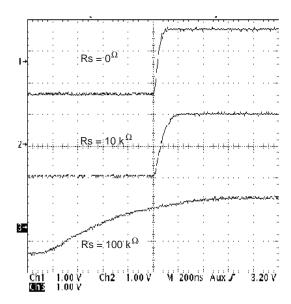


Figure 29. Typical SN65HVD233 250-kbps Output Pulse Waveforms With Slope Control

STANDBY

If a high-level input ($> 0.75 \ V_{CC}$) is applied to Rs (pin 8), the circuit enters a low-current, *listen only* standby mode during which the driver is switched off and the receiver remains active. The local controller can reverse this low-power standby mode when the rising edge of a dominant state (bus differential voltage $> 900 \ mV$ typical) occurs on the bus.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN65HVD233MDREP	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
V62/09611-01XE	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN65HVD233-EP:

Catalog: SN65HVD233

NOTE: Qualified Version Definitions:



23-Oct-2010

Catalog - TI's standard catalog product

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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