NXP (e)DP-to-LVDS bridge IC PTN3460

Support flexible display interfacing with DisplayPort to LVDS connectivity

This highly configurable, field-upgradable protocol converter gives computing OEMs and ODMs an efficient way to interface their (e)DP-capable CPUs and chipsets to a legacy LVDS display panel.

Key features

- Compliant to DP v1.1a and v1.2 standards
- Compliant to eDP v1.1 and v1.2 standards
- Supports DP Main Link operation with 1 or 2 lanes @ 1.62 or 2.7 Gbit/s
- Supports single- or dual-bus LVDS signaling
- Supports LVDS pixel clock frequency up to 112 MHz and color depths of 18 or 24 bits/pixel
- Firmware-controlled panel power-up/down sequencing timing parameters
- Supports 1920 x 1200, 60 Hz @ 24 bits/pixel
- Supports EDID structure v1.3 and on-chip EDID ROM emulation
- Brightness control without additional components
- HVQFN56 package (7 x 7 mm, 0.4 mm pitch)

Key benefits

- Significant BoM savings
  - EDID ROM emulation
  - No external timing reference
  - Brightness control support
- Non-volatile Flash memory supporting future upgradability
- Flexible configuration options (configuring through I^2C bus or DP AUX channel and hardware pins) support a wide choice of usage options and panel sizes
- Firmware and EDID Upgrade through Flash-over-AUX utility
- EDID Data Upgrade throughd Flash-over-DOS mode utility

Applications

- All-in-one PCs
- Notebook PCs
- Netbook and Nettop PCs

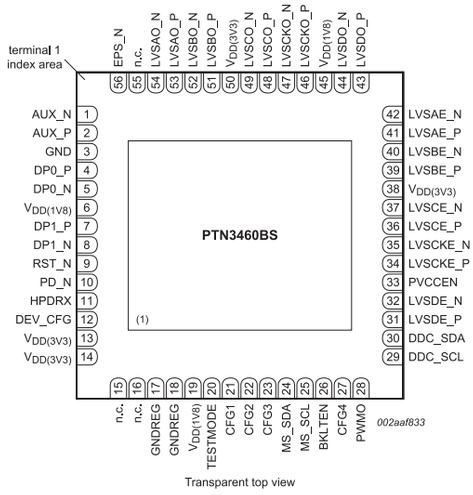
NXP's connectivity bridges enable seamless connectivity and protocol conversion between DisplayPort and legacy interfaces. As a DP-to-LVDS bridge, the PTN3460 supports DisplayPort and embedded DisplayPort, and is suitable for use with any computing platform, including all-in-one PCs and notebooks. The PTN3460 processes the incoming DP stream, performs protocol conversion, and then transmits the processed data stream in LVDS format. It has two high-speed ports: a Receive port facing the DP source (the CPU/GPU chipset), and a Transmit port facing the LVDS receiver (the LVDS controller).

The device receives the DP stream link at a rate of 1.62 or 2.7 Gbps, and supports one- or two-lane operation. It interacts with the DP source via DP Auxiliary (AUX) channel transactions for DP link training and set-up. It supports single- or dual-bus LVDS signaling with color depths of 18 or 24 bits per pixel, and at a pixel clock frequency of up to 112 MHz.

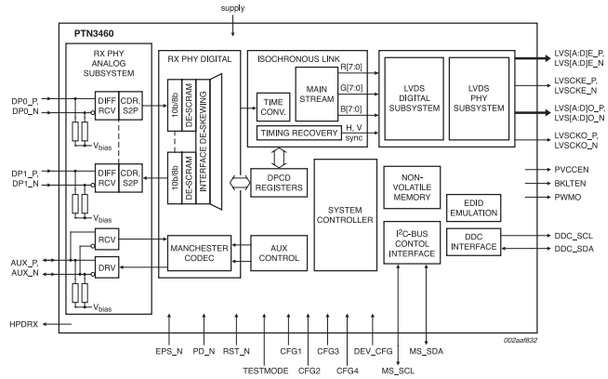
LVDS data packing can be done in VESA or JEIDA format. Also, the DP AUX interface transports I²C-over-AUX commands and supports EDID-DDC communications with the LVDS panel. To support panels without EDID ROM, the PTN3460 can emulate EDID ROM behavior and thus avoid specific changes in the system video BIOS. This also saves on the bill of materials.

Software packages support design-in at the customer factory. There is a Flash-over-AUX utility for upgrading product firmware and EDID data, and a Flash-over-DOS mode utility for updating the EDID data. Designers have access to an extensive set of documentation, including a datasheet, programmer's guide, and user manual, and can work with NXP's Global Application Support Team to address design-in issues.

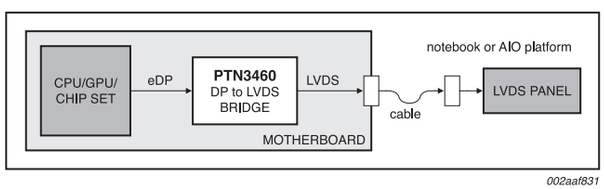
PTN3460 package pinouts



PTN3460 block diagram



PTN3460 application



PTN3460 Ordering information

Part Number	Package Name	Package Description	Package version
PTN3460BS	HVQFN56	Plastic thermal enhanced very thin quad flat package; no leads; 56 terminals; body 7 x 7 x 0.85 mm; 0.4 mm pitch. (Note: maximum package height is 1 mm)	SOT949-2

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