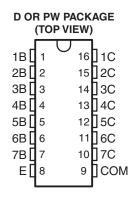


HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

Check for Samples: ULQ2003A-Q1, ULQ2004A-Q1

FEATURES

- **Qualified for Automotive Applications**
- **ESD Protection Exceeds 200 V Using Machine** Model (C = 200 pF, R = 0)
- 500-mA-Rated Collector Current (Single Output)
- High-Voltage Outputs: 50 V
- **Output Clamp Diodes**
- Inputs Compatible With Various Types of Logic
- **Relay-Driver Applications**



DESCRIPTION

The ULQ2003A and ULQ2004A are high-voltage high-current Darlington transistor arrays. Each consists of seven npn Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of a single Darlington pair is 500 mA. The Darlington pairs can be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers.

The ULQ2003A has a 2.7-kΩ series base resistor for each Darlington pair, for operation directly with TTL or 5-V CMOS devices. The ULQ2004A has a 10.5-kΩ series base resistor to allow operation directly from CMOS devices that use supply voltages of 6 V to 15 V. The required input current of the ULQ2004A is below that of the ULQ2003A.

ORDERING INFORMATION(1)

T _A	P	ACKAGE ⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
		Tube of 40	ULQ2003ATDQ1	LII 00000AT
	CO1C D	Reel of 2500	ULQ2003ATDRQ1	ULQ2003AT
-40°C to 105°C	SOIC – D	Tube of 40	ULQ2004ATDQ1	Product Preview
		Reel of 2500	ULQ2004ATDRQ1	ULQ2004AT
	TSSOP - PW	Reel of 2000	ULQ2003ATPWRQ1	U2003AT
-40°C to 125°C	SOIC - D	Reel of 2500	ULQ2003AQDRQ1	ULQ2003AQ

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

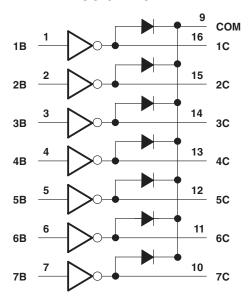


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

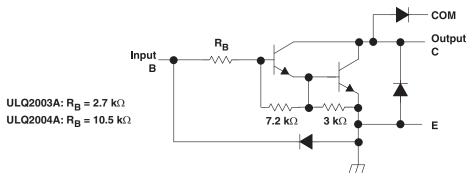
Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



LOGIC DIAGRAM



SCHEMATICS (EACH DARLINGTON PAIR)



- A. All resistor values shown are nominal.
- B. The collector-emitter diode is a parasitic structure and should not be used to conduct current. If the collector(s) go below ground an external Schottky diode should be added to clamp negative undershoots.



ABSOLUTE MAXIMUM RATINGS(1)

at 25°C free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Collector-emitter voltage			50	V
	Clamp diode reverse voltage ⁽²⁾			50	V
VI	Input voltage (2)			30	V
	Peak collector current	See Figure 14		500	mA
I _{OK}	Output clamp current			500	mA
	Total emitter-terminal current			-2.5	Α
P _D	Continuous total power dissipation		See Dissipa Ratings Ta		
_	Occupation for a sintension particle	ULQ200xAT	-40 105		00
T _A	Operating free-air temperature range	ULQ200xAQ	-40 125		°C
0	Dealers thereal in a dame (3) (4)	D package	73		9 0 /M
θ_{JA}	Package thermal impedance (3) (4)	PW package		108	°C/W
T _{stg}	Storage temperature range		-65	150	°C

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

PACKAGE	T _A = 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 85°C POWER RATING	T _A = 105°C POWER RATING	T _A = 125°C POWER RATING
D	950 mW	7.6 mW/°C	494 mW	342 mW	190 mW

All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.

Maximum power dissipation is a function of $T_J(max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

The package thermal impedance is calculated in accordance with JESD 51-7.



ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST	TEST CO	NDITIONS	UL	Q2003.	ΑT	UL	Q2003	ΑQ	UL	Q2004	AT	LINUT				
P	ARAWETER	FIGURE	IESI CO	NDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT				
				I _C = 125 mA									5					
				I _C = 200 mA			2.7			2.7			6					
V _{I(on)}	On-state input	Figure 6	V - 2 V	I _C = 250 mA			2.9			2.9				V				
	voltage	Figure 6	$V_{CE} = 2 V$	I _C = 275 mA									7	V				
				I _C = 300 mA			3			3								
				$I_{C} = 350 \text{ mA}$									8					
	Collector-emitter		$I_{I} = 250 \mu A$,	I _C = 100 mA		0.9	1.2		1	1.3		0.9	1.1					
V _{CE(sat)}		Figure 5	$I_1 = 350 \mu A$,	$I_C = 200 \text{ mA}$		1	1.4		1	1.5		1	1.3	V				
									$I_I = 500 \mu A$,	$I_C = 350 \text{ mA}$		1.2	1.7		1.2	1.8		1.2
	Collector cutoff current		V _{CE} = 50 V,	$T_A = 25^{\circ}C$			100			100			50					
Lamin			$I_1 = 0$	$T_A = 105$ °C			165							μА				
I _{CEX}			V _{CE} = 50 V	I ₁ = 0									100	μΑ				
		rigule 2	v CE = 20 v	V _I = 1 V									500					
V _F	Clamp forward voltage	Figure 8	I _F = 350 mA			1.7	2.2		1.7	2.2		1.7	2.1	V				
I _{I(off)}	Off-state input current	Figure 3	V _{CE} = 50 V,	I _C = 500 μA	30	65		30	65		50	65		μА				
			V _I = 3.85 V			0.93	1.35		0.93	1.35								
I	Input current	Figure 4	V _I = 5 V									0.35	0.5	mA				
			V _I = 12 V									1	1.45					
	Clamp reverse	Figure 7	V _R = 50 V	T _A = 25°C			100			100			50					
I _R	current	rigule /	v _R = 50 V				100			100			100	μA				
C _i	Input capacitance		V _I = 0,	f = 1 MHz		15	25		15	25		15	25	pF				

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	ULQ2003/	A, ULQ2	004A	UNIT
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNII
t _{PLH}	Propagation delay time, low- to high-level output	See Figure 9		1	10	μS
t_{PHL}	Propagation delay time, high- to low-level output	See Figure 9		1	10	μS
V _{OH}	High-level output voltage after switching	$V_S = 50 \text{ V}, I_O = 300 \text{ mA}, \text{ See Figure 10}$	V _S - 500			mV



PARAMETER MEASUREMENT INFORMATION

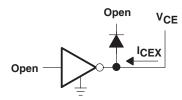


Figure 1. I_{CEX} Test Circuit

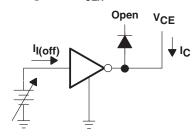


Figure 3. I_{I(off)} Test Circuit

C. I_I is fixed for measuring $V_{\text{CE(sat)}}$, variable for measuring h_{FE} .

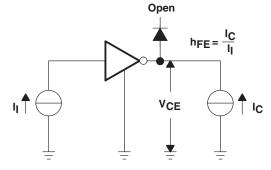


Figure 5. h_{FE} , $V_{CE(sat)}$ Test Circuit

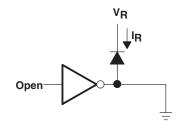


Figure 7. I_R Test Circuit

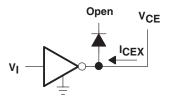


Figure 2. I_{CEX} Test Circuit

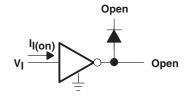


Figure 4. I_I Test Circuit

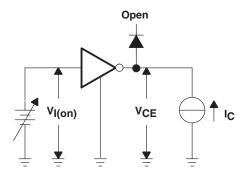


Figure 6. V_{I(on)} Test Circuit

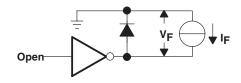
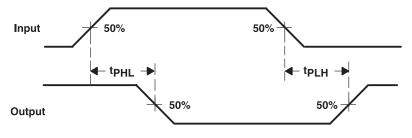


Figure 8. V_F Test Circuit

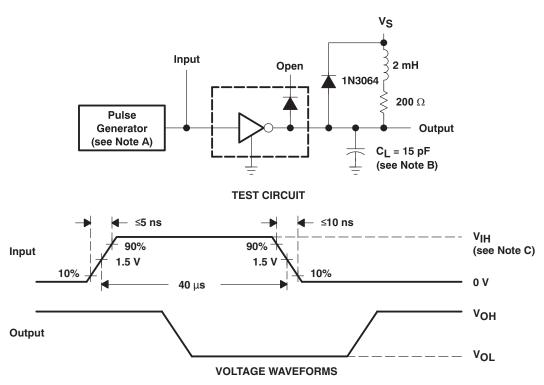


VOLTAGE WAVEFORMS

Figure 9. Propagation Delay-Time Waveforms



PARAMETER MEASUREMENT INFORMATION (continued)



- A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_0 = 50 Ω .
- B. C_L includes probe and jig capacitance.
- C. For testing the ULQ2003A, V_{IH} = 3 V; for the ULQ2004A, V_{IH} = 8 V.

Figure 10. Latch-Up Test Circuit and Voltage Waveforms



TYPICAL CHARACTERISTICS

COLLECTOR-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT (ONE DARLINGTON)

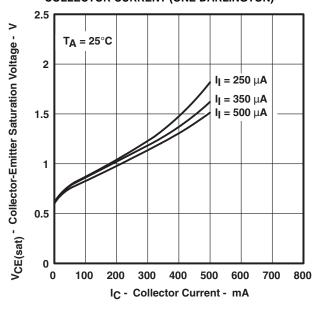


Figure 11.

COLLECTOR-EMITTER SATURATION VOLTAGE vs TOTAL COLLECTOR CURRENT (TWO DARLINGTONS IN PARALLEL)

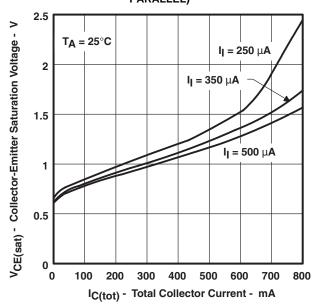


Figure 12.

COLLECTOR CURRENT vs

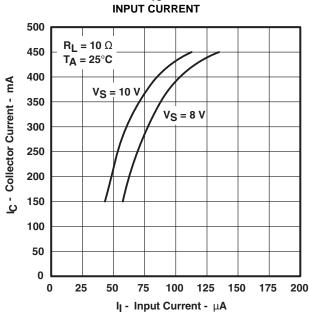


Figure 13.

D PACKAGE MAXIMUM COLLECTOR CURRENT VS

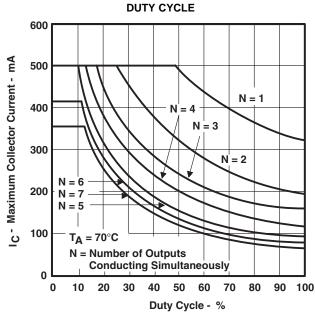


Figure 14.



APPLICATION INFORMATION

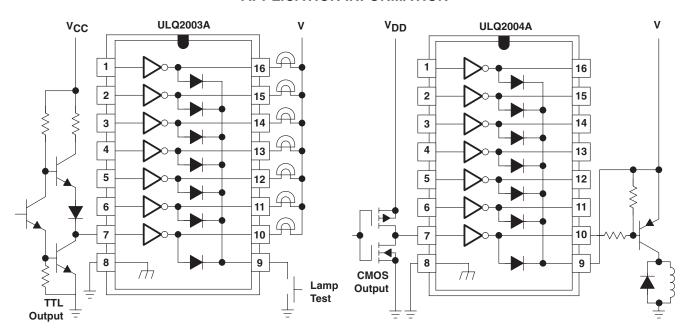


Figure 15. TTL to Load

Figure 16. Buffer for Higher Current Loads

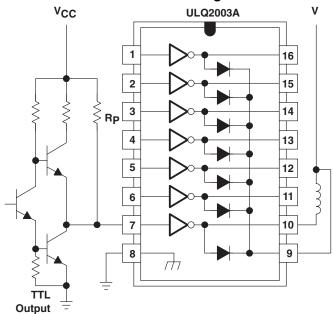


Figure 17. Use of Pullup Resistors to Increase Drive Current





31-Dec-2011

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
ULQ2003AQDRQ1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
ULQ2003ATDG4Q1	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
ULQ2003ATDQ1	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
ULQ2003ATDRG4Q1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
ULQ2003ATDRQ1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
ULQ2003ATPWRQ1	ACTIVE	TSSOP	PW	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
ULQ2004ATDRG4Q1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
ULQ2004ATDRQ1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



PACKAGE OPTION ADDENDUM

31-Dec-2011

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OTHER QUALIFIED VERSIONS OF ULQ2003A-Q1, ULQ2004A-Q1:

Catalog: ULQ2003A, ULQ2004A

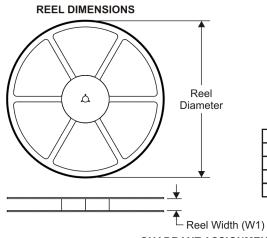
NOTE: Qualified Version Definitions:

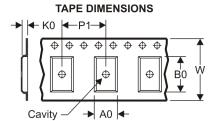
Catalog - TI's standard catalog product

PACKAGE MATERIALS INFORMATION

www.ti.com 30-Jul-2010

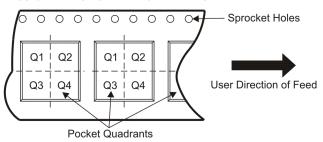
TAPE AND REEL INFORMATION





		Dimension designed to accommodate the component width
		Dimension designed to accommodate the component length
P	〈 0	Dimension designed to accommodate the component thickness
		Overall width of the carrier tape
П	P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ULQ2003ATPWRQ1	TSSOP	PW	16	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

www.ti.com 30-Jul-2010



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ULQ2003ATPWRQ1	TSSOP	PW	16	2500	346.0	346.0	29.0

D (R-PDS0-G16)

PLASTIC SMALL OUTLINE

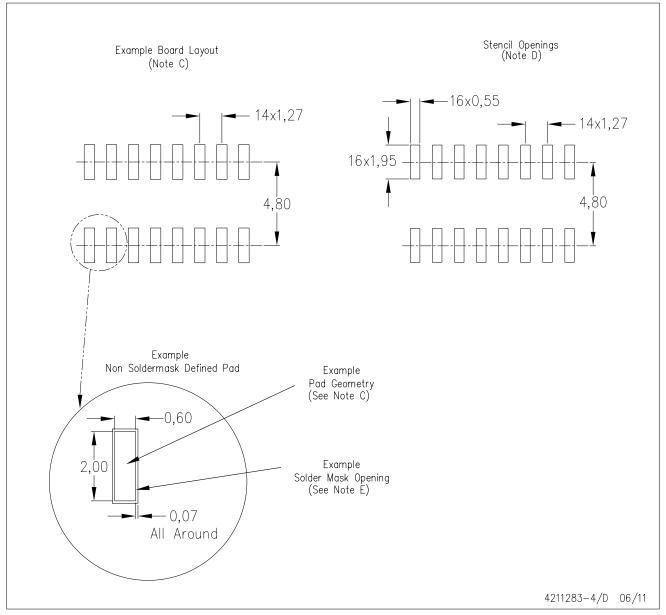


- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

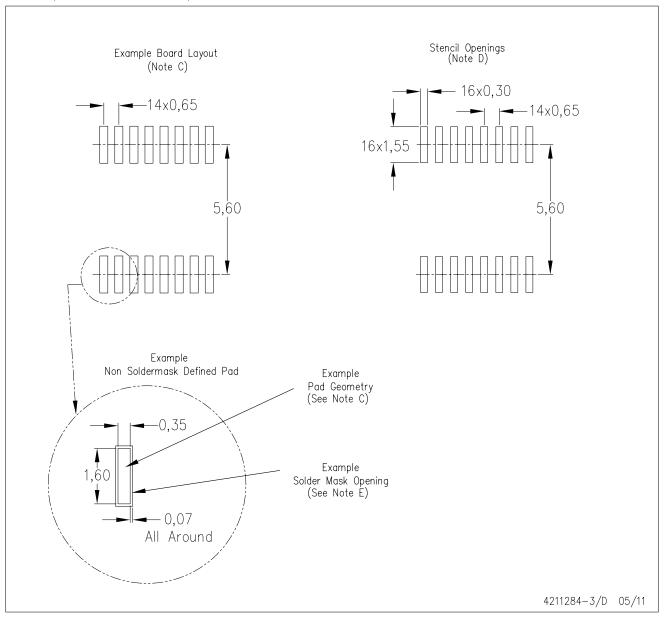


- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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