

#### FEATURES

- Low Supply Current...20 μA Typ
- Single Power Supply
- Rail-to-Rail Common-Mode Input Voltage Range
- Push-Pull Output Circuit
- Low Input-Bias Current

#### **APPLICATIONS**

- Battery Packs for Sensing Battery Voltage
- MP3 Players, Digital Cameras, PMPs
- Cellular Phones, PDAs, Notebook Computers
- Test Equipment
- General-Purpose Low-Voltage Applications

### **DESCRIPTION/ORDERING INFORMATION**

The TLV7256 is a CMOS-type general-purpose dual comparator capable of single power-supply operation and using lower supply currents than the conventional bipolar comparators. Its push-pull output can connect directly to local ICs such as TTL and CMOS circuits.

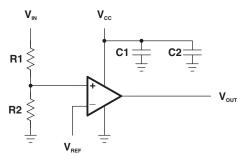
#### ORDERING INFORMATION<sup>(1)</sup>

T <sub>A</sub>	PACK	AGE <sup>(2)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
	SSOP – DCT	Reel of 3000	TLV7256IDCTR	PREVIEW	
–40°C to 85°C	550P - DC1	Reel of 250	TLV7256IDCTT	FREVIEW	
	VSSOP – DDU	Reel of 3000	TLV7256IDDUR	YAUA	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **Typical Application Circuit**



**Figure 1. Threshold Detector** 



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

5 2IN+

 $V_{cc-}$ 

 $\Pi_4$ 

## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage		1.5	7	V	
$V_{ID}$	Differential input voltage				V	
VI	Input voltage		V <sub>CC</sub> -	$V_{CC+}$	V	
I <sub>O</sub>	Output current			±35	mA	
0	Thermal registeres, justice to $embient(2)$	DCT package		220	°C/W	
OJA	JA Thermal resistance, juction to ambient <sup>(2)</sup>	DDU package		227	-0/00	
Р	Dower dissipation	DCT package		250	m)//	
PD	9 Power dissipation	DDU package		200	mW	
T <sub>A</sub>	Operating free-air temperature range		-40	85	°C	
T <sub>stg</sub>	Storage temperature range		-55	125	°C	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Package thermal impedance is calculated according to JESD 51-7.

#### **Recommended Operating Conditions**

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	1.8	5	V
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

## **Electrical Characteristics**

 $V_{CC+}$  = 5 V,  $V_{CC-}$  = GND,  $T_A$  = 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNIT
V			25°C		±2	±7	
V <sub>IO</sub>	Input offset voltage		-40°C to 85°C			±8	mV
I <sub>IO</sub>	Input offset current		25°C		2		pА
l <sub>l</sub>	Input bias current		25°C		4		pА
V <sub>CM</sub>	Common-mode input voltage		25°C	0		V <sub>CC</sub>	V
CMRR	Common mode rejection ratio	$\Delta V_{CM} = 5 V$	25°C	48	65		d٦
CINIKK	Common-mode rejection ratio	$0 \le V_{CM} \le 5 V$	–40°C to 85°C	48			dB
		Output = High, V <sub>IN</sub> = 5 V	25°C		37	51	
		Output = Low, $V_{IN} = 5 V$	25°C		40	60	μΑ
		Output = High, $V_{IN} = 5 V$	_40°C to 85°C			61	
	Supply surrent	Output = Low, $V_{IN} = 5 V$	-40 C 10 65 C			70	
I <sub>CC</sub>	Supply current	Output = High, $V_{IN}$ = 2.5 V	25°C		20	32	
		Output = Low, $V_{IN}$ = 2.5 V	25°C		26	42	
		Output = High, $V_{IN}$ = 2.5 V	–40°C to 85°C			40	
		Output = Low, $V_{IN}$ = 2.5 V	-40°C 10 85°C			53	
A <sub>VD</sub>	Voltage gain	$V_D = 3 V, 1 V \le V_{OUT} \le 4 V$	25°C		88		dB
	Sink current	V 05V	25°C	25	33		
Isink	Sink current	V <sub>OL</sub> = 0.5 V	–40°C to 85°C	20			mA
	Source current		25°C	30	35		mA
source	Source current	V <sub>OH</sub> = 4.5 V	–40°C to 85°C	25			ШA
		1 – 5 mA	25°C		0.07	0.12	v
V <sub>OL</sub>	Low-level output voltage	$I_{sink} = 5 \text{ mA}$	-40°C to 85°C			0.20	V
v		1 5 m A	25°C	4.9	4.93		V
V <sub>OH</sub>	High-level output voltage	I <sub>source</sub> = 5 mA	-40°C to 85°C	4.85			V

# TLV7256 **DUAL COMPARATOR**

SLCS147A-OCTOBER 2006-REVISED JANUARY 2007



#### **Electrical Characteristics**

 $V_{CC+}$  = 2.7 V,  $V_{CC-}$  = GND,  $T_{A}$  = 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNI
			25°C		±2	±8	
V <sub>IO</sub>	Input offset voltage		–40°C to 85°C			±9	mV
I <sub>IO</sub>	Input offset current		25°C		2		pА
l <sub>l</sub>	Input bias current		25°C		4		pА
V <sub>CM</sub>	Common-mode input voltage		25°C	0		$V_{CC}$	V
	Common mode sole stice setie	$\Delta V_{CM} = 2.7 V$	25°C	42	57		dB
CMRR	Common-mode rejection ratio	$0 \le V_{CM} \le 2.7 \text{ V}$	–40°C to 85°C	42			
		Output = High, $V_{IN}$ = 2.7 V	2500		30	55	
		Output = Low, $V_{IN}$ = 2.7 V	25°C		36	55	μΑ
		Output = High, $V_{IN}$ = 2.7 V	–40°C to 85°C			65	
сс	Current automat	Output = Low, $V_{IN}$ = 2.7 V	-40°C 10 85°C			65	
	Supply current	Output = High, V <sub>IN</sub> = 1.35 V	2500		30	48	
		Output = Low, $V_{IN}$ = 1.35 V	25°C		35	55	
		Output = High, V <sub>IN</sub> = 1.35 V	40%C to 95%C			55	
		Output = Low, $V_{IN}$ = 1.35 V	–40°C to 85°C			65	
A <sub>VD</sub>	Voltage gain	$V_D = 1.7 \text{ V},  0.5 \text{ V} \leq V_{OUT} \leq 2.2 \text{ V}$	25°C		88		dB
	Ciale aumont		25°C	13	18		
sink	Sink current	V <sub>OL</sub> = 0.5 V	–40°C to 85°C	11			mA
	Source ourrest	N 22N	25°C	15	20		~ ^
source	Source current	V <sub>OH</sub> = 2.2 V	–40°C to 85°C	13			mA
			25°C		0.11	0.16	V
/ <sub>OL</sub>	Low-level output voltage	$I_{sink} = 5 \text{ mA}$	–40°C to 85°C			0.19	v
,		L 5 m/	25°C	2.54	2.60		V
V <sub>ОН</sub>	High-level output voltage	I <sub>source</sub> = 5 mA	–40°C to 85°C	2.45			v

## **Electrical Characteristics**

 $V_{CC+}$  = 1.8 V,  $V_{CC-}$  = GND,  $T_{A}$  = 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNIT	
V	Input offect voltage		25°C		±2	±8	mV	
V <sub>IO</sub>	Input offset voltage		–40°C to 85°C			±9	mv	
I <sub>IO</sub>	Input offset current		25°C		2		pА	
l <sub>l</sub>	Input bias current		25°C		4		pА	
V <sub>CM</sub>	Common-mode input voltage		25°C	0		$V_{CC} - 0.3$	V	
CMRR	Common mode rejection ratio	$\Delta V_{CM} = 5 V$	25°C	40	55		dB	
CINKK	Common-mode rejection ratio	$0 \le V_{CM} \le 5 V$	–40°C to 85°C	40			uБ	
		Output = High, $V_{IN}$ = 1.8 V	25°C		30	55		
		Output = Low, V <sub>IN</sub> = 1.8 V	25'0		33	47	μΑ	
		Output = High, V <sub>IN</sub> = 1.8 V	–40°C to 85°C			60		
сс	Current current	Output = Low, V <sub>IN</sub> = 1.8 V	-40°C 10 85°C			51		
	Supply current	Output = High, $V_{IN} = 0.9 V$	2500		20	32		
		Output = Low, $V_{IN} = 0.9 V$	25°C		25	37		
		Output = High, V <sub>IN</sub> = 0.9 V	4000 to 0500			34		
		Output = Low, $V_{IN} = 0.9 V$	–40°C to 85°C			40	l.	
A <sub>VD</sub>	Voltage gain	$V_{D}$ = 1.1 V, 0.4 V $\leq V_{OUT} \leq 1.5$ V	25°C		88		dB	
	Cink ourrent	V 0.5.V	25°C	6	9			
I <sub>sink</sub>	Sink current	V <sub>OL</sub> = 0.5 V	–40°C to 85°C	5			mA	
	Source current		25°C	5	9		mA	
source	Source current	V <sub>OH</sub> = 2.2 V	–40°C to 85°C	4			ШA	
\ <i>\</i>	Low lovel output voltoge		25°C		0.2	0.34	V	
V <sub>OL</sub>	Low-level output voltage	I <sub>sink</sub> = 5 mA	–40°C to 85°C			0.39	v	
	Lish lovel output veltage	L 5 mA	25°C	1.3	1.6		V	
V <sub>OH</sub>	High-level output voltage	I <sub>source</sub> = 5 mA	–40°C to 85°C	1.2			V	

# **TLV7256 DUAL COMPARATOR**

SLCS147A-OCTOBER 2006-REVISED JANUARY 2007



#### **Switching Characteristics**

 $V_{CC+}$  = 5 V,  $V_{CC-}$  = GND,  $T_A$  = 25°C (unless otherwise noted)

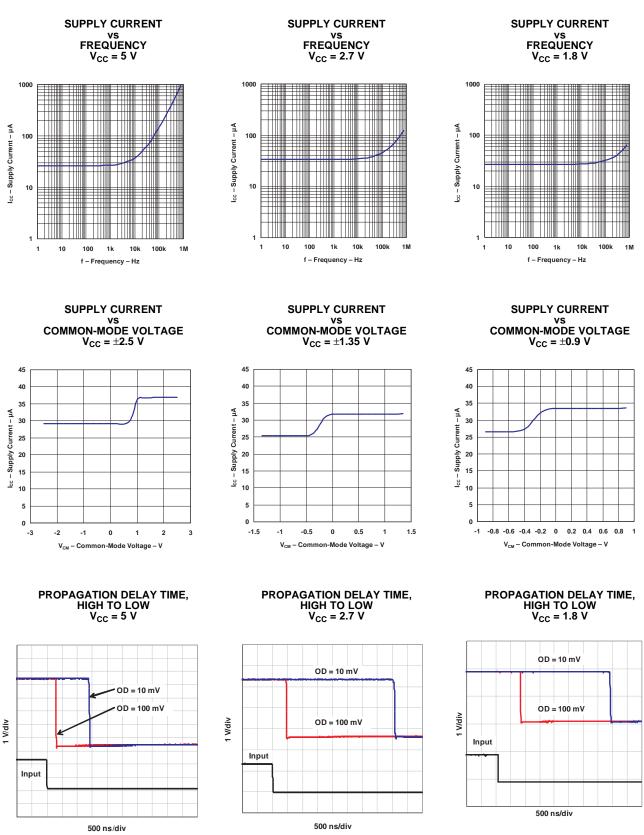
	PARAMETER	TEST CONDITIONS	TYP	UNIT
	Propagation dology time (turn on)	Overdrive = 100 mV	680	20
t <sub>PLH</sub>	Propagation delay time (turn on)	500	ns	
	Propagation dology time (turn off)	Overdrive = 100 mV	250	20
t <sub>PHL</sub>	Propagation delay time (turn off)	TTL step input	380	ns
t <sub>TLH</sub>	Pospono timo	Overdrive = 100 mV	60	ns
t <sub>THL</sub>	Response time		8	115

## **Switching Characteristics**

 $V_{CC+}$  = 3 V,  $V_{CC-}$  = GND,  $T_{A}$  = 25°C (unless otherwise noted)

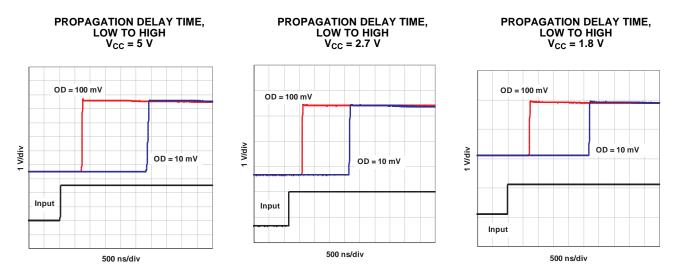
	PARAMETER	TEST CONDITIONS	TYP	UNIT
t <sub>PLH</sub>	Propagation delay time (turn on)	Overdrive = 100 mV	550	ns
t <sub>PHL</sub>	Propagation delay time (turn off)	Overdrive = 100 mV	250	ns
t <sub>TLH</sub>	Decements time		30	
t <sub>THL</sub>	Response time	Overdrive = 100 mV	8	ns

#### **TYPICAL CHARACTERISTICS**





#### **TYPICAL CHARACTERISTICS (continued)**



### PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins F	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TLV7256IDDUR	ACTIVE	VSSOP	DDU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV7256IDDURG4	ACTIVE	VSSOP	DDU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. **TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## PACKAGE MATERIALS INFORMATION

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### TAPE AND REEL INFORMATION

#### REEL DIMENSIONS

TEXAS INSTRUMENTS





TAPE AND REEL INFORMATION

#### TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV7256IDDUR	VSSOP	DDU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3

TEXAS INSTRUMENTS

www.ti.com

## PACKAGE MATERIALS INFORMATION

13-Jan-2012

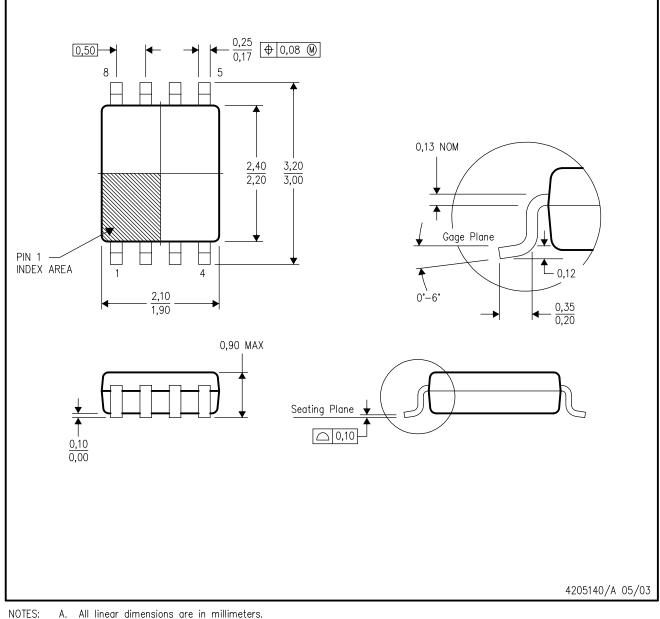


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV7256IDDUR	VSSOP	DDU	8	3000	202.0	201.0	28.0

DDU (R-PDSO-G8)

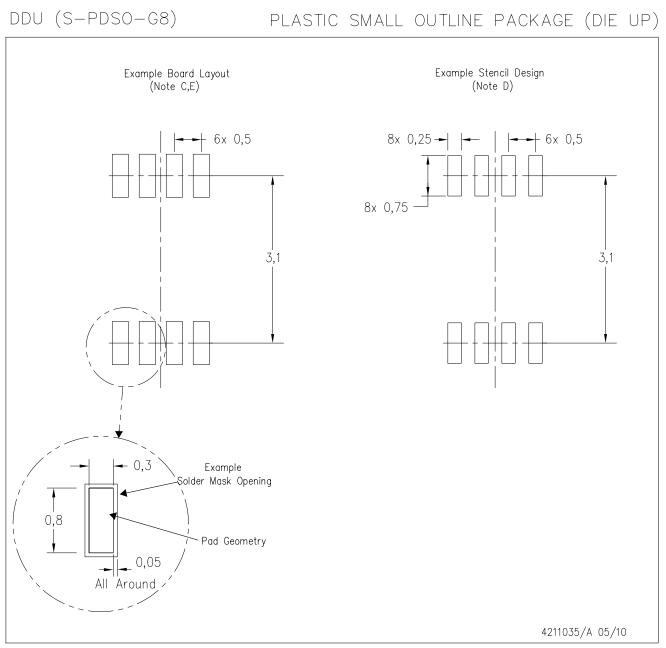
PLASTIC SMALL-OUTLINE PACKAGE



Α. All linear dimensions are in millimeters.

- Β. This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion. C.
- D. Falls within JEDEC MO-187 variation CA.





NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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