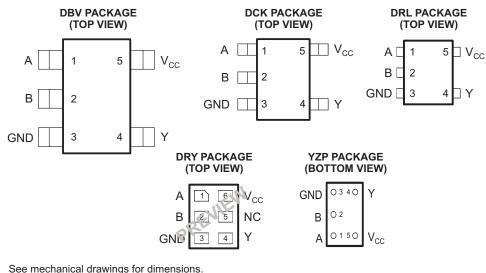


FEATURES

- Available in the Texas Instruments NanoFree™ Package
- Optimized for 1.8-V Operation and Is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- I_{off} Supports Partial-Power-Down Mode Operation
- Sub-1-V Operable
- Max t_{nd} of 2.4 ns at 1.8 V

- Low Power Consumption, 10-µA Max Icc
- ±8-mA Output Drive at 1.8 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



NC – No internal connection

DESCRIPTION/ORDERING INFORMATION

This single 2-input positive-AND gate is operational at 0.8-V to 2.7-V V_{CC}, but is designed specifically for 1.65-V to 1.95-V V_{CC} operation.

The SN74AUC1G08 performs the Boolean function $Y = A \bullet B$ or $Y = \overline{A + B}$ in positive logic.

T _A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽³⁾
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74AUC1G08YZPR	UE_
–40°C to 85°C	SON – DRY	Reel of 5000	SN74AUC1G08DRYR	PREVIEW
	SOT (SOT-23) – DBV	Reel of 3000	SN74AUC1G08DBVR	U08_
-	SOT (SC-70) – DCK	Reel of 3000	SN74AUC1G08DCKR	UE_

ORDERING INFORMATION

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

(3) DBV/DCK/DRY: The actual top-side marking has one additional character that designates the assembly/test site. YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN74AUC1G08 SINGLE 2-INPUT POSITIVE-AND GATE

SCES3740-SEPTEMBER 2001-REVISED APRIL 2007



DESCRIPTION/ORDERING INFORMATION (CONTINUED)

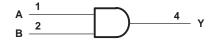
NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

FUNCTION TABLE

INP	UTS	OUTPUT
Α	В	Y
Н	Н	Н
L	Х	L
Х	L	L

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	3.6	V
VI	Input voltage range ⁽²⁾		-0.5	3.6	V
Vo	Voltage range applied to any output in the	high-impedance or power-off state ⁽²⁾	-0.5	3.6	V
Vo	Output voltage range ⁽²⁾		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V ₁ < 0		-50	mA
I _{OK}	Output clamp current	V ₀ < 0		-50	mA
I _O	Continuous output current			±20	mA
	Continuous current through V_{CC} or GND			±100	mA
		DBV package		206	
		DCK package		252	
θ_{JA}	Package thermal impedance ⁽³⁾	DRL package		142	°C/W
		DRY package		234	
		YZP package		132	
T _{stg}	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating" conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed. (2)

(3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT	
V _{CC}	Supply voltage		0.8	2.7	V	
V	High-level input voltage	$V_{CC} = 0.8 \text{ V to } 1.95 \text{ V}$	$0.65 imes V_{CC}$		V	
VIH	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		v	
V		V_{CC} = 0.8 V to 1.95 V		$0.35 \times V_{CC}$	V	
VIL	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	v	
VI	Input voltage		0	3.6	V	
Vo	Output voltage		0	V _{CC}	V	
		$V_{CC} = 0.8 V$		-0.7		
		$V_{CC} = 1.1 V$		-3		
I _{OH}	High-level output current	$V_{CC} = 1.4 V$		-5	mA	
	High-level output current	V _{CC} = 1.65 V				
		V _{CC} = 2.3 V		-9		
		V _{CC} = 0.8 V		0.7		
		$V_{CC} = 1.1 V$		3		
I _{OL}	Low-level output current	$V_{CC} = 1.4 V$		5	mA	
		V _{CC} = 1.65 V		8		
		$V_{CC} = 2.3 V$		9		
Δt/Δv	Input transition rise or fell rate	$V_{CC} = 0.8 \text{ V to } 1.95 \text{ V}$		20	201	
ΔVΔV	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		10	ns/V	
T _A	Operating free-air temperature		-40	85	°C	

 All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{cc}	MIN	TYP ⁽¹⁾	MAX	UNIT
	I _{OH} = -100 μA	0.8 V to 2.7 V	V _{CC} – 0.1			
	I _{OH} = -0.7 mA	0.8 V		0.55		
	$I_{OH} = -3 \text{ mA}$	1.1 V	0.8			V
V _{OH}	$I_{OH} = -5 \text{ mA}$	1.4 V	1			v
	$I_{OH} = -8 \text{ mA}$	1.65 V	1.2			
	$I_{OH} = -9 \text{ mA}$	2.3 V	1.8			
	I _{OL} = 100 μA	0.8 V to 2.7 V			0.2	
	I _{OL} = 0.7 mA	0.8 V		0.25		
M	I _{OL} = 3 mA	1.1 V			0.3	V
V _{OL}	I _{OL} = 5 mA	1.4 V			0.4	v
	I _{OL} = 8 mA	1.65 V			0.45	
	I _{OL} = 9 mA	2.3 V			0.6	
II A or B input	$V_{I} = V_{CC}$ or GND	0 to 2.7 V			±5	μA
l _{off}	$V_{I} \text{ or } V_{O} = 2.7 \text{ V}$	0			±10	μA
I _{CC}	$V_{I} = V_{CC} \text{ or } GND, \qquad I_{O} = 0$	0.8 V to 2.7 V			10	μA
CI	V _I = V _{CC} or GND	2.5 V		3		pF

(1) All typical values are at $T_A = 25^{\circ}C$.

SN74AUC1G08 SINGLE 2-INPUT POSITIVE-AND GATE

SCES374O-SEPTEMBER 2001-REVISED APRIL 2007

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 15 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)			/ _{CC} = 1.2 V ± 0.1 V		V_{CC} = 1.5 V ± 0.1 V		V _{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V \pm 0.2 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
t _{pd}	A or B	Y	4.7	0.9	3.3	0.6	2.3	0.4	1.1	1.7	0.2	1.6	ns

TEXAS

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Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ (unless otherwise noted) (see Figure 1)

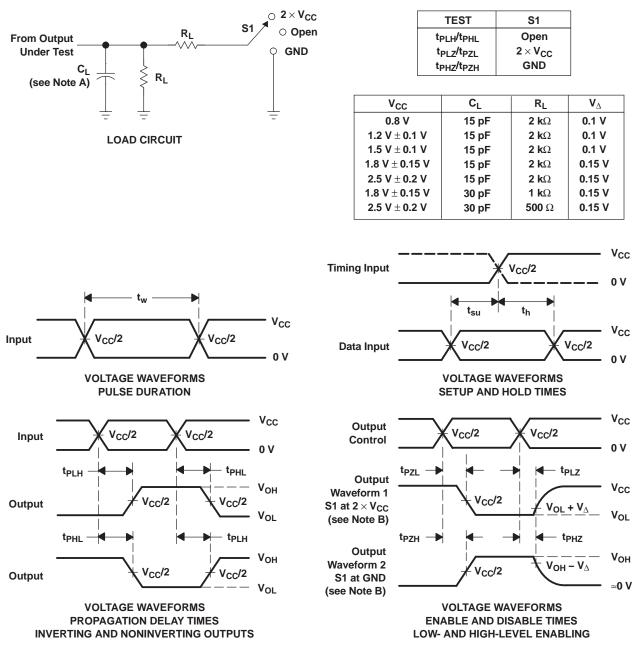
	FROM (INPUT)	TO (OUTPUT)	۷ _{cc}	,	V _{CC} = ± 0.2	UNIT		
	(INFOT)	(001201)	MIN	TYP	MAX	MIN	MAX	
t _{pd}	A or B	Y	0.7	1.3	2.4	0.5	2	ns

Operating Characteristics

 $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	V _{CC} = 0.8 V TYP	V _{CC} = 1.2 V TYP	V _{CC} = 1.5 V TYP	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	UNIT
C_{pd}	Power dissipation capacitance	f = 10 MHz	15	15	15	15	19	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , slew rate \geq 1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74AUC1G08DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC1G08DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC1G08DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC1G08DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC1G08DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC1G08DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC1G08DRLR	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC1G08DRLRG4	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC1G08YZPR	ACTIVE	DSBGA	YZP	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. **TBD:** The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TEXAS INSTRUMENTS





TAPE AND REEL INFORMATION

TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUC1G08DBVR	SOT-23	DBV	5	3000	180.0	9.2	3.17	3.23	1.37	4.0	8.0	Q3
SN74AUC1G08DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AUC1G08DCKR	SC70	DCK	5	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74AUC1G08DRLR	SOT	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74AUC1G08YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

25-Jan-2012



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUC1G08DBVR	SOT-23	DBV	5	3000	205.0	200.0	33.0
SN74AUC1G08DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AUC1G08DCKR	SC70	DCK	5	3000	205.0	200.0	33.0
SN74AUC1G08DRLR	SOT	DRL	5	4000	202.0	201.0	28.0
SN74AUC1G08YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.

D. Falls within JEDEC MO-178 Variation AA.



DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters.B. This drawing is subject to change without notice.

- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-203 variation AA.



LAND PATTERN DATA



NOTES:

- A. All linear dimensions are in millimeters.B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



DRL (R-PDSO-N5)

PLASTIC SMALL OUTLINE



NOTES:

All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994. Α. B. This drawing is subject to change without notice.

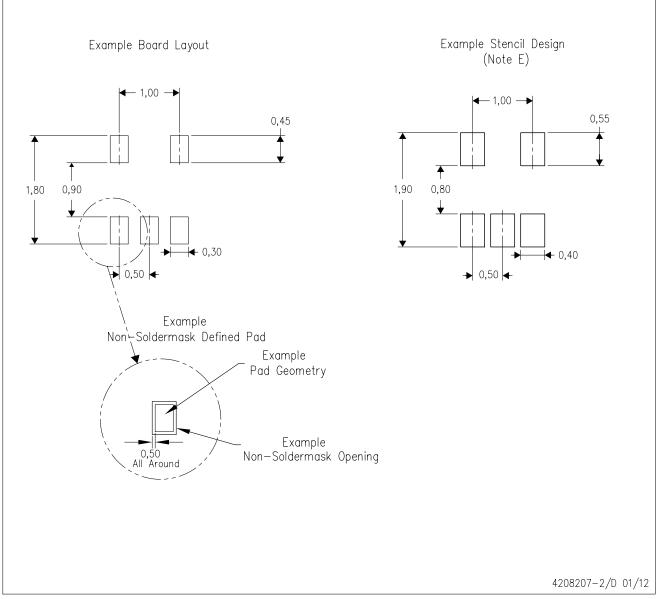
🖄 Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.





DRL (R-PDSO-N5)

PLASTIC SMALL OUTLINE



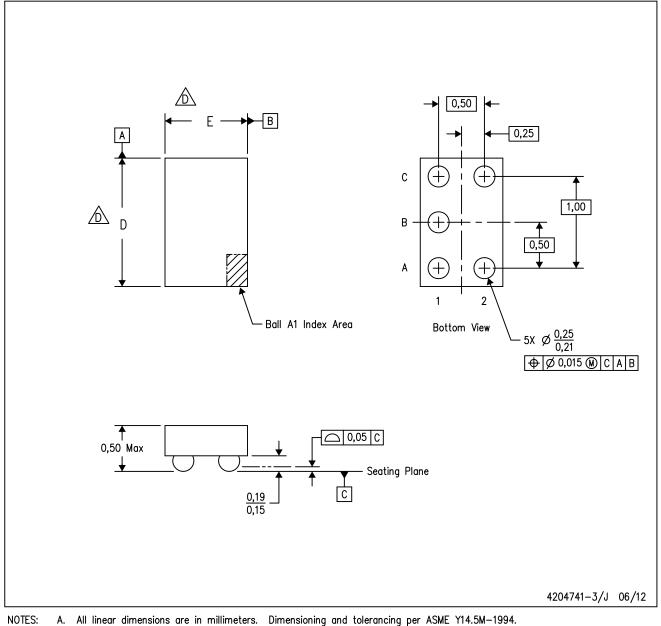
NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.



YZP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.
- The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
- E. This package is a Pb-free solder ball design. Refer to the 5 YEP package (drawing 4204725) for tin-lead (SnPb).

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