

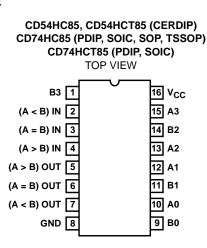
Data sheet acquired from Harris Semiconductor SCHS136E

August 1997 - Revised October 2003

Features

- Buffered Inputs and Outputs
- Typical Propagation Delay: 13ns (Data to Output at $V_{CC} = 5V, C_L = 15pF, T_A = 25^{\circ}C$
- · Serial or Parallel Expansion Without External Gating
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range ... -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at $V_{CC} = 5V$
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)
 - CMOS Input Compatibility, II \leq 1µA at V_{OL}, V_{OH}

Pinout



CD54HC85, CD74HC85, CD54HCT85, CD74HCT85

High-Speed CMOS Logic 4-Bit Magnitude Comparator

Description

The 'HC85 and 'HCT85 are high speed magnitude comparators that use silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

These 4-bit devices compare two binary, BCD, or other monotonic codes and present the three possible magnitude results at the outputs (A > B, A < B, and A = B). The 4-bit input words are weighted (A0 to A3 and B0 to B3), where A3 and B₃ are the most significant bits.

The devices are expandable without external gating, in both serial and parallel fashion. The upper part of the truth table indicates operation using a single device or devices in a serially expanded application. The parallel expansion scheme is described by the last three entries in the truth table.

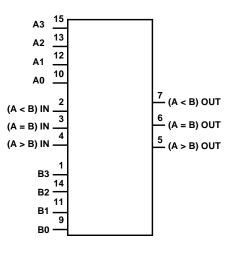
Ordering Information

PART NUMBER	TEMP. RANGE (^o C)	PACKAGE
CD54HC85F3A	-55 to 125	16 Ld CERDIP
CD54HCT85F3A	-55 to 125	16 Ld CERDIP
CD74HC85E	-55 to 125	16 Ld PDIP
CD74HC85M	-55 to 125	16 Ld SOIC
CD74HC85MT	-55 to 125	16 Ld SOIC
CD74HC85M96	-55 to 125	16 Ld SOIC
CD74HC85NSR	-55 to 125	16 Ld SOP
CD74HC85PW	-55 to 125	16 Ld TSSOP
CD74HC85PWR	-55 to 125	16 Ld TSSOP
CD74HC85PWT	-55 to 125	16 Ld TSSOP
CD74HCT85E	-55 to 125	16 Ld PDIP
CD74HCT85M	-55 to 125	16 Ld SOIC
CD74HCT85MT	-55 to 125	16 Ld SOIC
CD74HCT85M96	-55 to 125	16 Ld SOIC

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures. Copyright © 2003, Texas Instruments Incorporated

PFunctional Diagram



TRUTH TABLE

	COMPARIN	NG INPUTS		CAS	CADING IN	PUTS	OUTPUTS			
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B	
SINGLE DEVIC	E OR SERIES C	ASCADING								
A3 > B3	Х	Х	Х	x	х	х	н	L	L	
A3 < B3	Х	Х	Х	x	х	х	L	н	L	
A3 = B3	A2 >B2	Х	Х	x	х	х	н	L	L	
A3 = B3	A2 < B2	Х	Х	x	х	х	L	н	L	
A3 = B3	A2 = B2	A1 > B1	Х	x	х	х	н	L	L	
A3 = B3	A2 = B2	A1 < B1	Х	x	х	х	L	н	L	
A3 = B3	A2 = B2	A1 = B1	A0 > B0	x	х	х	н	L	L	
A3 = B3	A2 = B2	A1 = B1	A0 < B0	x	х	х	L	н	L	
A3 = B3	A2 = B2	A1 = B1	A0 = B0	н	L	L	н	L	L	
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	н	L	L	н	L	
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	н	L	L	н	
PARALLEL CA	SCADING		•		•	•			•	
A3 = B3	A2 = B2	A1 = B1	A0 = B0	x	х	н	L	L	н	
A3 = B3	A2 = B2	A1 = B1	A0 = B0	н	н	L	L	L	L	
A3 = B3	A2 = B2S	A1 = B1	A0 = B0	L	L	L	Н	н	L	

H = High Voltage Level, L = Low Voltage, Level, X = Don't Care

Absolute Maximum Ratings

DC Supply Voltage, V _{CC}
DC Input Diode Current, I _{IK}
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ ±20mA DC Output Diode Current, I_{OK}
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ ±20mA
DC Output Source or Sink Current per Output Pin, I_O
For $V_{O} > -0.5V$ or $V_{O} < V_{CC} + 0.5V$
DC V _{CC} or Ground Current, I _{CC or} I _{GND} ±50mA
Operating Conditions

Temperature Range (T _A)55°C to 125°C
Supply Voltage Range, V _{CC}
HC Types
HCT Types4.5V to 5.5V
DC Input or Output Voltage, V _I , V _O 0V to V _{CC}
Input Rise and Fall Time
2V
4.5V 500ns (Max)
6V

Thermal Information

Package Thermal Impedance, θ_{JA} (see Note 1):
E (PDIP) Package
M (SOIC) Package73 ^o C/W
NS (SOP) Package 64 ^o C/W
PW (TSSOP) Package 108 ^o C/W
Maximum Junction Temperature
Maximum Storage Temperature Range65°C to 150°C
Maximum Lead Temperature (Soldering 10s)
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

		TE: CONDI		v _{cc}		25 ⁰ C		-40 ^о С Т	O 85°C	-55 ⁰ C T	O 125 ⁰ C	
PARAMETER	SYMBOL	V _I (V)	I _O (mA)	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES	-	-			-		_	_		_		-
	VIH	-	-	2	1.5	-	-	1.5	-	1.5	-	V
Voltage				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input	VIL	-	-	2	-	-	0.5	-	0.5	-	0.5	V
Voltage				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output	ut V _{OH}	V _{IH} or V _{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
Voltage CMOS Loads			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
CIVIOS LUAUS			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output			-	-	-	-	-	-	-	-	-	V
Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
TTE LUaus			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output	V _{OL}	V _{IH} or V _{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
Voltage CMOS Loads			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
CIVIOS LUAUS			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	Ι	V _{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	Icc	V _{CC} or GND	0	6	-	-	8	-	80	-	160	μA

CD54HC85, CD74HC85, CD54HCT85, CD74HCT85

DC Electrical Specifications (Continued

		TEST CONDITIONS		V _{CC}	25 ⁰ C			-40°C TO 85°C		-55°C TO 125°C		
PARAMETER	SYMBOL	V _I (V)	I _O (mA)	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HCT TYPES		•										
High Level Input Voltage	VIH	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	VIL	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	lı	V _{CC} and GND	0	5.5	-		±0.1	-	±1	-	±1	μA
Quiescent Device Current	Icc	V _{CC} or GND	0	5.5	-	-	8	-	80	-	160	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	∆I _{CC} (Note 2)	V _{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

2. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS				
A0-A3, B0-B3 and (A = B) IN	1.5				
(A > B) IN, (A < B) IN	1				

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g. $360\mu A$ max at 25° C.

Switching Specifications Input t_{r} , $t_{f} = 6ns$

		TEST		25 ⁰ C			-40 ⁰ C TO 85 ⁰ C		-55 [°] C TO 125 [°] C		
PARAMETER	SYMBOL	CONDITIONS	V _{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES						-					
Propagation Delay,	t _{PLH} , t _{PHL}	$C_L = 50 pF$	2	-	-	195	-	245	-	295	ns
A _n , B _n to (A > B) OUT, (A < B) OUT			4.5	-	-	39	-	47	-	59	ns
		C _L = 15pF	5	-	16	-	-	-	-	-	ns
		$C_L = 50 pF$	6	-	-	33	-	42	-	50	ns
A_n , B_n to (A = B) OUT	^t PLH, ^t PHL	$C_L = 50 pF$	2	-	-	175	-	240	-	265	ns
			4.5	-	-	35	-	44	-	53	ns
		C _L = 15pF	5	-	14	-	-	-	-	-	ns
		$C_L = 50 pF$	6	-	-	30	-	37	-	45	ns

CD54HC85, CD74HC85, CD54HCT85, CD74HCT85

		TEST		25°C			-40°C TO 85°C		-55°C TO 125°C		
PARAMETER	SYMBOL	CONDITIONS	V _{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
(A > B) IN, $(A < B)$ IN, $(A = B)$ IN	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	140	-	175	-	210	ns
to $(A > B)$ OUT, $(A < B)$ OUT			4.5	-	-	28	-	35	-	42	ns
		C _L = 15pF	5	-	11	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	24	-	30	-	36	ns
(A > B) IN to $(A = B)$ OUT	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	120	-	150	-	180	ns
			4.5	-	-	24	-	30	-	36	ns
		C _L = 15pF	5	-	9	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	20	-	26	-	31	ns
Power Dissipation Capacitance (Notes 3, 4)	C _{PD}	-	5	-	24	-	-	-	-	-	pF
Output Transition Times (Figure 1)	t _{TLH} , t _{THL}	C _L = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C _{IN}	-	-	-	-	10	-	10	-	10	pF
HCT TYPES											
Propagation Delay,	t _{PLH} , t _{PHL}	C _L = 50pF	4.5	-	-	37	-	46	-	56	ns
An, Bn to $(A > B)$ OUT, (A < B) OUT		C _L = 15pF	5	-	15	-	-	-	-	-	ns
An, Bn to (A = B) OUT	t _{PLH} , t _{PHL}	$C_L = 50 pF$	4.5	-	-	40	-	50	-	60	ns
		C _L = 15pF	5	-	17	-	-	-	-	-	ns
(A > B) IN, (A < B) IN, (A = B) IN	t _{PLH} , t _{PHL}	$C_L = 50 pF$	4.5	-	-	30	-	38	-	45	ns
to $(A > B)$ OUT, $(A < B)$ OUT		C _L = 15pF	5	-	12	-	-	-	-	-	ns
(A > B) IN to $(A = B)$ OUT	t _{PLH} , t _{PHL}	$C_L = 50 pF$	4.5	-	-	31	-	39	-	47	ns
		C _L = 15pF	5	-	13	-	-	-	-	-	ns
Output Transition Times (Figure 1)	t _{TLH} , t _{THL}	C _L = 50pF	4.5	-	-	15	-	19	-	22	ns
Power Dissipation Capacitance (Notes 3, 4)	C _{PD}	-	5	-	26	-	-	-	-	-	pF
Input Capacitance	C _{IN}	_	-	-	-	10	-	10	-	10	pF

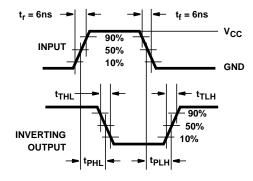
Switching Specifications Input t_r , $t_f = 6ns$ (Continued)

NOTES:

3. $C_{\mbox{PD}}$ is used to determine the dynamic power consumption, per gate/package.

4. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms





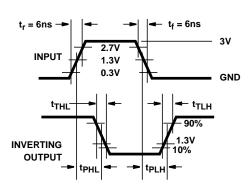
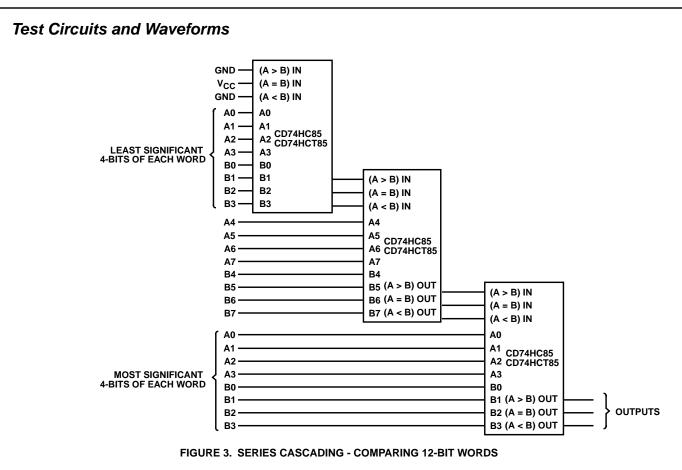
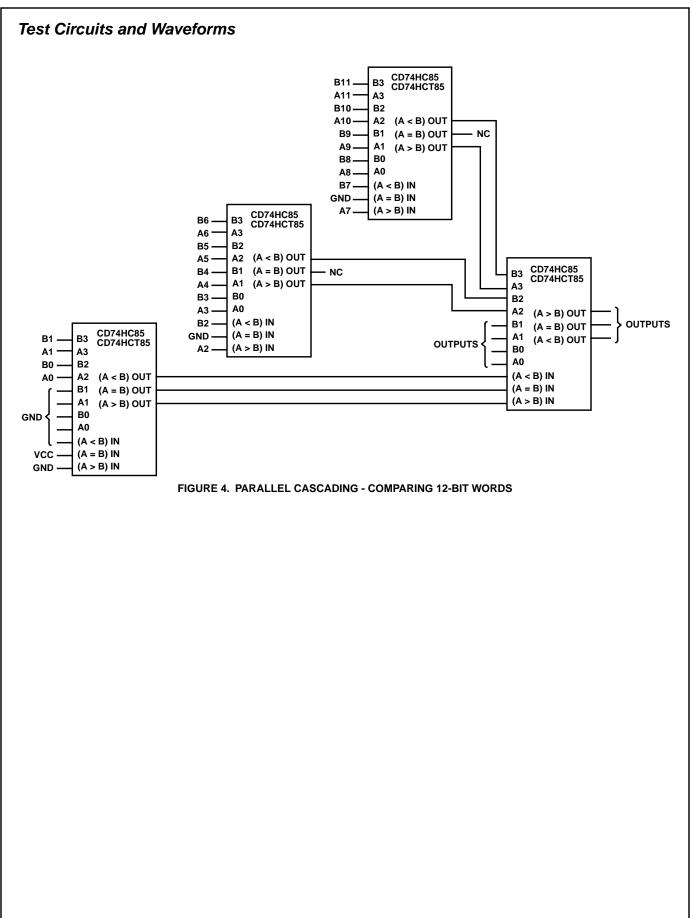


FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC







www.ti.com

5-Sep-2011

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-8867201EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Call TI	
8601301EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Call TI	
CD54HC85F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
CD54HCT85F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
CD74HC85E	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HC85EE4	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HC85M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC85M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC85M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC85M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC85ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC85MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC85MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC85MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC85MTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC85NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC85NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC85NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC85PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	



5-Sep-2011

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
CD74HC85PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC85PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC85PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC85PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC85PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC85PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC85PWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC85PWTG4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT85E	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HCT85EE4	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HCT85M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT85M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT85M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT85M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT85ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT85MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT85MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT85MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT85MTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	



www.ti.com

5-Sep-2011

(1) The marketing status values are defined as follows:
 ACTIVE: Product device recommended for new designs.
 LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
 NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
 PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
 OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54HC85, CD54HCT85, CD74HC85, CD74HCT85 :

• Catalog: CD74HC85, CD74HCT85

• Military: CD54HC85, CD54HCT85

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

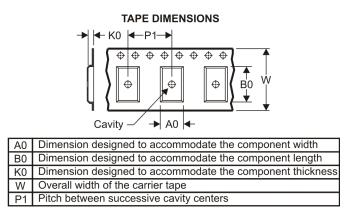
PACKAGE MATERIALS INFORMATION

www.ti.com

Texas Instruments

TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC85M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC85NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD74HC85PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC85PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HCT85M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TEXAS INSTRUMENTS

www.ti.com

PACKAGE MATERIALS INFORMATION

6-Aug-2010



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC85M96	SOIC	D	16	2500	333.2	345.9	28.6
CD74HC85NSR	SO	NS	16	2000	346.0	346.0	33.0
CD74HC85PWR	TSSOP	PW	16	2000	346.0	346.0	29.0
CD74HC85PWT	TSSOP	PW	16	250	346.0	346.0	29.0
CD74HCT85M96	SOIC	D	16	2500	333.2	345.9	28.6

J (R-GDIP-T**) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



4211283-4/D 06/11

D (R-PDSO-G16) PLASTIC SMALL OUTLINE Stencil Openings (Note D) Example Board Layout (Note C) -16x0,55 - 14x1,27 -14x1,27 16x1,95 4,80 4,80 Example Non Soldermask Defined Pad Example Pad Geometry (See Note C) 0,60 Example 2,00 Solder Mask Opening

(See Note E)

NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

← 0,07 All Around

- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994. β . This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153



LAND PATTERN DATA



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 \bigcirc Gage Plane ₽ 0,25 7 1 1,05 0,55 0°-10° Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS ** 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G**)

14-PINS SHOWN

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connctivity	www.ti.com/wirelessconnectivity		
		a O a Al a a m	

TI E2E Community Home Page

e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2011, Texas Instruments Incorporated