

# 100mA / 50V Digital transistors (with built-in resistors)

DTC144GE / DTC144GUA / DTC144GKA

● **Applications**

Inverter, Interface, Driver

● **Features**

- 1) The built-in bias resistors consist of thin-film resistors with complete isolation to allow negative biasing of the input, and parasitic effects are almost completely eliminated.
- 2) Only the on / off conditions need to be set for operation, making the device design easy.
- 3) Higher mounting densities can be achieved.

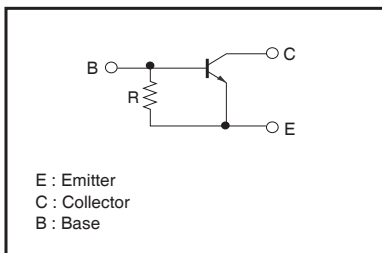
● **Structure**

NPN epitaxial planar silicon transistor (Resistor built-in type)

● **Packaging specifications**

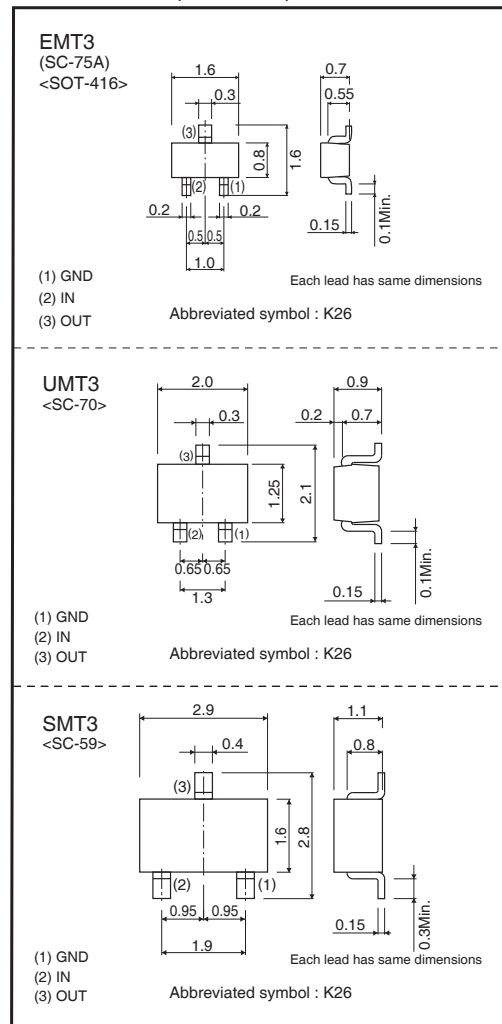
Part No.	Package	EMT3	UMT3	SMT3
	Packaging type	Taping	Taping	Taping
	Code	TL	T106	T146
	Basic ordering unit (pieces)	3000	3000	3000
DTC144GE		○	—	—
DTC144GUA		—	○	—
DTC144GKA		—	—	○

● **Inner circuit**



R=47kΩ

● **Dimensions (Unit : mm)**



● **Absolute maximum ratings (Ta=25°C)**

Parameter	Symbol	Limits	Unit
Collector-base voltage	V <sub>CB0</sub>	50	V
Collector-emitter voltage	V <sub>CE0</sub>	50	V
Emitter-base voltage	V <sub>EB0</sub>	5	V
Collector current	I <sub>c</sub>	100	mA
Collector power dissipation	P <sub>c</sub>	150	mW
		200	
Junction temperature	T <sub>j</sub>	150	°C
Storage temperature	T <sub>stg</sub>	-55 to +150	°C

● Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Collector-base breakdown voltage	$BV_{CBO}$	50	–	–	V	$I_C=50\mu A$
Collector-emitter breakdown voltage	$BV_{CEO}$	50	–	–	V	$I_C=1mA$
Emitter-base breakdown voltage	$BV_{EBO}$	5	–	–	V	$I_E=160\mu A$
Collector cutoff current	$I_{CBO}$	–	–	0.5	$\mu A$	$V_{CB}=50V$
Emitter cutoff current	$I_{EBO}$	65	–	130	$\mu A$	$V_{EB}=4V$
Collector-emitter saturation voltage	$V_{CE(sat)}$	–	–	0.3	V	$I_C=10mA, I_B=0.5mA$
DC current transfer ratio	$h_{FE}$	68	–	–	–	$I_C=5mA, V_{CE}=5V$
Emitter-base resistance	R	32.9	47	61.1	k $\Omega$	–
Transition frequency	$f_T$ *	–	250	–	MHz	$V_{CE}=10V, I_E=-5mA, f=100MHz$

\* Characteristics of built-in transistor

● Electrical characteristics curves

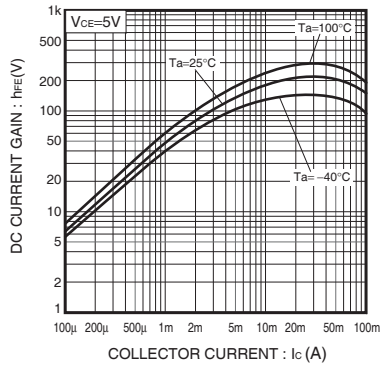


Fig.1 DC current gain vs. Collector current

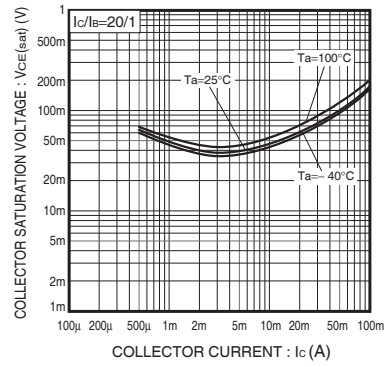


Fig.2 Collector-Emitter saturation vs. Collector current

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