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'90A, 'LS90 . . . Decade Counters

'92A, 'LS92 . . . Divide By-Twelve Counters

'93A, 'LS93 . . . 4-Bit Binary Counters

TV050	TYPICAL
TYPES	POWER DISSIPATION
'90A	145 mW
'92A, '93A	130 mW
'LS90, 'LS92, 'LS93	45 mW

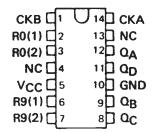
#### description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '90A and 'LS90, divide-by-six for the '92A and 'LS92, and the divide-by-eight for the '93A and 'LS93.

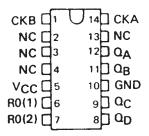
All of these counters have a gated zero reset and the '90A and 'LS90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four-bit binary) of these counters, the CKB input is connected to the  $\Omega_A$  output. The input count pulses are applied to CKA input and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '90A or 'LS90 counters by connecting the  $\Omega_D$  output to the CKA input and applying the input count to the CKB input which gives a divide-by-ten square wave at output  $\Omega_A$ .

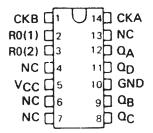
SN5490A, SN54LS90 . . . J OR W PACKAGE SN7490A . . . N PACKAGE SN74LS90 . . . D OR N PACKAGE (TOP VIEW)



SN5492A, SN54LS92...J OR W PACKAGE SN7492A...N PACKAGE SN74LS92...D OR N PACKAGE (TOP VIEW)

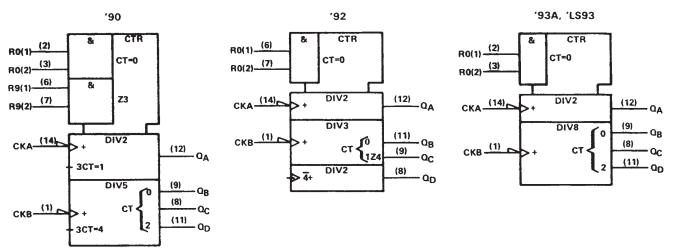


SN5493A, SN54LS93 . . . J OR W PACKAGE SN7493 . . . N PACKAGE SN74LS93 . . . D OR N PACKAGE (TOP VIEW)



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#### logic symbols†



<sup>&</sup>lt;sup>†</sup>These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.



'90A, 'LS90 BCD COUNT SEQUENCE

(See Note A)

COUNT	OUTPUT											
COOM	ap	$\alpha_{\text{C}}$	QΒ	QA								
0	L	L	L	L								
1	L	L	L	н								
2	L	L	Н	L								
3	Ĺ	L	Н	н								
4	L	Н	L	L								
5	L	Н	L	н								
6	L	Н	Н	L								
7	L	Н	Н	Н								
8	н	L	L	L								
9	Н	L	L	н								

'92A, 'LS92 COUNT SEQUENCE

(See Note C)

COUNT		OUT	PUT	
COON	$\sigma_{D}$	$\sigma_{C}$	$\sigma_{B}$	QA
0	L	L	L	L
1	L	L	L	н
2	L	L	Н	L
3	L	L	Н	Н
4	L	Н	L	L
5	L	Н	L	н
6	н	Ł	L	L
7	н	L	L	н
8	н	L	Н	L
9	н	L	Н	н
10	н	Н	L	L
11	н	Н	L	н

'92A, 'LS92, '93A, 'LS93 RESET/COUNT FUNCTION TABLE

RESET	INPUTS	OUTPUT									
R <sub>0(1)</sub>	R <sub>0(2)</sub>	a <sub>D</sub>	QA								
Н	Н	L	L	L	L						
L	X	COUNT									
X	L	COUNT									

NOTES: A. Output  $\Omega_{\mbox{\scriptsize A}}$  is connected to input CKB for BCD count.

- B. Output  $\mathbf{Q}_{D}$  is connected to input CKA for bi-quinary count.
- C. Output  $Q_A$  is connected to input CKB.
- D. H = high level, L = low level, X = irrelevant

'90A, 'LS90 BI-QUINARY (5-2)

(See Note B)

COUNT	OUTPUT										
COOM	QA	α <sub>D</sub>	ac	αB							
0	L	L	L	L							
1	L	L	L	Н							
2	L	L	Н	L							
3	L	L	Н	н							
4	L	Н	L	L							
5	н	L	L	L							
6	н	L	L	H							
7	н	L	Н	L							
8	н	L	Н	Н							
9	н	Н	L	L							

'90A, 'LS90 RESET/COUNT FUNCTION TABLE

1	RESET	INPUTS	3	OUTPUT							
R <sub>0(1)</sub>	R <sub>0(2)</sub>	R <sub>9(1)</sub>	R9(2)	$a_{D}$	QC	QB	QA				
Н	Н	L	Х	L	L	L	L				
Н	H	×	L	L	L	L	L				
X	×	н	н	н	Н						
X	L	×	L		СО	UNT					
L	×	L	Х	COUNT							
L	×	×	L	COUNT							
×	L	L	х	COUNT							

#### '93A, 'LS93 COUNT SEQUENCE

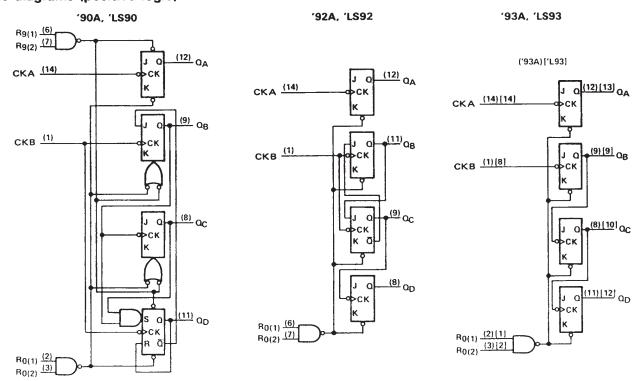
(See Note C)

(246 140f4 C)												
COUNT		ουτ	PUT									
COOK	QD	$\mathbf{a}_{\mathbf{C}}$	QB	QA								
0	L	L	L	L								
1	L	L	L	Н								
2	L	L	Н	L								
3	L	L	Н	Н								
4	L	Н	L	L								
5	L	Н	L	Н								
6	L	Н	Н	L								
7	L	Н	Н	Н								
8	н	L	L	L								
9	н	L	L	Н								
10	н	L	Н	L								
11	н	L	Н	Н								
12	н	Н	L	L								
13	н	н	L	Н								
14	н	Н	L									
15	н	Н	Н	Н								



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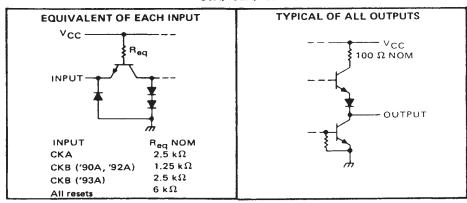
#### logic diagrams (positive logic)



The J and K inputs shown without connection are for reference only and are functionally at a high level. Pin numbers shown in () are for the 'LS93 and '93A and pin numbers shown in () are for the 54L93.

#### schematics of inputs and outputs

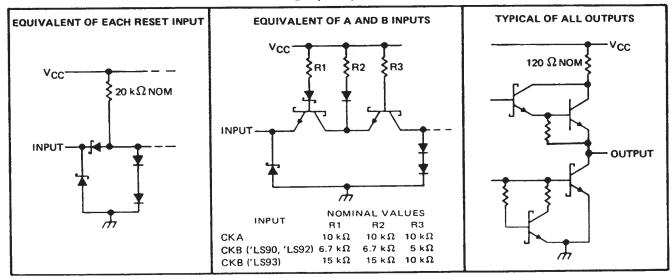
'90A, '92A, '93A



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#### schematics of inputs and outputs (continued)

'LS90, 'LS92, 'LS93



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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)											7 V
Input voltage											5.5 V
Interemitter voltage (see Note 2)											5.5 V
Operating free-air temperature range:	SN5490A, S	SN5492A	SN5493A						–55°C	to '	125°C
Special and a service and a se	SN7490A, S	SN7492A	SN7493A						. 0°0	C to	70°C
Storage temperature range											

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.

2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the two R<sub>0</sub> inputs, and for the '90A circuit, it also applies between the two Rg inputs.

#### recommended operating conditions

		i	00A, SN SN5493		SN749	UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V <sub>CC</sub>		4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH		_	-800			-800	μΑ	
Low-level output current, IOI				16			16	mA
	A input	0		32	0		32	MHz
Count frequency, f <sub>count</sub> (see Figure 1)	B input	0		16	0		16	141112
	A input	15			15			
Pulse width, tw	8 input	30			30			ns
•	Reset inputs	15			15			
Reset inactive-state setup time, t <sub>SU</sub>		25			25			ns
Operating free-air temperature, T <sub>A</sub>				125	0		70	°C

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

						'90A			'92A			'93A		UNIT
	PARAMETE	R¶	TEST CONDIT	TIONST	MIN	TYP‡	MAX	MIN	TYP	MAX	MIN	TYP <sup>‡</sup>	MAX	UNIT
VIH	High-level inpu	ıt voltage			2			2			2			V
VIL	Low-level inpu						0.8			0.8			8.0	٧
VIK	Input clamp vo		VCC = MIN, II = -	-12 mA			-1.5			-1.5			-1.5	V
	High-level outp		V <sub>CC</sub> = MIN, V <sub>IH</sub> V <sub>IL</sub> = 0.8 V, I <sub>OH</sub>	= 2 V,	2.4	3.4		2.4	3.4		2.4	3.4		V
VOL	Low-level outp	out voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub>	= 2 V,		0.2	0.4		0.2	0.4		0.2	0.4	٧
11	Input current maximum input		V <sub>CC</sub> = MAX, V <sub>1</sub> = 5.5 V				1			1			1	mA
		Any reset					40			40			40	
ίн	High-level	CKA	VCC = MAX, VI =	2.4 V			80			80			80	μΑ
111	input current	СКВ					120			120			80	<u> </u>
		Any reset					-1.6			-1.6			-1.6	]
l <sub>IL</sub>	Low-level	CKA	VCC = MAX, VI =	0.4 V			-3.2			-3.2			-3.2	mA
.1.	input current	СКВ	1	CC mind of one			-4.8			-4.8			-3.2	
	Short-circuit		SN54'		-20		-57	-20		-57	-20		-57	mA
los	00		VCC = MAX	SN74'	-18		-57	-18		-57	-18		57	
¹cc	Supply curren		V <sub>CC</sub> = MAX, See Note 3			29	42		26	39		26	39	mA

<sup>&</sup>lt;sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 3: I<sub>CC</sub> is measured with all outputs open, both R<sub>0</sub> inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.



 $<sup>^{\</sup>ddagger}$ All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_{A} = 25 ^{\circ}\text{C}$ .

Not more than one output should be shorted at a time.

 $<sup>\</sup>P_{Q_A}$  outputs are tested at  $I_{QL}$  = 16 mA plus the limit value for  $I_{IL}$  for the CKB input. This permits driving the CKB input while maintaining

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# switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$

	FROM	TO			'90A			'92A			'93A		UNIT
PARAMETER <sup>†</sup>	(INPUT)	(OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	OWIT
	CKA	QA		32	42		32	42		32	42		MHz
f <sub>max</sub>	СКВ	QB		16			16			16			
tPLH	CKA				10	16		10	16		10	16	ns
tPHL .		QΑ			12	18		12	18		12	18	
tPLH		0			32	48		32	48		46	70	ns
tPHL	CKA	$\sigma^{D}$			34	50		34	50		46	70	,,,,
tPLH .		_	CL = 15 pF,		10	16		10	16		10	16	ns
tPHL	СКВ	QΒ	R <sub>L</sub> = 400 Ω,		14	21		14	21		14	21	
tPLH			See Figure 1		21	32		10	16_		21	32	ns
tPHL	СКВ	ОC			23	35		14	21		23	35	113
tPLH		_	1		21	32		21	32		34	51	ns
tPHL	СКВ	σD			23	35		23	35		34	51	113
tPHL	Set-to-0	Any			26	40		26	40		26	40	ns
tPLH		$Q_A, Q_D$	1		20	30							ns
	tPHL Set-to-9 QB, QC		1		26	40							

 $<sup>^{\</sup>dagger}f_{max} = maximum count frequency$ 

tpLH ≡ propagation delay time, low-to-high-level output

tpHL ≡ propagation delay time, high-to-low-level output

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)			 	 	 	 		7 V
Input voltage: R inputs			 	 	 	 		7 V
A and B inputs .			 	 	 	 		5.5 V
Operating free-air temperature range:	SN54LS	' Circuits		 	 			-55°C to 125°C
								. 0°C to 70°C
Storage temperature range								-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

#### recommended operating conditions

		SN54LS90 SN54LS92 SN54LS93			SN74LS90 SN74LS92 SN74LS93			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, VCC		4.5	5	5.5	4.75	5	5.25	٧
High-level output current, IOH				-400			-400	μА
Low-level output current, IOL				4			8	mA
Count (	A input	0		32	32 0		32	MHz
Count frequency, f <sub>count</sub> (see Figure 1)	B input	0		16	0		16	MHZ
	A input	15			15			
Pulse width, tw	B input	30			30			ns
	Reset inputs	30			30			1
Reset inactive-state setup time, t <sub>su</sub>		25			25			ns
Operating free-air temperature, TA		-55		125	0		70	°C

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		•			•								
						1	N54LS9		_	N74LS9			
	PARAMET	rer	TE:	ST CONDITION	Sī	S	N54LS9	92	S	N74LS9	12	UNIT	
						MIN	TYP‡	MAX	MIN	TYP‡	MAX		
$V_{IH}$	High-level inpu	t voltage				2			2			V	
VIL	Low-level input	t voltage						0.7			0.8	٧	
VIK	Input clamp vo	Itage	V <sub>CC</sub> = MIN,	$I_1 = -18 \text{ mA}$				-1.5			-1.5	٧	
Vон	High-level outp	gh-level output voltage $ \begin{array}{c} V_{CC} = MIN, & V_{IH} = 2 V, \\ V_{IL} = V_{IL} max, & I_{OH} = -400  \mu A \end{array} $		2.5	3.4		2.7	3.4		V			
V	1 and land and	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 4 mA¶			0.25	0.4		0.25	0.4	v			
VOL Low-level output v		ut voitage	VIL = VIL max,		10L = 8 mA¶					0.35	0.5	ľ	
	Input current	Any reset	V <sub>CC</sub> = MAX,	V <sub>1</sub> = 7 V				0.1			0.1		
11	at maximum	CKA		V . F.F.V				0.2			0,2	mA	
	input voltage	CKB	V <sub>CC</sub> = MAX,	$V_1 = 5.5 V$				0.4			0.4		
	High-level	Any reset						20			20		
чн	_	CKA	VCC = MAX,	$V_1 = 2.7 V$				40			40	μА	
	input current	СКВ						80			80		
	Low-level	Any reset						-0.4			-0.4		
11L		CKA	V <sub>CC</sub> = MAX,	$V_{CC} = MAX$ , $V_1 = 0.4 V$				-2.4			-2.4	mA	
	input current	CKB						-3.2			-3.2		
los	Short-circuit ou	tput current§	VCC = MAX			-20		-100	-20		-100	mA	
laa	Supply current		V <sub>CC</sub> = MAX,	See Note 2	'LS90		9	15		9	15	mA	
ICC	C Supply current	Supply current		VCC - WAX,	See Note 3	'LS92		9	15		9	15	IIIA

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 3: ICC is measured with all outputs open, both RO inputs grounded following momentary connection to 4,5 V, and all other inputs grounded.



 $<sup>\</sup>ddagger$ All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

<sup>§</sup>Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

<sup>¶</sup>QA outputs are tested at specified IOL plus the limit value of IIL for the CKB input. This permits driving the CKB input while maintaining full fan-out capability.

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

					•	S	N54LS9	3	S	N74LS9	3	
	PARAMET	ER	TE	ST CONDITIONS	5'	MIN	TYP‡	MAX	MIN	TYP‡	MAX	UNIT
VIH	High-level inpu	t voltage				2			2			V
VIL	Low-level input	t voltage						0.7			8.0	٧
VIK	Input clamp vo	Itage	V <sub>CC</sub> = MIN,	1 <sub>1</sub> = -18 mA				-1.5			-1.5	V
Vон	High-level outp	ut voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = V <sub>IL</sub> max,	V <sub>IH</sub> = 2 V, 1 <sub>OH</sub> = -400 μA	λ.	2.5	3.4		2.7	3.4		V
	VOL Low-level output voltage		VCC = MIN,	V <sub>IH</sub> = 2 V,	IOL = 4 mA¶		0.25	0.4		0.25	0.4	V
VOL			VIL = VIL max		I <sub>OL</sub> = 8 mA¶					0.35	0.5	
	Input current	Any reset	V <sub>CC</sub> = MAX,	V <sub>1</sub> = 7 V				0.1			0.1	mA
Ц	at maximum input voltage	CKA or CKB	V <sub>CC</sub> = MAX,	V <sub>1</sub> = 5.5 V				0.2			0.2	
	High-level	Any reset		V - 27V				20			20	μA
чн	input current	CKA or CKB	V <sub>CC</sub> = MAX,	$V_{l} = 2.7 V$				40			80	μΑ.
		Any reset						-0.4			-0.4	
IIL.	Low-level	CKA	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V					-2.4			-2.4	mA
	input current	CKB	1					-1.6			-1.6	<u> </u>
los	Short-circuit or	utput current §	V <sub>CC</sub> = MAX			-20		-100	-20		-100	mA
Icc			V <sub>CC</sub> = MAX,	See Note 3			9	15		9	15	mA

<sup>&</sup>lt;sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions

## switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$

	FROM	TO			'LS90			LS92			'LS93		UNIT
PARAMETER#	(INPUT)	(OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	Olviii
	CKA	QΑ		32	42		32	42		32	42		MHz
f <sub>max</sub>	CKB	QB	1	16			16			16			
tPLH	OK A	0.	1		10	16		10	16		10	16	ns
<sup>t</sup> PHL	CKA	QA	12 18 12	18		12	18						
tPLH .	CKA	0			32	48		32	48		46	70	ns
tPHL	CKA	αD	CL = 15 pF,		34	50		34	50		46	70	
tPLH					10	16		10	16		10	16	ns
tPHL	СКВ	ΩB	R <sub>L</sub> = 2 kΩ		14	21		14	21		14	21	113
†PLH		_	See Figure 1		21	32		10	16		21	32	ns
tPHL	CKB	ac			23	35		14	21		23	35	113
tPLH					21	32		21	32		34	51	ns
<sup>1</sup> PHL	CKB	σD	1		23	35		23	35		34	51	13
tPHL	Set-to-0	Any	1		26	40		26	40		26	40	ns
tPLH		Q <sub>A</sub> , Q <sub>D</sub>	1		20	30							ns
tPHL	Set-to-9	Q <sub>B</sub> , Q <sub>C</sub>	1		26	40							

<sup>#</sup>fmax = maximum count frequency



<sup>‡</sup>All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

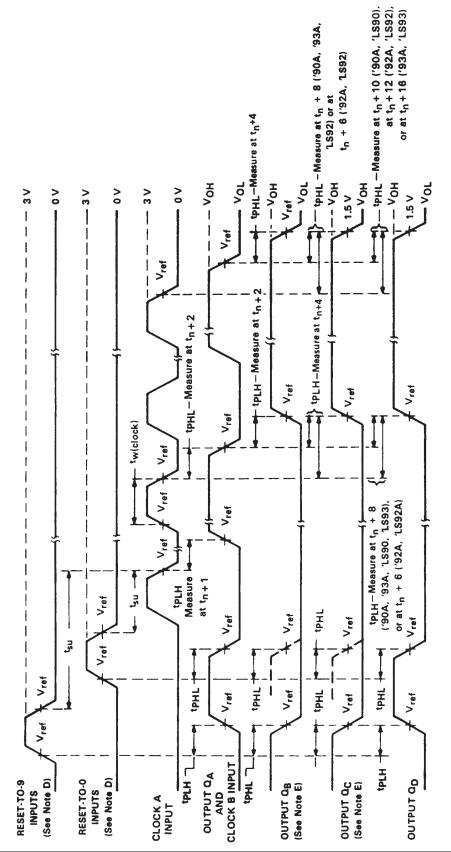
Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

<sup>¶</sup>QA outputs are tested at specified IQL plus the limit value for IIL for the CKB input. This permits driving the CKB input while maintaining full fan-out capability.

NOTE 3: I<sub>CC</sub> is measured with all outputs open, both R<sub>0</sub> inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

 $tp_{LH} = propagation delay time, low-to-high-level output$ 

tpHL = propagation delay time, high-to-low-level output



NOTES: A. Input pulses are supplied by a generator having the following characteristics:

for 'LS90, 'LS92, 'LS93,  $t_f \le 15$  ns,  $t_f \le 5$  ns, PRR = 1 MHz, duty cycle = 50%,  $Z_{out} \approx 50$  ohms. for '90A, '92A, '93A, t<sub>f</sub> ≤ 5 ns, t<sub>f</sub> ≤ 5 ns, PRR = 1 MHz, duty cycle = 50%, Z<sub>out</sub> ≈ 50 ohms;

- CL includes probe and jig capacitance. All diodes are 1N3064 or equivalent.
- Each reset input is tested separately with the other reset at 4.5 V. BB CJ CJ UJ UL
  - Reference waveforms are shown with dashed lines.
- For '90A, '92A, and '93A;  $V_{ref} = 1.5 \text{ V}$ . For 'LS90, 'LS92, and 'LS93;  $V_{ref} = 1.3 \text{ V}$ .

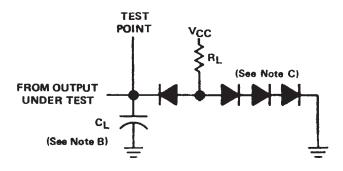
# FIGURE 1A



PARAMETER MEASUREMENT INFORMATION

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#### PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

- NOTES: A. Input pulses are supplied by a generator having the following characteristics: for '90A, '92A, '93A,  $t_r \le 5$  ns,  $t_f \le 5$  ns, PRR = 1 MHz, duty cycle = 50%,  $z_{out} \approx 50$  ohms; for 'LS90, 'LS92, 'LS93,  $t_r \le 15$  ns,  $t_f \le 5$  ns, PRR = 1 MHz, duty cycle = 50%,  $z_{out} \approx 50$  ohms.
  - B. C<sub>L</sub> includes probe and jig capacitance.
  - C. All diodes are 1N3064 or equivalent.
  - D. Each reset input is tested separately with the other reset at  $4.5\ V.$
  - E. Reference waveforms are shown with dashed lines.
  - F. For '90A, '92A, and '93A;  $V_{ref} = 1.5 \text{ V}$ . For 'LS90, 'LS92, and 'LS93;  $V_{ref} = 1.3 \text{ V}$ .

FIGURE 1B

25-Jan-2012

#### **PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
7603201CA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Call TI	
7603201DA	ACTIVE	CFP	W	14	1	TBD	Call TI	Call TI	
7700101CA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Call TI	
7700101DA	ACTIVE	CFP	W	14	1	TBD	Call TI	Call TI	
JM38510/31501BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
JM38510/31501BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
JM38510/31502BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
JM38510/31502BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
M38510/31501BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
M38510/31501BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
M38510/31502BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
M38510/31502BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
SN5490AJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	
SN5492AJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	
SN54LS90J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SN54LS93J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SN7490AN	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	
SN7492AN	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	
SN7493AN	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	
SN74LS90D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS90DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS90DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS90DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS90DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS90DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	



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SN74LS90N SN74LS90NE4 SN74LS92D SN74LS92DE4 SN74LS92DG4 SN74LS92NS SN74LS92N3 SN74LS92NSR	ACTIVE ACTIVE ACTIVE ACTIVE	PDIP PDIP SOIC	N N D	14 14	25 25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS92D  SN74LS92DE4  SN74LS92DG4  SN74LS92N  SN74LS92N3  SN74LS92NE4	ACTIVE			14	O.F				
SN74LS92DE4 SN74LS92DG4 SN74LS92N SN74LS92N3 SN74LS92NE4	ACTIVE	SOIC			∠5	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS92DG4  SN74LS92N  SN74LS92N3  SN74LS92NE4			5	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS92N SN74LS92N3 SN74LS92NE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS92N3 SN74LS92NE4		SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS92NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	
SN74LS92NSR	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS92NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS92NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS93D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS93DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS93DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS93N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS93N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	
SN74LS93NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS93NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS93NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS93NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS	CU NIPDAU	Level-1-260C-UNLIM	
SNJ5490AJ						& no Sb/Br)			
SNJ5490AW	OBSOLETE	CDIP	J	14		& no Sb/Br) TBD	Call TI	Call TI	



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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SNJ5492AJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	
SNJ5492AW	OBSOLETE	CFP	W	14		TBD	Call TI	Call TI	
SNJ54LS90J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SNJ54LS90W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
SNJ54LS93J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SNJ54LS93W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### OTHER QUALIFIED VERSIONS OF SN5490A, SN5492A, SN54LS90, SN54LS93, SN7490A, SN7492A, SN74LS90, SN74LS93:

Catalog: SN7490A, SN7492A, SN74LS90, SN74LS93





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• Military: SN5490A, SN5492A, SN54LS90, SN54LS93

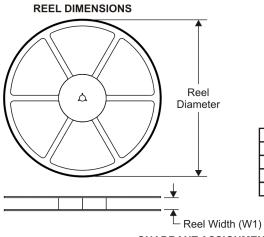
NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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#### TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

All difficultions are norminal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS90DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS92NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LS93NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

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\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS90DR	SOIC	D	14	2500	346.0	346.0	33.0
SN74LS92NSR	SO	NS	14	2000	346.0	346.0	33.0
SN74LS93NSR	SO	NS	14	2000	346.0	346.0	33.0

### 14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

# W (R-GDFP-F14)

## CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB



## N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



## D (R-PDSO-G14)

#### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



# D (R-PDSO-G14)

# PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



#### **MECHANICAL DATA**

## NS (R-PDSO-G\*\*)

# 14-PINS SHOWN

#### PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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