

Data sheet acquired from Harris Semiconductor ${\rm SCHS163F}$

September 1997 - Revised October 2003

High-Speed CMOS Logic Presettable Synchronous 4-Bit Up/Down Counters

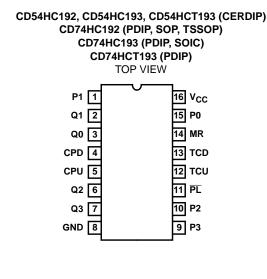
Features

- Synchronous Counting and Asynchronous Loading
- Two Outputs for N-Bit Cascading
- Look-Ahead Carry for High-Speed Counting
- Fanout (Over Temperature Range)
 - Standard Outputs..... 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)
 - CMOS Input Compatibility, II \leq 1 μA at V_OL, V_OH

Description

The 'HC192, 'HC193 and 'HCT193 are asynchronously presettable BCD Decade and Binary Up/Down synchronous counters, respectively.

Pinout



Presetting the counter to the number on the preset data inputs (P0-P3) is accomplished by a LOW asynchronous parallel load input (PL). The counter is incremented on the low-to-high transition of the Clock-Up input (and a high level on the Clock-Down input) and decremented on the low to high transition of the Clock-Down input (and a high level on the Clock-up input). A high level on the MR input overrides any other input to clear the counter to its zero state. The Terminal Count up (carry) goes low half a clock period before the zero count is reached and returns to a high level at the zero count. The Terminal Count Down (borrow) in the count down mode likewise goes low half a clock period before the maximum count (9 in the 192 and 15 in the 193) and returns to high at the maximum count. Cascading is effected by connecting the carry and borrow outputs of a less significant counter to the Clock-Up and Clock-Down inputs, respectively, of the next most significant counter.

If a decade counter is preset to an illegal state or assumes an illegal state when power is applied, it will return to the normal sequence in one count as shown in state diagram.

Ordering Information

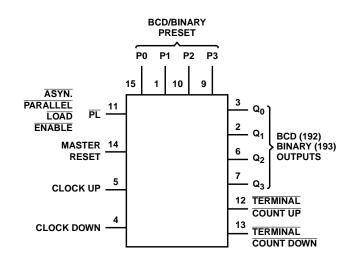
PART NUMBER	TEMP. RANGE (^o C)	PACKAGE
CD54HC192F3A	-55 to 125	16 Ld CERDIP
CD54HC193F3A	-55 to 125	16 Ld CERDIP
CD54HCT193F3A	-55 to 125	16 Ld CERDIP
CD74HC192E	-55 to 125	16 Ld PDIP
CD74HC192NSR	-55 to 125	16 Ld SOP
CD74HC192PW	-55 to 125	16 Ld TSSOP
CD74HC192PWR	-55 to 125	16 Ld TSSOP
CD74HC192PWT	-55 to 125	16 Ld TSSOP
CD74HC193E	-55 to 125	16 Ld PDIP
CD74HC193M	-55 to 125	16 Ld SOIC
CD74HC193MT	-55 to 125	16 Ld SOIC
CD74HC193M96	-55 to 125	16 Ld SOIC
CD74HCT193E	-55 to 125	16 Ld PDIP

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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Functional Diagram



TRUTH TABLE

CLOCK UP	CLOCK DOWN	RESET	PARALLEL LOAD	FUNCTION
Ŷ	Н	L	Н	Count Up
Н	Ŷ	L	Н	Count Down
Х	Х	н	Х	Reset
х	х	L	L	Load Preset Inputs

H = High Voltage Level, L = Low Voltage Level, X = Don't Care, \uparrow = Transition from Low to High Level

Absolute Maximum Ratings

DC Supply Voltage, V _{CC} 0.5V to 7V
DC Input Diode Current, I _{IK}
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ ±20mA
DC Output Diode Current, I _{OK}
For $V_0 < -0.5V$ or $V_0 > V_{CC} + 0.5V$
DC Output Source or Sink Current per Output Pin, IO
For $V_0 > -0.5V$ or $V_0 < V_{CC} + 0.5V$
DC V _{CC} or Ground Current, I _{CC or} I _{GND} ±50mA
Operating Conditions

Temperature Range (T _A)55°C to 125°C
Supply Voltage Range, V _{CC}
HC Types
HCT Types4.5V to 5.5V
DC Input or Output Voltage, V _I , V _O 0V to V _{CC}
Input Rise and Fall Time
2V
4.5V 500ns (Max)
6V

Thermal Information

Package Thermal Impedance, θ_{JA} (see Note 1):
E (PDIP) Package
M (SOIC) Package
NS (SOP) Package 64 ^o C/W
PW (TSSOP) Package 108 ^o C/W
Maximum Junction Temperature 150 ^o C
Maximum Storage Temperature Range65°C to 150°C
Maximum Lead Temperature (Soldering 10s)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

		С	TEST ONDITION	IS		25 ⁰ C		-40 ⁰ C T	O 85°C	-55°C T	O 125ºC		
PARAMETER	SYMBOL	V _I (V)	I _O (mA)	V _{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS	
HC TYPES													
High Level Input	VIH	-	-	2	1.5	-	-	1.5	-	1.5	-	V	
Voltage				4.5	3.15	-	-	3.15	-	3.15	-	V	
				6	4.2	-	-	4.2	-	4.2	-	V	
Low Level Input	V _{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V	
Voltage				4.5	-	-	1.35	-	1.35	-	1.35	V	
				6	-	-	1.8	-	1.8	-	1.8	V	
High Level Output	V _{OH}	V _{IH} or	-0.02	2	1.9	-	-	1.9	-	1.9	-	V	
Voltage CMOS Loads		VIL	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V	
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V	
High Level Output			-4	4.5	3.98	-	-	3.84	-	3.7	-	V	
Voltage TTL Loads			-5.2	6	5.48	-	-	5.34	-	5.2	-	V	
Low Level Output	V _{OL}	V _{IH} or	0.02	2	-	-	0.1	-	0.1	-	0.1	V	
Voltage CMOS Loads		VIL	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V	
			0.02	6	-	-	0.1	-	0.1	-	0.1	V	
Low Level Output			4	4.5	-	-	0.26	-	0.33	-	0.4	V	
Voltage TTL Loads			5.2	6	-	-	0.26	-	0.33	-	0.4	V	
Input Leakage Current	lı	V _{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	μΑ	
Quiescent Device Current	Icc	V _{CC} or GND	0	6	-	-	8	-	80	-	160	μΑ	

DC Electrical Spec	cifications	S (Con	tinued)										
		TEST CONDITIONS				25 ⁰ C			о 85°С	-55°C T	O 125 ⁰ C		
PARAMETER	SYMBOL	V _I (V)	I _O (mA)	V _{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX		
HCT TYPES													
High Level Input Voltage	VIH	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V	
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V	
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V	
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V	
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V	
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V	
Input Leakage Current	lı	V _{CC} to GND	-	5.5	-	-	±0.1	-	±1	-	±1	μA	
Quiescent Device Current	Icc	V _{CC} or GND	-	5.5	-	-	8	-	80	-	160	μΑ	
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI _{CC} (Note 2)	V _{CC} - 2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA	

NOTE:

2. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
P0-P3	0.4
MR	1.45
PL	0.85
CPU, CPD	1.45

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g. $360\mu A$ max at $25^{\circ}C$.

			v _{cc}		25 ⁰ C		-40°C 1	O 85°C	-55°C T	O 125 ⁰ C	
PARAMETER		SYMBOL	(V)	MIN	ТҮР	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES				-	-	-	-		-	-	
Pulse Width		t _W	2	115	-	-	145	-	175	-	ns
CPU, CPD			4.5	23	-	-	29	-	35	-	ns
	192		6	20	-	-	25	-	30	-	ns
		t _W	2	100	-	-	125	-	150	-	ns
CPU, CPD		Γ	4.5	20	-	-	25	-	30	-	ns
	193	Γ	6	17	-	-	21	-	26	-	ns
PL		t _W	2	80	-	-	100	-	120	-	ns
			4.5	16	-	-	20	-	24	-	ns
			6	14	-	-	17	-	20	-	ns
MR		t _W	2	100	-	-	125	-	150	-	ns
			4.5	20	-	-	25	-	30	-	ns
			6	17	-	-	21	-	26	-	ns
Set-up Time		t _{SU}	2	80	-	-	100	-	120	-	ns
Pn to PL			4.5	16	-	-	20	-	24	-	ns
			6	14	-	-	17	-	20	-	ns
Hold Time		t _H	2	0	-	-	0	-	0	-	ns
Pn to \overline{PL}			4.5	0	-	-	0	-	0	-	ns
		-	6	0	-	-	0	-	0	-	ns
Hold Time		t _H	2	80	<u> </u>	<u> </u>	100		120	_	ns
CPD to CPU or			4.5	16	-	-	20		24	-	ns
CPU to CPD		-	6	14	-	_	17	-	24	_	ns
Recovery Time		tana	2	80		_	100	_	120	-	
PL to CPU, CPD		^t REC	4.5	16		-	20	-	24	-	ns
		-		14			17	-		-	ns
			6						20		ns
MR to CPU, CPD		^t REC	2	5	-	-	5	-	5	-	ns
		-	4.5	5	-	-	5	-	5	-	ns
			6	5	-	-	5	-	5	-	ns
Maximum Frequency		fMAX	2	5	-	-	4	-	3	-	MHz
CPU, CPD			4.5	22	-	-	18	-	15	-	MHz
	192		6	24	-	-	21	-	18	-	MHz
		fmax	2	5	-	-	4	-	3	-	MHz
CPU, CPD			4.5	25	-	-	20	-	17	-	MHz
	193		6	29	-	-	24	-	20	-	MHz
HCT TYPES		. I									
Pulse Width		t _W	2	-	-	-	-	-	-	-	ns
CPU, CPD			4.5	23	-	-	29	-	35	-	ns
	192		6	-	-	-	-	-	-	-	ns
CPU, CPD		t _W	2	-	-	-	-	-	-	-	ns
	193		4.5	23	-	-	29	-	35	-	ns
			6	-	-	-	-	-	-	-	ns

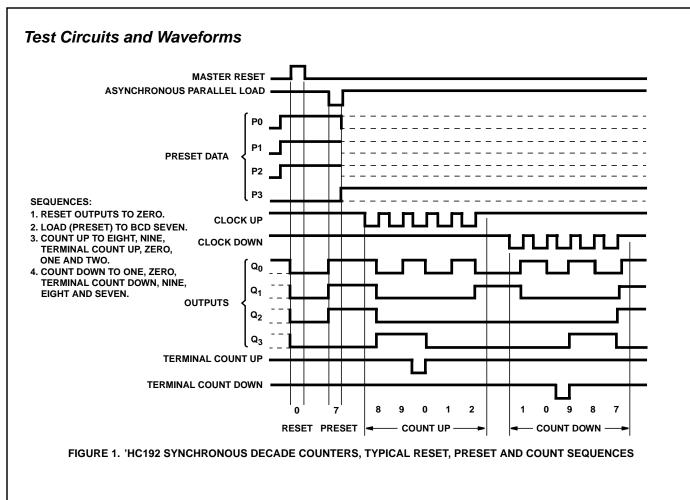
	、			25 ⁰	°C		-40°	С ТО 850	°C -55°	νсто	125 ⁰ C		
SYMBOL		(V)	MIN	TY	P	MAX	MIN	MA	х м	IN	MAX	UN	IITS
t _W		2	-	-		-	-	-	-	-	-	r	าร
		4.5	16	-		-	20	-	2	4	-	r	าร
		6	-	-		-	-	-	-		-	r	าร
t _W		2	-	-		-	-	-	-		-	r	าร
		4.5	20	-		-	25	-	3	0	-	r	าร
		6	-	-		-	-	-	-		-	r	าร
ts∪		2	-	-		-	-	-	-		-	r	าร
		4.5	15	-		-	19	-	2	2	-	r	าร
		6	-	-		-	- 1				-	r	าร
t _H		2	-	-		-	-	-			-	r	าร
		4.5	0	-		-	0			,	-	r	าร
		6	-	-		-	- 1	-	-	.	-	r	าร
t _H		2	-	-		-	-	-	-	.	-	r	าร
		4.5	16	-		-	20		2	4	-	r	าร
		6	-	-		-	-	-			-	r	าร
t _{REC}		2	-	-		-	- 1	<u> </u>		.	-		าร
		4.5	15	-		-	19		2	2	-	r	าร
		6	-	-		-	<u> </u>	+ -	<u> </u>	. +	-	r r	าร
t _{REC}		2	-	-		-	- 1	<u> </u>			-	r r	าร
TREO			5	-		-	5	<u> </u>		5	-		าร
			-	-		-	-	<u> </u>			-		าร
fMAX		-	-	-		-	<u> </u>	+ -	<u> </u>		-	<u> </u>	IHz
IWIAA			22	-		-	18	+ -	1	5	-	<u> </u>	IHz
				_		_		_			<u> </u>		IHz
		-		+	_	_	<u> </u>	_					IHz
				+				_					IHz
				+				_				<u> </u>	IHz
		0											
S Input t _r , t _f	= 6ns					0-						-0-1	
				V _{CC}									
SYME	BOL	COND	THONS	(V)	MIN		MAX	MIN	WAX			X I	UN
touu t		Cı = 5	0nF	2	I .	<u> </u>	125	_	155	<u> </u>	10	10	1
PLH, Y	PHL										_		
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					<u> </u>								
<u> </u>					<u> </u>						_		
^t PLH,	^I PHL				<u> </u>						_		
					<u> </u>					-	_		
					<u> </u>						_		
					—						_		
t _{PLH} ,	^t PHL				-	-		-		-			
		$C_{L} = 5$	0pF	4.5	-	-	43	-	54	-	6	5	
		C _L = 1		5		18				<u> </u>		<u> </u>	
	tw tw tw tsu th th th tREC fMAX fMAX fMAX fMAX tPLH, t tPLH, t	SYMBOL I tw	tw 2 tw 2 tw 2 tw 2 4.5 6 tw 2 4.5 6 tsu 2 4.5 6 tH 2 tH 2 tH 2 tH 2 4.5 6 tREC 2 4.5 6 tREC 2 4.5 6 fMAX 2 for the	SYMBOL (V) MIN tw 2 - 4.5 16 6 - tw 2 - tw 2 - 4.5 20 6 tw 2 - tsu 2 - tsu 2 - 4.5 15 6 th 2 - 4.5 0 6 th 2 - 4.5 0 6 th 2 - th 2 - th 2 - th 2 - tkec 2 - tkec 2 - thkx 2 - tkec 2 - thkec 2 - thkec 2 - thkec 2 - thkec 2	SYMBOL VCC (V) MIN TY tw 2 - - 4.5 16 - 6 - - tw 2 - - 4.5 20 - 4.5 20 - 6 - - tw 2 - - 4.5 15 - 6 - - - 4.5 15 - - 4.5 16 - - - 4.5 16 - - - - th 2 - - - - - th 2 - - - - - - the 2 - - - - - - the 2 - - - - - - the 2	SYMBOL VCC (V) MIN TYP tw 2 - - 4.5 16 - 1 6 - - 1 tw 2 - - 1 tw 2 - - 1 tw 2 - - 1 4.5 20 - 1 1 4.5 15 - 1 1 th 2 - - 1 4.5 15 - 1 1 th 2 - - 1 th	SYMBOL VCC (V) MIN TYP MAX tw 2 - - - 4.5 16 - - 6 - - - tw 2 - - 4.5 16 - - tw 2 - - 4.5 20 - - 4.5 15 - - 4.5 15 - - 4.5 0 - - 4.5 0 - - 4.5 16 - - 4.5 16 - - 4.5 16 - - 4.5 15 - - 4.5 15 - - 4.5 5 - - 4.5 22 - - fmAx 2 - - fmAx	SYMBOL VCC 4.5 MIN TYP MAX MIN 4.5 16 - - 20 6 - - - 20 6 - - - 20 4.5 20 - - 20 4.5 20 - - 25 6 - - - 25 6 - - - 25 6 15 - - 19 6 - - - 19 6 - - - 0 4.5 16 - - 10 4.5 16 - - 10 4.5 16 - - 10 4.5 15 - - 10 4.5 15 - - 10 4.5 22 - - 10 fMA	SYMBOL VCC (V) MIN TYP MAX MIN MAX tw 2 -	SYMBOL V(C) (V) MIN TYP MAX MIN MAX MIN 10 2 - - - 20 - 2 6 - - - 20 - 2 6 - - - - - - - 4.5 20 - <	SYMBOL VV MIN TYP MAX MIN MAX </td <td>SYMBOL VVC (V) MIN TYP MAX MIN MAX MIN MAX tw 2 .<</td> <td>SYMBOL '''CO MIN TYP MAX MIN MA</td>	SYMBOL VVC (V) MIN TYP MAX MIN MAX MIN MAX tw 2 .<	SYMBOL '''CO MIN TYP MAX MIN MA

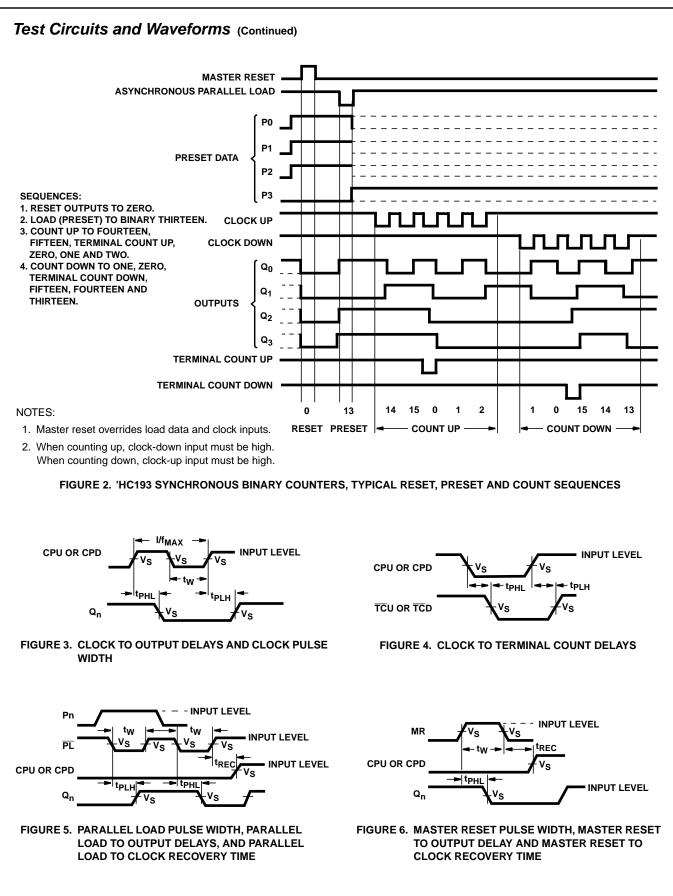
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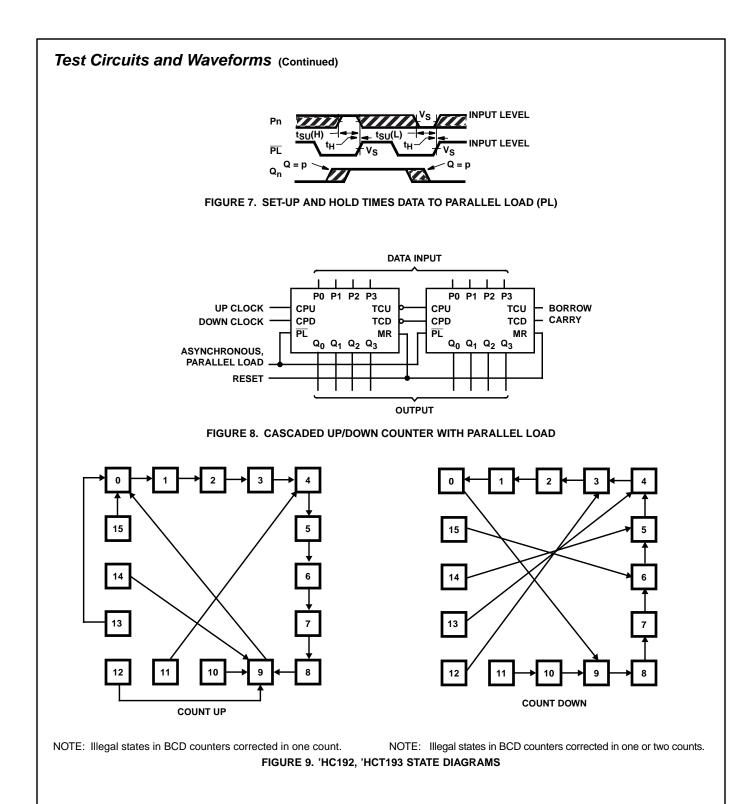
		TEST	v _{cc}		25 ⁰ C		-40°C 1	O 85°C	-55°C T	O 125 ⁰ C	
PARAMETER	SYMBOL	CONDITIONS	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
CPD to Q _n	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	220	-	270	-	325	ns
		C _L = 50pF	4.5	-	-	43	-	54	-	65	ns
		C _L = 15pF	5	-	18	-	-	-	-		ns
		C _L = 50pF	6	-	-	37	-	46	-	55	ns
PL to Q _n	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	220	-	275	-	330	ns
		$C_L = 50 pF$	4.5	-	-	44	-	55	-	66	ns
		C _L = 15pF	5	-	18	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	37	-	47	-	56	ns
MR to Q _n	tPHL	C _L = 50pF	2	-	-	200	-	250	-	300	ns
		C _L = 50pF	4.5	-	-	40	-	50	-	60	ns
		C _L = 15pF	5	-	17	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	34	-	43	-	51	ns
Transition Time	t _{TLH} , t _{THL}	C _L = 50pF	2	-	-	75	-	95	-	110	ns
Q, TCU, TCD			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C _{IN}	C _L = 50pF	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 3, 4)	C _{PD}	C _L = 15pF	5	-	40	-	-	-	-	-	pF
HCT TYPES											
Propagation Delay	t _{PLH} , t _{PHL}	C _L = 50pF	4.5	-	-	27	-	34	-	41	ns
CPU to TCU		C _L = 15pF	5	-	11	-	-	-	-	-	ns
CPU to TCD	t _{PLH} , t _{PHL}	C _L = 50pF	4.5	-	-	27	-	34	-	41	ns
		C _L = 15pF	5	-	11	-	-	-	-	-	ns
CPU to Q _n	t _{PLH} , t _{PHL}	$C_L = 50 pF$	4.5	-	-	40	-	50	-	60	ns
		C _L = 15pF	5	-	17	-	-	-	-	-	ns
CPD to Q _n	t _{PLH} , t _{PHL}	$C_L = 50 pF$	4.5	-	-	40	-	50	-	60	ns
		C _L = 15pF	5	-	17	-	-	-	-	-	ns
PL to Q _n	t _{PLH} , t _{PHL}	$C_L = 50 pF$	4.5	-	-	46	-	58	-	69	ns
		C _L = 15pF	5	-	21	-	-	-	-	-	ns
MR to Q _n	t _{PHL}	$C_L = 50 pF$	4.5	-	-	43	-	54	-	65	ns
		C _L = 15pF	5	-	18	-	-	-	-	-	ns
Transition Time	t _{TLH} , t _{THL}	C _L = 50pF									
Q, TCU, TCD			4.5	-	-	15	-	19	-	22	ns
Input Capacitance	C _{IN}	C _L = 50pF	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 3, 4)	C _{PD}	C _L = 15pF	5	-	50	-	-	-	-	-	pF

NOTES:

3. C_{PD} is used to determine the dynamic power consumption, per gate. 4. $P_D = V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.









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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-8780801EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Call TI	
5962-9084801MEA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Call TI	
9084801MEAS2035	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	
CD54HC192F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
CD54HC193F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
CD54HCT193F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
CD74HC192E	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HC192EE4	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HC192NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC192NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC192NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC192PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC192PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC192PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC192PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC192PWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC192PWTG4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC193E	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HC193EE4	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HC193M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC193M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	



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Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
CD74HC193M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC193M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC193ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC193MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC193MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC193MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC193MTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT193E	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HCT193EE4	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and pa

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF CD54HC192, CD54HC193, CD54HC193, CD74HC192, CD74HC193, CD74HC193 :

• Catalog: CD74HC192, CD74HC193, CD74HCT193

• Military: CD54HC192, CD54HC193, CD54HCT193

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

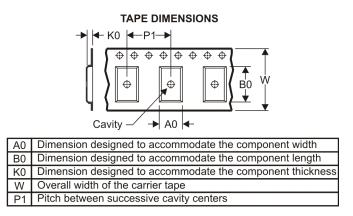
PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC192NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD74HC192PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC192PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC193M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

6-Aug-2010



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC192NSR	SO	NS	16	2000	346.0	346.0	33.0
CD74HC192PWR	TSSOP	PW	16	2000	346.0	346.0	29.0
CD74HC192PWT	TSSOP	PW	16	250	346.0	346.0	29.0
CD74HC193M96	SOIC	D	16	2500	333.2	345.9	28.6

J (R-GDIP-T**) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



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D (R-PDSO-G16) PLASTIC SMALL OUTLINE Stencil Openings (Note D) Example Board Layout (Note C) -16x0,55 - 14x1,27 -14x1,27 16x1,95 4,80 4,80 Example Non Soldermask Defined Pad Example Pad Geometry (See Note C) 0,60 Example 2,00 Solder Mask Opening

(See Note E)

NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

← 0,07 All Around

- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994. β . This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153



LAND PATTERN DATA



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 \bigcirc Gage Plane ₽ 0,25 7 1 1,05 0,55 0°-10° Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS ** 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G**)

14-PINS SHOWN

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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