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- Inputs Are TTL-Voltage Compatible
- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- SCR-Latchup-Resistant CMOS Process and Circuit Design
- Exceeds 2-kV ESD Protection per MIL-STD-883, Method 3015

#### CD54ACT161 . . . F PACKAGE CD74ACT161 . . . E OR M PACKAGE (TOP VIEW) CLR [ 16 V<sub>CC</sub> CLK 2 15 RCO A 🛮 3 14 🛮 Q<sub>A</sub> B 🛮 4 13 🛛 Q<sub>B</sub> C [ 5 12 Q<sub>C</sub> DΠ 6 11 Q<sub>D</sub> 10 ENT ENP II 7 9 LOAD GND 8

### description/ordering information

The 'ACT161 devices are 4-bit binary counters. These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes that normally are associated with synchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

These devices are fully programmable; that is, they can be preset to any number between 0 and 9 or 15. Presetting is synchronous; therefore, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

The clear function is asynchronous. A low level at the clear ( $\overline{\text{CLR}}$ ) input sets all four of the flip-flop outputs low, regardless of the levels of the CLK, load ( $\overline{\text{LOAD}}$ ), or enable inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are ENP, ENT, and a ripple-carry output (RCO). Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. Enabling RCO produces a high-level pulse while the count is maximum (9 or 15, with Q<sub>A</sub> high). This high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

The counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or  $\overline{\text{LOAD}}$ ) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

### **ORDERING INFORMATION**

TA	PAC	KAGEŤ	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP – E	Tube	CD74ACT161E	CD74ACT161E
_55°C to 125°C	SOIC - M	Tube	CD74ACT161M	ACT161M
-55 0 10 125 0	SOIC - W	Tape and reel	CD74ACT161M96	ACTION
	CDIP – F	Tube	CD54ACT161F3A	CD54ACT161F3A



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



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#### **FUNCTION TABLE**

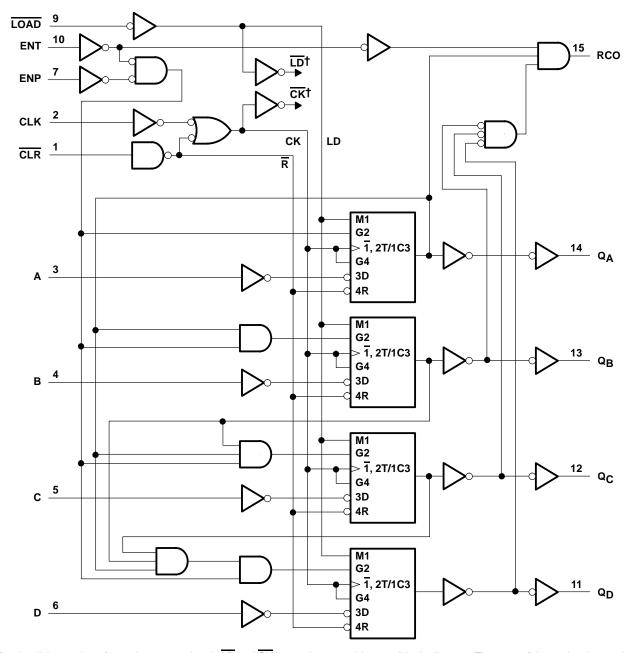
		IN	IPUTS		OUT	PUTS	FUNCTION	
CLR	CLK	ENP	ENT	LOAD	A,B,C,D	Qn	RCO	FUNCTION
L	Χ	Χ	Χ	Χ	Χ	L	L	Reset (clear)
Н	<b>↑</b>	Х	Х	I	I	L	L	Parallel load
Н	$\uparrow$	Χ	Χ	I	h	Н	Note 1	Parallel load
Н	<b>↑</b>	h	h	h	Χ	Count	Note 1	Count
Н	Χ	!	Χ	h	Х	q <sub>n</sub>	Note 1	Inhibit
Н	Χ	Χ	I	h	Χ	q <sub>n</sub>	L	HIHIDIL

H = high level, L = low level, X = don't care, h = high level one setup time prior to the CLK low-to-high transition, I = low level one setup time prior to the CLK low-to-high transition, q = the state of the referenced output prior to the CLK low-to-high transition, and  $\uparrow$  = CLK low-to-high transition.

NOTE 1: The RCO output is high when ENT is high and the counter is at terminal count (HHHH).



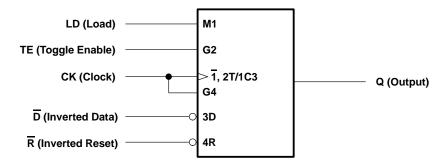
# logic diagram (positive logic)



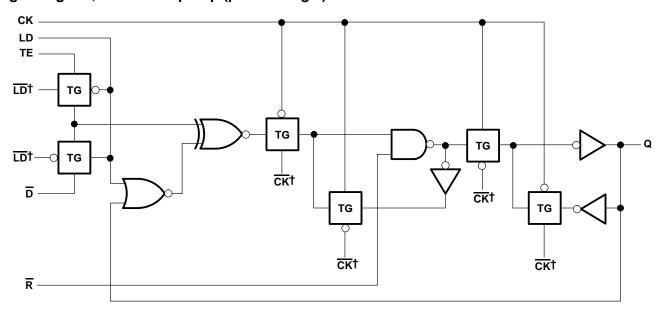
 $<sup>^{\</sup>dagger}$  For simplicity, routing of complementary signals  $\overline{\text{LD}}$  and  $\overline{\text{CK}}$  is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

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### logic symbol, each D/T flip-flop



## logic diagram, each D/T flip-flop (positive logic)

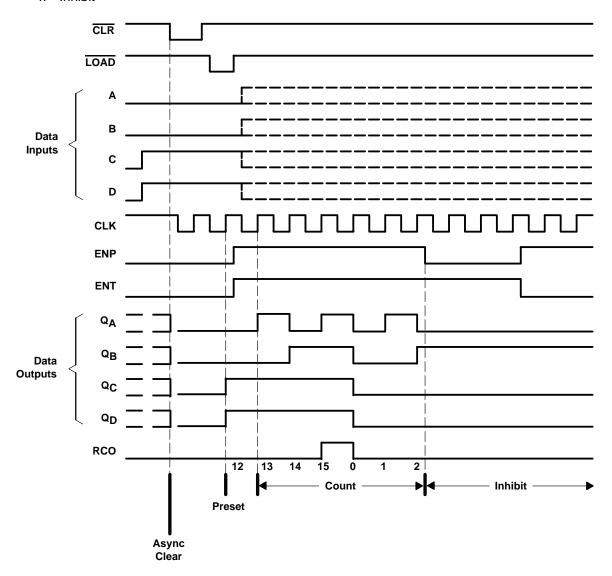


 $<sup>^{\</sup>dagger}$  The origins of  $\overline{LD}$  and  $\overline{CK}$  are shown in the logic diagram of the overall device.

### typical clear, preset, count, and inhibit sequence

The following sequence is illustrated below:

- 1. Clear outputs to zero (asynchronous)
- 2. Preset to binary 12
- 3. Count to 13, 14, 15, 0, 1, and 2
- 4. Inhibit



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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	–0.5 V to 6 V
Input clamp current, $I_{IK}$ ( $V_I < 0 \text{ V or } V_I > V_{CC}$ ) (see Note 2)	±20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 V or V <sub>O</sub> > V <sub>CC</sub> ) (see Note 2)	±50 mA
Continuous output current, I <sub>O</sub> (V <sub>O</sub> > 0 V or V <sub>O</sub> < V <sub>CC</sub> )	±50 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 3): E package	67°C/W
M package	73°C/W
Storage temperature range, T <sub>stg</sub>	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions (see Note 4)

		T <sub>A</sub> = 1	25°C	–55°0 125				UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Vcc	Supply voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
VIH	High-level input voltage	2		2		2		V
V <sub>IL</sub>	Low-level input voltage		0.8		0.8		0.8	V
٧ <sub>I</sub>	Input voltage	0	VCC	0	VCC	0	VCC	V
٧o	Output voltage	0	VCC	0	VCC	0	VCC	V
IOH	High-level output current		-24		-24		-24	mA
l <sub>OL</sub>	Low-level output current		24		24		24	mA
Δt/Δν	Input transition rise or fall rate		10		10		10	

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



NOTES: 2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>3.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST COND	VCC	T <sub>A</sub> = 25°C		–55°C to 125°C		–40°C to 85°C		UNIT	
				MIN MA	AΧ	MIN	MAX	MIN	MAX	
		I <sub>OH</sub> = -50 μA	4.5 V	4.4		4.4		4.4		
Vou	VI = VIH or VIL	$I_{OH} = -24 \text{ mA}$	4.5 V	3.94		3.7		3.8		V
VOH	v  = v H or v L	$I_{OH} = -50 \text{ mA}^{\dagger}$	5.5 V	-		3.85		_		
		$I_{OH} = -75 \text{ mA}^{\dagger}$	5.5 V					3.85		
		I <sub>OL</sub> = 50 μA	4.5 V	(	0.1	0.1			0.1	
\/a.	VI = VIH or VIL	I <sub>OL</sub> = 24 mA	4.5 V	0.	36		0.5		0.44	V
VOL		$I_{OL} = 50 \text{ mA}^{\dagger}$	5.5 V		-		1.65		J	v
		$I_{OL} = 75 \text{ mA}^{\dagger}$	5.5 V		-		ı		1.65	
lį	$V_I = V_{CC}$ or GND		5.5 V	±(	0.1		±1		±1	μΑ
ICC	$V_I = V_{CC}$ or GND,	IO = 0	5.5 V		8		160		80	μΑ
Δl <sub>CC</sub> ‡	$V_I = V_{CC} - 2.1 \text{ V}$		4.5 V to 5.5 V	2	2.4		3		2.8	mA
C <sub>i</sub>					10		10		10	pF

<sup>†</sup> Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C. ‡ Additional quiescent supply current per input pin, TTL inputs high, 1 unit load

#### **ACT INPUT LOAD TABLE**

INPUT	UNIT LOAD
A, B, C, or D	0.13
CLK	1
CLR, ENT	0.83
LOAD	0.67
ENP	0.5

Unit Load is  $\Delta I_{CC}$  limit specified in electrical characteristics table (e.g., 2.4 mA at 25°C).

### timing requirements over recommended operating conditions (unless otherwise noted)

			–55°C to 125°C		–40°C to 85°C		UNIT	
			MIN	MAX	MIN	MAX		
fclock	Clock frequency			80		91	MHz	
+	Pulse duration	CLK high or low	6.2		5.4		ns	
t <sub>W</sub>	r dise ddiallon	CLR low	6		5.3		115	
	Setup time, before CLK↑	A, B, C, or D	5		4.4		no	
t <sub>su</sub>	Setup time, before CEN	LOAD	6		5.3		ns	
	Hald time of the CLIVE	A, B, C, or D	0		0			
<sup>t</sup> h	Hold time, after CLK↑	ENP or ENT	0		0		ns	
t <sub>rec</sub>	Recovery time, CLR↑ before CLK↑		6		5.3		ns	

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# switching characteristics over recommended operating conditions, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

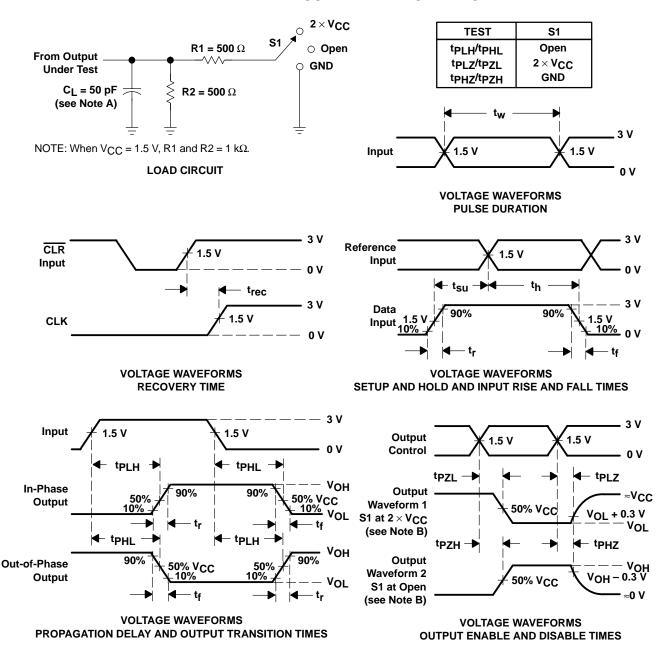
PARAMETER	FROM (INPUT)	TO (OUTPUT)	–55° 125		–40°0 85°	UNIT	
	(1141 01)	(6611 61)	MIN	MAX	MIN	MAX	
f <sub>max</sub>			80		91		MHz
	CLK	RCO	4.2	16.7	4.3	15.2	
	CER	Any Q	4.1	16.5	4.2	15	
t <sub>pd</sub>	ENT	RCO	2.7	10.8	2.8	9.8	ns
	CLR	Any Q	4.1	16.5	4.2	15	
	CLR	RCO	4.1	16.5	4.2	15	

# operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	No load	66	pF



#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>I</sub> includes probe and test-fixture capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50~\Omega$ ,  $t_f = 3$  ns,  $t_f = 3$  ns. Phase relationships between waveforms are arbitrary.
- D. For clock inputs,  $f_{\mbox{max}}$  is measured with the input duty cycle at 50%.
- E. The outputs are measured one at a time with one input transition per measurement.
- F. tpLH and tpHL are the same as tpd.
- G. tpzL and tpzH are the same as ten.
- H.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- I. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



### PACKAGE OPTION ADDENDUM

www.ti.com 15-Oct-2009

#### PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CD54ACT161F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
CD74ACT161E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74ACT161EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74ACT161M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT161M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT161M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT161M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT161ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT161MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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### TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



### \*All dimensions are nominal

Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74ACT161M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1





#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74ACT161M96	SOIC	D	16	2500	333.2	345.9	28.6

# 14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

# N (R-PDIP-T\*\*)

# PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



# D (R-PDS0-G16)

### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



# D (R-PDSO-G16)

# PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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