TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor SCHS203D

February 1998 - Revised October 2003

Features

- Fully Static Operation
- Buffered Inputs
- Common Reset
- Negative Edge Pulsing
- Fanout (Over Temperature Range)
 - Standard Outputs..... 10 LSTTL Loads
- Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: NIL = 30%, NIH = 30% of V_CC at V_CC = 5V
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)
 - CMOS Input Compatibility, IJ \leq 1µA at VOL, VOH

CD54HC4040, CD74HC4040, CD54HCT4040, CD74HCT4040

High-Speed CMOS Logic 12-Stage Binary Counter

Description

The 'HC4040 and 'HCT4040 are 14-stage ripple-carry binary counters. All counter stages are master-slave flipflops. The state of the stage advances one count on the negative clock transition of each input pulse; a high voltage level on the MR line resets all counters to their zero state. All inputs and outputs are buffered.

Ordering Information

PART NUMBER	TEMP. RANGE (^o C)	PACKAGE
CD54HC4040F3A	-55 to 125	16 Ld CERDIP
CD54HCT4040F3A	-55 to 125	16 Ld CERDIP
CD74HC4040E	-55 to 125	16 Ld PDIP
CD74HC4040M	-55 to 125	16 Ld SOIC
CD74HC4040MT	-55 to 125	16 Ld SOIC
CD74HC4040M96	-55 to 125	16 Ld SOIC
CD74HC4040NSR	-55 to 125	16 Ld SOP
CD74HCT4040E	-55 to 125	16 Ld PDIP
CD74HCT4040M	-55 to 125	16 Ld SOIC
CD74HCT4040MT	-55 to 125	16 Ld SOIC
CD74HCT4040M96	-55 to 125	16 Ld SOIC

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

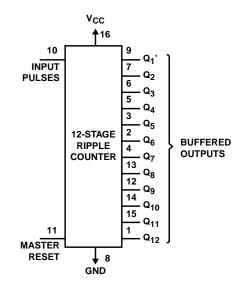
Pinout

(CE CD74 (PDIP, S CD74F (PDIP	, CD54HCT4040 RDIP) HC4040 OIC, SOP) HCT4040 P, SOIC) VIEW
Q ₁₂ 1	16 V _{CC}
Q ₆ 2	15 Q ₁₁
Q ₅ 3	14 Q ₁₀
Q ₇ 4	13 Q ₈
Q ₄ 5	12 Q ₉
Q ₃ 6	11 MR
Q ₂ 7	10 CP
GND 8	9 Q ₁ '

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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Functional Diagram



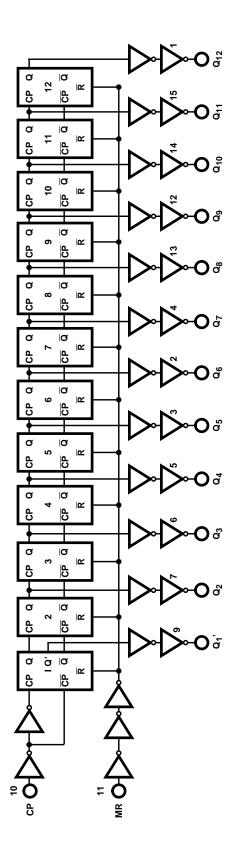
TRUTH TABLE

CP COUNT	MR	OUTPUT STATE
↑	L	No Change
\downarrow	L	Advance to Next State
Х	Н	All Outputs Are Low

H = High Voltage Level, L = Low Voltage Level, X = Don't Care,

 \uparrow = Transition from Low to High Level, \downarrow = Transition from High to Low.

Logic Diagram



Absolute Maximum Ratings

Operating Conditions

Temperature Range (T _A)55 ^o C to 125 ^o C Supply Voltage Range, V _{CC}
HC Types
HCT Types
DC Input or Output Voltage, V _I , V _O V to V _{CC}
Input Rise and Fall Time
2V
4.5V 500ns (Max)
6V

Thermal Information

Package Thermal Impedance, θ_{JA} (see Note 1):
E (PDIP) Package67 ^o C/W
M (SOIC) Package
NS (SOP) Package 64°C/W
Maximum Junction Temperature
Maximum Storage Temperature Range65°C to 150°C
Maximum Lead Temperature (Soldering 10s)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

		TES CONDIT				25 ⁰ C		-40 ⁰ C 1	го 85 ⁰ С	-55 ⁰ C T	O 125 ⁰ C	
PARAMETER SYMB	SYMBOL	V _I (V)	I _O (mA)	V _{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES					-	-						-
High Level Input	VIH	-	-	2	1.5	-	-	1.5	-	1.5	-	V
Voltage			4.5	3.15	-	-	3.15	-	3.15	-	V	
			6	4.2	-	-	4.2	-	4.2	-	V	
Low Level Input	VIL	-	-	2	-	-	0.5	-	0.5	-	0.5	V
Voltage				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output V _{OH} Y Voltage CMOS Loads	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V	
		-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V	
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output		-	-	-	-	-	-	-	-	-	V	
Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output V _{OL} V _{IH} Voltage CMOS Loads	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V	
		0.02	4.5	-	-	0.1	-	0.1	-	0.1	V	
	CIVICO LUGUS		0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output	1		-	-	-	-	-	-	-	-	-	V
Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	Ιį	V _{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	ICC	V _{CC} or GND	0	6	-	-	8	-	80	-	160	μA

CD54HC4040, CD74HC4040, CD54HCT4040, CD74HCT4040

DC Electrical Specifications (Continued)	DC Electrical S	pecifications	(Continued)
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		TEST CONDITIONS			25 ⁰ C			-40°C TO 85°C		-55°C TO 125°C		
PARAMETER SYMI	SYMBOL	V _I (V)	I _O (mA)	V _{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HCT TYPES												
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	lı	V _{CC} and GND	0	5.5	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	Icc	V _{CC} or GND	0	5.5	-	-	8	-	80	-	160	μA
Additional Quies- cent Device Current Per Input Pin: 1 Unit Load	∆I _{CC} (Note 2)	V _{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE:

2. For dual-supply systems theoretical worst case ($V_I = 2.4V$, $V_{CC} = 5.5V$) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS					
MR	0.65					
СР	0.5					

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g., 360µA max at 25°C.

Prerequisite for Switching Specifications

			25 ⁰ C		-40 ⁰ C T	О 85 ⁰ С	-55 ⁰ C T		
PARAMETER	SYMBOL	V _{CC} (V)	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES				-	-	-	-	-	_
Maximum Input Pulse Frequency	f _{MAX}	2	6	-	5	-	4	-	MHz
		4.5	30	-	25	-	20	-	MHz
		6	35	-	29	-	24	-	MHz
Input Pulse Width	t _W	2	80	-	100	-	120	-	ns
		4.5	16	-	20	-	24	-	ns
		6	14	-	17	-	20	-	ns

CD54HC4040, CD74HC4040, CD54HCT4040, CD74HCT4040

			25	°C	-4	0 ^о С ТО	85 ⁰ C	-55 ⁰	C TO 12	TO 125°C	
PARAMETER	SYMBOL	_ v _{cc} (v)	MIN	MAX	м	IN	MAX	MIN	Ν	IAX	UNITS
Reset Removal Time	^t REM	2	50	-	6	5	-	75		-	ns
		4.5	10	-	1	3	-	15		-	ns
		6	9	-	1	1	-	13		-	ns
Reset Pulse Width	t _W	2	80	-	10	00	-	120		-	ns
		4.5	16	-	2	0	-	24		-	ns
		6	14	-	1	7	-	20		-	ns
HCT TYPES											
Maximum Input Pulse Frequency	f _{MAX}	4.5	25	-	2	0	-	16		-	MHz
Input Pulse Width	t _W	4.5	20	-	2	5	-	30		-	ns
Reset Recovery Time	^t REM	4.5	10	-	1	3	-	15		-	ns
Reset Pulse Width	t _W	4.5	20	-	2	5	-	30		-	ns
Switching Specification	ons Input t _r , t	f = 6ns									
		TEST 25°C		-40 ⁰ C TO 85 ⁰ C		-55 ⁰ C TO 125 ⁰ C					
PARAMETER SYMBOL		CONDITIONS	Vcc (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES						-	-	-		-	
Propagation Delay (Figure 1)	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	140	-	175	-	210	ns
CP to Q ₁ ' Output			4.5	-	-	28	-	35	-	42	ns
		C _L =15pF	5	-	11	-	-	-	-	-	ns
		$C_L = 50 pF$	6	-	-	24	-	30	-	36	ns
Q _n to Q _n + 1	tPLH, tPHL	$C_L = 50 pF$	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
		C _L =15pF	5	-	4	-	-	-	-	-	ns
		$C_L = 50 pF$	6	-	-	13	-	16	-	19	ns
MR to Q _n	t _{PLH} , t _{PHL}	$C_L = 50 pF$	2	-	-	170	-	215	-	255	ns
			4.5	-	-	34	-	43	-	51	ns
			5	-	14	-	-	-	-	-	ns
			6	-	-	29	-	37	-	43	ns
Output Transition Time	t _{TLH} , t _{THL}	$C_L = 50 pF$	2	-	-	75	-	95	-	110	ns
(Figure 1)			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C _{IN}	$C_L = 50 pF$	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 3, 4)	C _{PD}	C _L =15pF	5	-	40	-	-	-	-	-	pF
HCT TYPES											
Propagation Delay (Figure 1)	t _{PLH} , t _{PHL}	C _L = 50pF	4.5	-	-	40	-	50	-	60	ns
CP to Q1' Output		C _L =15pF	5	-	17	. I	_	-	-	-	ns

		TEST		25 ⁰ C			-40 ^o C TO 85 ^o C		-55 ⁰ C TO 125 ⁰ C		
PARAMETER	SYMBOL		V _{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Q _n to Q _n + 1	t _{PLH} , t _{PHL}	$C_L = 50 pF$	4.5	-	-	15	-	19	-	22	ns
		C _L =15pF	5	-	4	-	-	-	-	-	ns
MR to Q _n	t _{PLH} , t _{PHL}	C _L = 50pF	4.5	-	-	40	-	50	-	60	ns
		C _L =15pF	5	-	17	-	-	-	-	-	ns
Output Transition	t _{TLH} , t _{THL}	C _L = 50pF	4.5	-	-	15	-	19	-	22	ns
Input Capacitance	C _{IN}	C _L =15pF	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 3, 4)	C _{PD}	C _L =15pF	5	-	45	-	-	-	-	-	pF

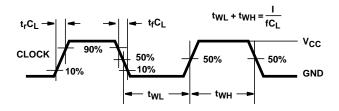
Switching Specifications Input t_r , $t_f = 6ns$ (Continued)

NOTES:

3. C_{PD} is used to determine the dynamic power consumption, per package.

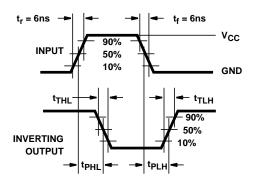
4. $P_D = V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_i/M)$ where: $M = 2^1, 2^2, 2^3, ...2^{12}, f_i =$ Input Frequency, $C_L =$ Output Load Capacitance, $V_{CC} =$ Supply Voltage.

Test Circuits and Waveforms

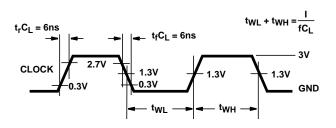


NOTE: Outputs should be switching from $10\% V_{CC}$ to $90\% V_{CC}$ in accordance with device truth table. For f_{MAX}, input duty cycle = 50%. FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND

PULSE WIDTH







NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 2. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

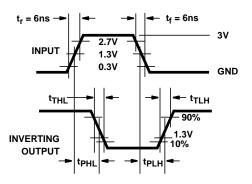
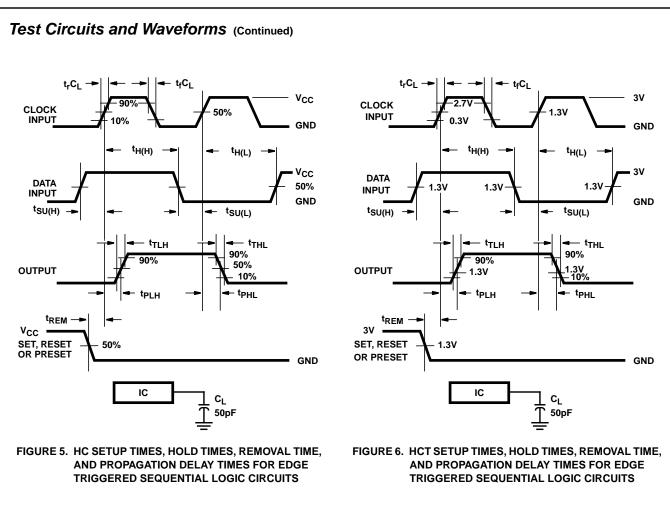


FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC





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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-8994701MEA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Call TI	
CD54HC4040F	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
CD54HC4040F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
CD54HCT4040F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
CD74HC4040E	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HC4040EE4	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HC4040M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4040M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4040M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4040M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4040ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4040MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4040MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4040MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC4040MTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT4040E	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HCT4040EE4	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HCT4040M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT4040M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT4040M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	



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Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
CD74HCT4040M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT4040ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT4040MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT4040MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT4040MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT4040MTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and pa

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE OPTION ADDENDUM



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5-Sep-2011

OTHER QUALIFIED VERSIONS OF CD54HC4040, CD54HCT4040, CD74HC4040, CD74HCT4040 :

• Catalog: CD74HC4040, CD74HCT4040

• Military: CD54HC4040, CD54HCT4040

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

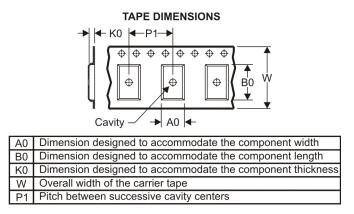
PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4040M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT4040M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

29-Jul-2009



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4040M96	SOIC	D	16	2500	333.2	345.9	28.6
CD74HCT4040M96	SOIC	D	16	2500	333.2	345.9	28.6

J (R-GDIP-T**) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



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D (R-PDSO-G16) PLASTIC SMALL OUTLINE Stencil Openings (Note D) Example Board Layout (Note C) -16x0,55 - 14x1,27 -14x1,27 16x1,95 4,80 4,80 Example Non Soldermask Defined Pad Example Pad Geometry (See Note C) 0,60 Example 2,00 Solder Mask Opening

(See Note E)

NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

← 0,07 All Around

- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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