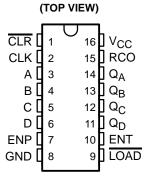
D. DB. OR N PACKAGE

SDFS056B - MARCH 1987 - REVISED AUGUST 2001

- Internal Look-Ahead Circuitry for Fast Counting
- Carry Output for N-Bit Cascading
- Fully Synchronous Operation for Counting

#### description

This synchronous, presettable, 4-bit binary counter has internal carry look-ahead circuitry for use in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when



so instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. However, counting spikes can occur on the ripple-carry (RCO) output. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of CLK.

This counter is fully programmable. That is, it can be preset to any number between 0 and 15. Because presetting is synchronous, a low logic level at the load  $(\overline{LOAD})$  input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of ENP and ENT.

The clear function is asynchronous, and a low logic level at the clear ( $\overline{\text{CLR}}$ ) input sets all four of the flip-flop outputs to low, regardless of the levels of CLK,  $\overline{\text{LOAD}}$ , ENP, and ENT.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications, without additional gating. This function is implemented by the ENP and ENT inputs and an RCO output. Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. RCO, thus enabled, produces a high-logic-level pulse while the count is 15 (HHHH). The high-logic-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

The SN74F161A features a fully independent clock circuit. Changes at ENP, ENT, or  $\overline{\text{LOAD}}$  that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the setup and hold times.

#### ORDERING INFORMATION

TA	PACKA	AGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP – N	Tube	SN74F161AN	SN74F161AN
0°C to 70°C	SOIC – D	Tube	SN74F161AD	F161A
0 0 10 70 0	30IC = D	Tape and reel	SN74F161ADR	FIOTA
	SSOP – DB	Tape and reel	SN74F161ADBR	F161A

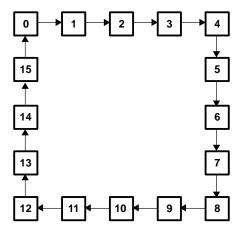
<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



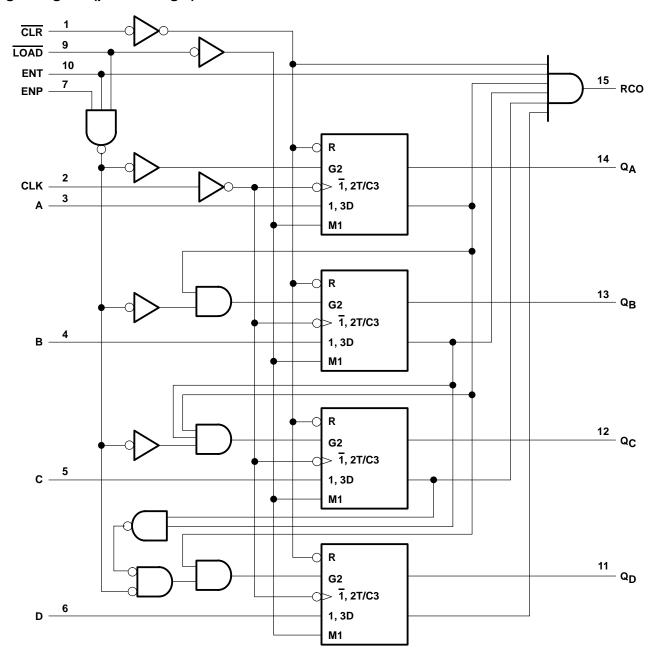
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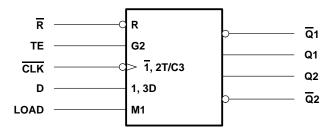
## state diagram



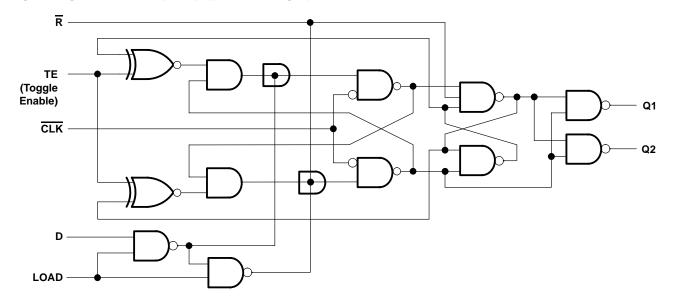
# logic diagram (positive logic)



## logic symbol, each flip-flop



## logic diagram, each flip-flop (positive logic)

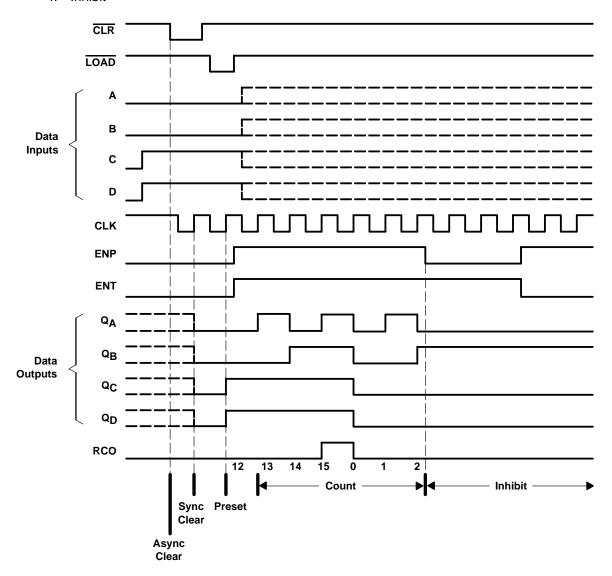




## typical clear, preset, count, and inhibit sequences

The following timing sequence is illustrated below:

- 1. Clear outputs to zero
- 2. Preset to binary 12
- 3. Count to 13, 14, 15, 0, 1, and 2
- 4. Inhibit



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V <sub>CC</sub>		0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)		
Input current range		30 mA to 5 mA
Voltage range applied to any output in the high	state	0.5 V to V <sub>CC</sub>
Current into any output in the low state		
Package thermal impedance, θ <sub>JA</sub> (see Note 2)		
-	DB package	82°C/W
	N package	67°C/W
Storage temperature range, T <sub>stg</sub>		65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	V
VIH	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
lıK	Input clamp current			-18	mA
ЮН	High-level output current			-1	mA
lOL	Low-level output current			20	mA
TA	Operating free-air temperature	0		70	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TE	ST CONDITIONS	MIN	TYP‡	MAX	UNIT
٧ıK		$V_{CC} = 4.5 \text{ V},$	$I_{I} = -18 \text{ mA}$			-1.2	V
V		$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -1 \text{ mA}$	2.5	3.4		V
VOH		$V_{CC} = 4.75 \text{ V},$	$I_{OH} = -1 \text{ mA}$	2.7			V
VOL		$V_{CC} = 4.5 \text{ V},$	$I_{OL} = 20 \text{ mA}$		0.3	0.5	V
II		$V_{CC} = 5.5 \text{ V},$	V <sub>I</sub> = 7 V			0.1	mA
lн		$V_{CC} = 5.5 V,$	V <sub>I</sub> = 2.7 V			20	μΑ
	ENP, CLK, A, B, C, D					- 0.6	
Ι <sub>Ι</sub> L	ENT, LOAD	$V_{CC} = 5.5 V$ ,	$V_{I} = 0.5 V$			- 1.2	mA
	CLR					- 0.6	
los§		$V_{CC} = 5.5 V$ ,	V <sub>O</sub> = 0	-60		-150	mA
Icc		V <sub>CC</sub> = 5.5 V			37	55	mA

<sup>‡</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.



NOTES: 1. The input voltage ratings may be exceeded provided the input current ratings are observed.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

<sup>§</sup> Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				V <sub>CC</sub> =	= 5 V, 25°C	MIN	MAX	UNIT
				MIN	MAX			
fclock	Clock frequency			0	100	0	90	MHz
		CLK high or low (loading)		5		5		
t <sub>W</sub> Pulse duration	Pulse duration	CLK (counting)	High	4		4		ns
	ruise uuralion	CER (counting)	Low	6		7		115
		CLR low		5		5		
		Data before CLK↑	High or low	5		5		
		LOAD before CLK↑	High	11		11.5		ns
t <sub>su</sub>	Setup time	LOAD before CLK	Low	8.5		9.5		
		ENP and ENT before CLK↑	High	11		11.5		
		ENP and ENT before CLK	Low	5		5		
		Data after CLK↑	High or low	2		2		
ļ.	Hold time	LOAD after OLK	High	2		2		200
<sup>t</sup> h	Hold time	LOAD aπer CLK	LOAD after CLK↑			0		ns
		ENP and ENT after CLK↑	High or low	0		0		
t <sub>su</sub>	Inactive-state setup time, C	LR high before CLK↑†		6		6		ns

<sup>†</sup> Inactive-state setup time also is referred to as recovery time.

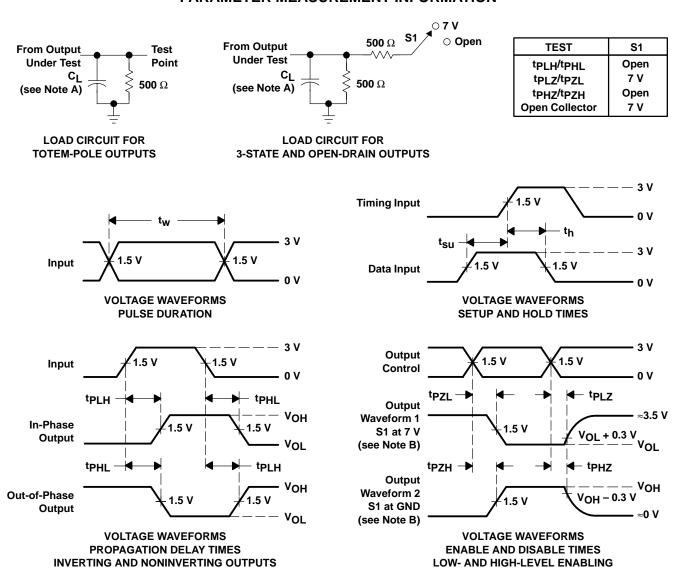
## switching characteristics (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$ = 5 V, $C_L$ = 50 PF, $R_L$ = 500 $\Omega$ , $T_A$ = 25°C			V <sub>CC</sub> = 4.5 V C <sub>L</sub> = 50 R <sub>L</sub> = 50 T <sub>A</sub> = MIN TC	UNIT	
			MIN	TYP	MAX	MIN	MAX	
f <sub>max</sub>			100	120		90		MHz
t <sub>PLH</sub>	OLK (LOAD bimb)	A O	2.7	5.1	7.5	2.7	8.5	no
t <sub>PHL</sub>	CLK (LOAD high)	Any Q	2.7	7.1	10	2.7	11	ns
t <sub>PLH</sub>	CLK (I OAD law)	A O	3.2	5.6	8.5	3.2	9.5	ns
<sup>t</sup> PHL	CLK (LOAD low)	Any Q	3.2	5.6	8.5	3.2	9.5	115
<sup>t</sup> PLH	CLK	DCO	4.2	9.6	14	4.2	15	ns
<sup>t</sup> PHL	CLK	RCO	4.2	9.6	14	4.2	15	115
<sup>t</sup> PLH	FNT	DCO	1.7	4.1	7.5	1.7	8.5	no
<sup>t</sup> PHL	ENT	RCO	1.7	4.1	7.5	1.7	8.5	ns
4	OL D	Any Q	4.7	8.6	12	4.7	13	
<sup>t</sup> PHL	CLR	RCO	3.7	7.6	10.5	3.7	11.5	ns

<sup>‡</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. NOTE 4: Load circuits and waveforms are shown in Figure 1.



#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_f \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ , duty cycle = 50%.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



#### PACKAGE OPTION ADDENDUM

www.ti.com 11-Nov-2009

#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74F161AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74F161ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74F161ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74F161ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74F161ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74F161ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74F161AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74F161AN3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74F161ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74F161ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74F161ANSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74F161ANSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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# **PACKAGE OPTION ADDENDUM**

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## PACKAGE MATERIALS INFORMATION

29-Jul-2009 www.ti.com

## TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F161ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74F161ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

**PACKAGE MATERIALS INFORMATION** 

www.ti.com 29-Jul-2009



#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F161ADR	SOIC	D	16	2500	333.2	345.9	28.6
SN74F161ANSR	SO	NS	16	2000	346.0	346.0	33.0

# N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



# D (R-PDS0-G16)

## PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



# D (R-PDSO-G16)

# PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



## **MECHANICAL DATA**

## NS (R-PDSO-G\*\*)

# 14-PINS SHOWN

#### PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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