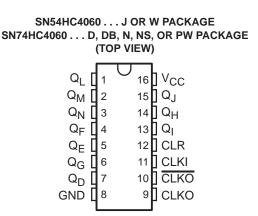
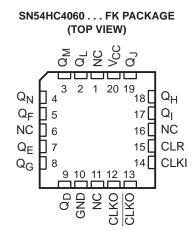
- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80-μA Max I<sub>CC</sub>
- Typical t<sub>pd</sub> = 14 ns



- SCLS161D DECEMBER 1982 REVISED SEPTEMBER 2003
- $\pm$ 4-mA Output Drive at 5 V
- Low Input Current of 1 µA Max
- Allow Design of Either RC- or Crystal-Oscillator Circuits



NC - No internal connection

#### description/ordering information

The 'HC4060 devices consist of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC- or crystal-oscillator circuits. A high-to-low transition on the clock (CLKI) input increments the counter. A high level at the clear (CLR) input disables the oscillator (CLKO goes high and CLKO goes low) and resets the counter to zero (all Q outputs low).

TA	PACKA	GE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP – N	Tube of 25	SN74HC4060N	SN74HC4060N
		Tube of 40	SN74HC4060D	
	SOIC – D	Reel of 2500	SN74HC4060DR	HC4060
		Reel of 250	SN74HC4060DT	
–40°C to 85°C	SOP – NS	Reel of 2000	SN74HC4060NSR	HC4060
	SSOP – DB	Reel of 2000	SN74HC4060DBR	HC4060
		Tube of 90	SN74HC4060PW	
	TSSOP – PW	Reel of 2000	SN74HC4060PWR	HC4060
		Reel of 250	SN74HC4060PWT	
	CDIP – J	Tube of 25	SNJ54HC4060J	SNJ54HC4060J
–55°C to 125°C	CFP – W	Tube of 150	SNJ54HC4060W	SNJ54HC4060W
	LCCC – FK	Tube of 55	SNJ54HC4060FK	SNJ54HC4060FK

#### ORDERING INFORMATION

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

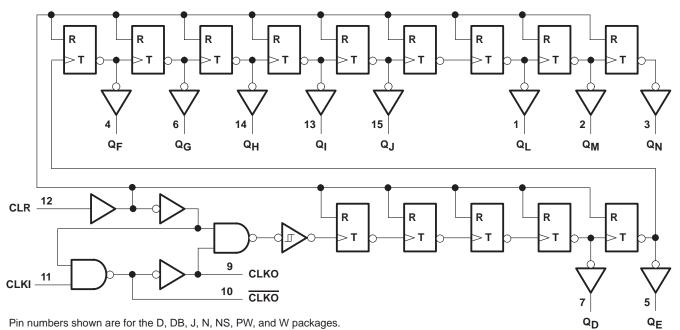


Copyright i 2003, Texas Instruments Incorporated On products compliant to MIL-PRF-3853, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SCLS161D - DECEMBER 1982 - REVISED SEPTEMBER 2003

	FUNCTION TABLE (each buffer)											
INPUTS FUNCTION												
CLK	CLR	FUNCTION										
<b>↑</b>	L	No change										
$\downarrow$	L	Advance to next stage										
Х	Н	All outputs L										

## logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

	20 mA 20 mA 25 mA 3°C/W 2°C/W 7°C/W 4°C/W
PW package	

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.



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### recommended operating conditions (see Note 3)

			SN	54HC40	60	SN	74HC40	60	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage		2	5	6	2	5	6	V
		V <sub>CC</sub> = 2 V	1.5			1.5			
VIH	High-level input voltage	V <sub>CC</sub> = 4.5 V	3.15			3.15			V
		$V_{CC} = 6 V$	4.2			4.2			
		V <sub>CC</sub> = 2 V			0.5			0.5	
VIL Low-level input voltage	Low-level input voltage	V <sub>CC</sub> = 4.5 V			1.35			1.35	V
		V <sub>CC</sub> = 6 V			1.8			1.8	
VI	Input voltage		0		VCC	0		VCC	V
VO	Output voltage		0		VCC	0		VCC	V
		V <sub>CC</sub> = 2 V			1000			1000	
$\Delta t / \Delta v$	Input transition rise/fall time	V <sub>CC</sub> = 4.5 V			500			500	ns
		V <sub>CC</sub> = 6 V			400			400	
TA	Operating free-air temperature	·	-55		125	-40		85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		7507.00			Т	A = 25°C	;	SN54H	C4060	SN74H	C4060	
PAR	AMETER	TEST CO	NDITIONS	Vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
				2 V	1.9	1.998		1.9		1.9		
	All outputs	$V_{I} = V_{IH} \text{ or } V_{IL},$	l <sub>OH</sub> = -20 μA	4.5 V	4.4	4.499		4.4		4.4		
VOH				6 V	5.9	5.999		5.9		5.9		V
	O austrausta		$I_{OH} = -4 \text{ mA}$	4.5 V	3.98	4.3		3.7		3.84		
	Q outputs	$V_I = V_{IH} \text{ or } V_{IL}$	I <sub>OH</sub> = -5.2 mA	6 V	5.48	5.8		5.2		5.34		
				2 V		0.002	0.1		0.1		0.1	
	All outputs	$V_{I} = V_{IH} \text{ or } V_{IL},$	l <sub>OL</sub> = 20 μA	4.5 V		0.001	0.1		0.1		0.1	
VOL				6 V		0.001	0.1		0.1		0.1	V
	O austrausta		$I_{OL} = 4 \text{ mA}$	4.5 V		0.17	0.26		0.4		0.33	
	Q outputs	$V_I = V_{IH} \text{ or } V_{IL}$	I <sub>OL</sub> = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
Ц		$V_{I} = V_{CC} \text{ or } 0$		6 V		±0.1	±100		±1000		±1000	nA
ICC		$V_I = V_{CC} \text{ or } 0,$	IO = 0	6 V			8		160		80	μΑ
Ci				2 V to 6 V		3	10		10		10	pF



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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

				T <sub>A</sub> =	25°C	SN54H	C4060	SN74H	C4060	
			VCC	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V		5.5		3.7		4.3	
fclock	Clock frequency		4.5 V		28		19		22	MHz
			6 V		33		22		25	
			2 V	90		135		115		
		CLKI high or low	4.5 V	18		27		23		
	Dulas duration		6 V	15		23		20		
tw	Pulse duration		2 V	90		135		115		ns
		CLR high	4.5 V	18		27		23		
			6 V	15		23		20		
			2 V	160		240		200		
t <sub>su</sub>	$t_{su}$ Setup time, CLR inactive before CLKI $\downarrow$		4.5 V	32		48		40		ns
			6 V	27		41		34		

# switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

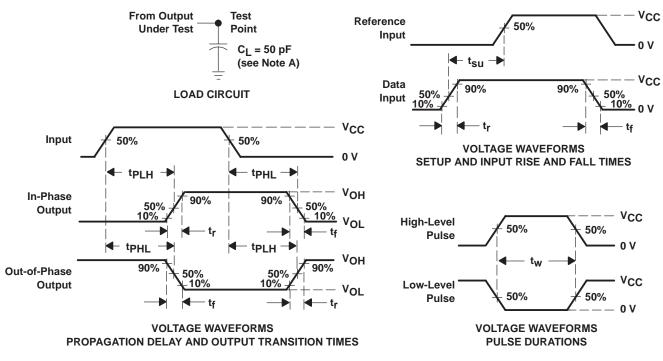
	FROM	то		Т	ן = 25°C	;	SN54H	C4060	SN74H	C4060	
PARAMETER	(INPUT)	(OUTPUT)	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V	5.5	10		3.7		4.3		
fmax			4.5 V	28	45		19		22		MHz
			6 V	33	53		22		25		
			2 V		240	490		735		615	
<sup>t</sup> pd	CLKI	QD	4.5 V		58	98		147		123	ns
			6 V		42	83		125		105	
			2 V		66	140		210		175	
<sup>t</sup> PHL	CLR	Any Q	4.5 V		18	28		42		35	ns
			6 V		14	24		36		30	
			2 V		28	75		110		95	
t	tt	Any	4.5 V		8	15		22		19	ns
			6 V		6	30		19		16	

## operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	TYP	UNIT
Cpd	Power dissipation capacitance	No load	88	pF



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### PARAMETER MEASUREMENT INFORMATION

- NOTES: A. C<sub>L</sub> includes probe and test-fixture capacitance.
  - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz, Z<sub>Q</sub> = 50  $\Omega$ , t<sub>f</sub> = 6 ns, t<sub>f</sub> = 6 ns.
  - C. For clock inputs, fmax is measured when the input duty cycle is 50%.
  - D. The outputs are measured one at a time with one input transition per measurement.
  - E. tPLH and tPHL are the same as tpd.

#### Figure 1. Load Circuit and Voltage Waveforms

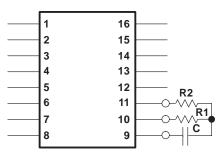


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## CONNECTING AN RC-OSCILLATOR CIRCUIT TO THE 'HC4060 DEVICES

The 'HC4060 devices consist of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC- or crystal-oscillator circuits.

When an RC-oscillator circuit is implemented, two resistors and a capacitor are required. The components are attached to the terminals as shown:



To determine the values of capacitance and resistance necessary to obtain a specific oscillator frequency (f), use this formula:

$$f = \frac{1}{2(R1)(C)\left(\frac{0.405 R2}{R1 + R2} + 0.693\right)}$$

If R2 > > R1 (i.e., R2 = 10R1), the above formula simplifies to:

$$f = \frac{0.455}{RC}$$



18-Sep-2008

#### **PACKAGING INFORMATION**

TEXAS INSTRUMENTS www.ti.com

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN54HC4060FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SN74HC4060D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4060DBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4060DBRE4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4060DBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4060DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4060DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4060DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4060DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4060DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4060DT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4060DTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4060DTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4060N	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74HC4060NE4	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74HC4060NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4060NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4060NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4060PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4060PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4060PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4060PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4060PWRE4	ACTIVE	TSSOP	PW	16	2000	,	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4060PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4060PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM



Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74HC4060PWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4060PWTG4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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# PACKAGE MATERIALS INFORMATION

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#### TAPE AND REEL INFORMATION

#### REEL DIMENSIONS

Texas Instruments





TAPE AND REEL INFORMATION

#### TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

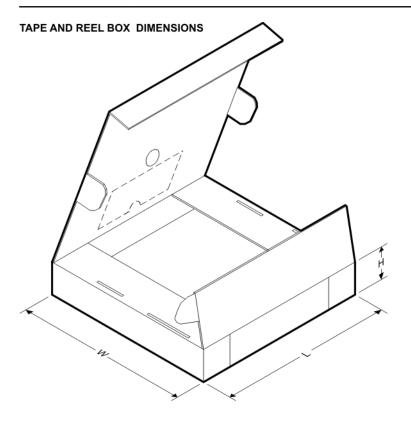
All dimensions are nominal								-		-		
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC4060DBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74HC4060DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC4060NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74HC4060PWR	TSSOP	PW	16	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
SN74HC4060PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC4060PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC4060PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TEXAS INSTRUMENTS

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# PACKAGE MATERIALS INFORMATION

26-Jun-2012



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC4060DBR	SSOP	DB	16	2000	346.0	346.0	33.0
SN74HC4060DR	SOIC	D	16	2500	346.0	346.0	33.0
SN74HC4060NSR	SO	NS	16	2000	346.0	346.0	33.0
SN74HC4060PWR	TSSOP	PW	16	2000	364.0	364.0	27.0
SN74HC4060PWR	TSSOP	PW	16	2000	346.0	346.0	29.0
SN74HC4060PWRG4	TSSOP	PW	16	2000	346.0	346.0	29.0
SN74HC4060PWT	TSSOP	PW	16	250	346.0	346.0	29.0

LEADLESS CERAMIC CHIP CARRIER

FK (S-CQCC-N\*\*) 28 TERMINAL SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



# N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- $\triangle$  The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



4211283-4/D 06/11

# D (R-PDSO-G16) PLASTIC SMALL OUTLINE Stencil Openings (Note D) Example Board Layout (Note C) -16x0,55 - 14x1,27 -14x1,27 16x1,95 4,80 4,80 Example Non Soldermask Defined Pad Example Pad Geometry (See Note C) 0,60 Example 2,00 Solder Mask Opening

(See Note E)

NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

← 0,07 All Around

- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.  $\beta$ . This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153



## LAND PATTERN DATA



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



## MECHANICAL DATA

#### PLASTIC SMALL-OUTLINE PACKAGE

#### 0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 $\bigcirc$ Gage Plane ₽ 0,25 7 1 1,05 0,55 0°-10° Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS \*\* 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G\*\*)

**14-PINS SHOWN** 

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



# **MECHANICAL DATA**

MSSO002E - JANUARY 1995 - REVISED DECEMBER 2001

## DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150



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