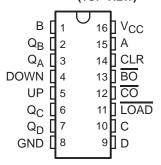
- DECEMBER 1982 - REVISED OCTOBER 200

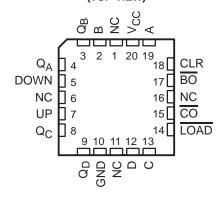
- Wide Operating Voltage Range of 2 V to 6 V
- **Outputs Can Drive Up To 10 LSTTL Loads**
- Low Power Consumption, 80-µA Max ICC
- Typical  $t_{nd} = 20 \text{ ns}$
- ±4-mA Output Drive at 5 V
- Low Input Current of 1 µA Max

SN54HC193 . . . J OR W PACKAGE SN74HC193...D, N, NS, OR PW PACKAGE (TOP VIEW)



- **Look-Ahead Circuitry Enhances Cascaded** Counters
- **Fully Synchronous in Count Modes**
- Parallel Asynchronous Load for Modulo-N **Count Lengths**
- **Asynchronous Clear**

SN54HC193 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

#### description/ordering information

'HC193 devices 4-bit synchronous, reversible, up/down binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

#### ORDERING INFORMATION

TA	PACKA	GE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING		
	PDIP – N	Tube of 25	SN74HC193N	SN74HC193N		
		Tube of 40 SN74HC193D				
	SOIC - D	Reel of 2500	SN74HC193DR	HC193		
4000 1- 0500		Reel of 250	SN74HC193DT			
-40°C to 85°C	SOP - NS	Reel of 2000	SN74HC193NSR	HC193		
		Tube of 90	SN74HC193PW			
	TSSOP - PW	Reel of 2000	SN74HC193PWR	HC193		
		Reel of 250	SN74HC193PWT			
	CDIP – J	Tube of 25	SNJ54HC193J	SNJ54HC193J		
−55°C to 125°C	CFP – W	Tube of 150	SNJ54HC193W	SNJ54HC193W		
	LCCC - FK	Tube of 55	SNJ54HC193FK	SNJ54HC193FK		

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



### SN54HC193, SN74HC193 4-BIT SYNCHRONOUS UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

SCLS122D - DECEMBER 1982 - REVISED OCTOBER 2003

#### description/ordering information (continued)

The outputs of the four flip-flops are triggered on a low-to-high-level transition of either count (clock) input (UP or DOWN). The direction of counting is determined by which count input is pulsed while the other count input is high.

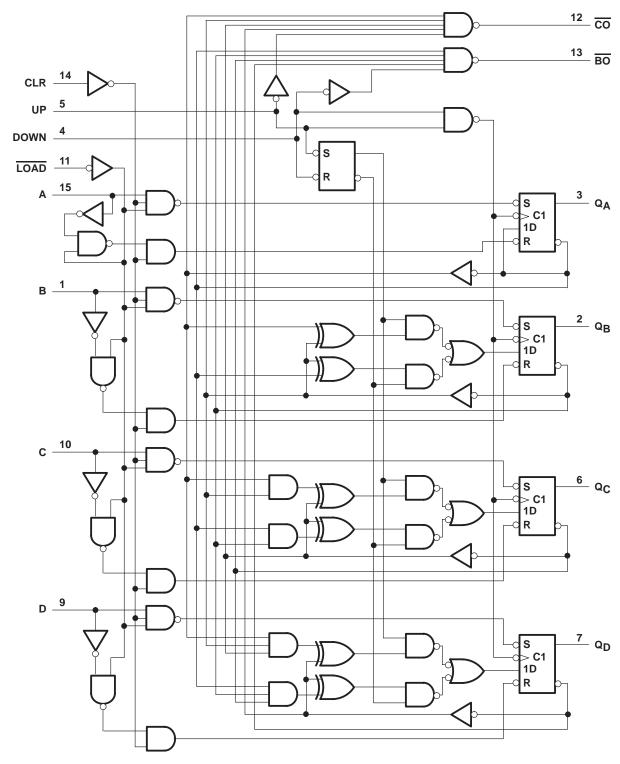
All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load (LOAD) input and entering the desired data at the data inputs. The output changes to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers simply by modifying the count length with the preset inputs.

A clear (CLR) input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and LOAD inputs.

These counters were designed to be cascaded without the need for external circuitry. The borrow  $(\overline{BO})$  output produces a low-level pulse while the count is zero (all outputs low) and DOWN is low. Similarly, the carry  $(\overline{CO})$  output produces a low-level pulse while the count is maximum (9 or 15), and UP is low. The counters then can be cascaded easily by feeding  $\overline{BO}$  and  $\overline{CO}$  to DOWN and UP, respectively, of the succeeding counter.



#### logic diagram (positive logic)



Pin numbers shown are for the D, J, N, NS, PW, and W packages.

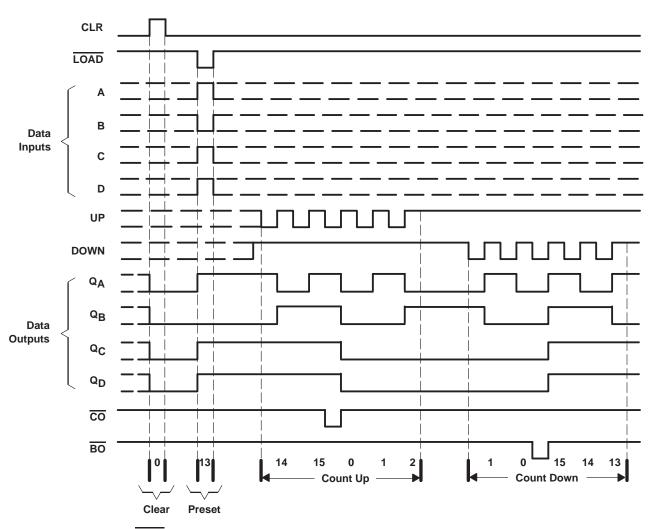


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#### typical clear, load, and count sequence

The following sequence is illustrated below:

- 1. Clear outputs to 0
- 2. Load (preset) to binary 13
- 3. Count up to 14, 15, carry, 0, 1, and 2
- 4. Count down to 1, 0, borrow, 15, 14, and 13



NOTES: A. CLR overrides LOAD, data, and count inputs.

B. When counting up, count-down input must be high; when counting down, count-up input must be high.



## SN54HC193, SN74HC193 4-BIT SYNCHRONOUS UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR) SCLS122D - DECEMBER 1982 - REVISED OCTOBER 2003

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V <sub>CC</sub>		–0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see	ee Note 1)	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CO}$	C) (see Note 1)	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	-	±25 mA
Continuous current through V <sub>CC</sub> or GND		±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	: D package	73°C/W
	N package	67°C/W
	NS package	64°C/W
	PW package	108°C/W
Storage temperature range, T <sub>Stg</sub>		–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 3)

			SN	154HC19	)3	SN	174HC19	3	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		2	5	6	2	5	6	V
		V <sub>CC</sub> = 2 V	1.5			1.5			
ViH	High-level input voltage	V <sub>CC</sub> = 4.5 V	3.15			3.15			V
		VCC = 6 V	4.2			4.2			
		V <sub>CC</sub> = 2 V			0.5			0.5	
VIL	Low-level input voltage	V <sub>CC</sub> = 4.5 V			1.35			1.35	V
		V <sub>CC</sub> = 6 V			1.8			1.8	
VI	Input voltage		0		VCC	0		VCC	V
VO	Output voltage		0		VCC	0		VCC	V
		V <sub>CC</sub> = 2 V			1000			1000	
Δt/Δv‡	Input transition rise/fall time	V <sub>CC</sub> = 4.5 V			500			500	ns
		V <sub>CC</sub> = 6 V			400			400	
TA	Operating free-air temperature		-55		125	-40		85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

<sup>‡</sup> If this device is used in the threshold region (from V<sub>IL</sub>max = 0.5 V to V<sub>IH</sub>min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t<sub>t</sub> = 1000 ns and V<sub>CC</sub> = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

# SN54HC193, SN74HC193 4-BIT SYNCHRONOUS UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR) SCLS122D - DECEMBER 1982 - REVISED OCTOBER 2003

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

242445752	7507.00	NIDITIONS	.,	Т	A = 25°C	;	SN54H	C193	SN74H	IC193	
PARAMETER	TEST CC	ONDITIONS	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V	1.9	1.998		1.9		1.9		
		$I_{OH} = -20  \mu A$	4.5 V	4.4	4.499		4.4		4.4		
∨он	VI = VIH or VIL		6 V	5.9	5.999		5.9		5.9		V
		$I_{OH} = -4 \text{ mA}$	4.5 V	3.98	4.3		3.7		3.84		
		$I_{OH} = -5.2 \text{ mA}$	6 V	5.48	5.8		5.2		5.34		
			2 V		0.002	0.1		0.1		0.1	
		$I_{OL} = 20 \mu A$	4.5 V		0.001	0.1		0.1		0.1	
VOL	VI = VIH or VIL		6 V		0.001	0.1		0.1		0.1	V
		I <sub>OL</sub> = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I <sub>OL</sub> = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
lį	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000	nA
Icc	$V_I = V_{CC}$ or 0,	IO = 0	6 V			8		160		80	μΑ
Ci			2 V to 6 V		3	10		10		10	pF

#### timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			Ι.,	T <sub>A</sub> =	25°C	SN54H	IC193	SN74H	C193	
			vcc	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V		4.2		2.8		3.3	
fclock	Clock frequency		4.5 V		21		14		17	MHz
			6 V		24		16		19	
			2 V	120		180		150		
		CLR high	4.5 V	24		36		30		
			6 V	21		31		26		
			2 V	120		180		150		
$t_{W}$	Pulse duration	LOAD low	4.5 V	24		36		30		ns
			6 V	21		31		26		
			2 V	120		180		150		
		UP or DOWN high or low	4.5 V	24		36		30		
			6 V	21		31		26		
			2 V	110		165		140		
		Data before LOAD inactive	4.5 V	22		33		28		
			6 V	19		28		24		
			2 V	110		165		140		
t <sub>su</sub>	Setup time	CLR inactive before UP↑ or DOWN↑	4.5 V	22		33		28		ns
			6 V	19		28		24		
			2 V	110		165		140		
		LOAD inactive before UP↑ or DOWN↑	4.5 V	22		33		28		
			6 V	19		28		24		
			2 V	5		5		5		_
th	Hold time	Data after LOAD inactive	4.5 V	5		5		5		ns
			6 V	5		5		5		



# SN54HC193, SN74HC193 4-BIT SYNCHRONOUS UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR) SCLS122D - DECEMBER 1982 - REVISED OCTOBER 2003

# switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

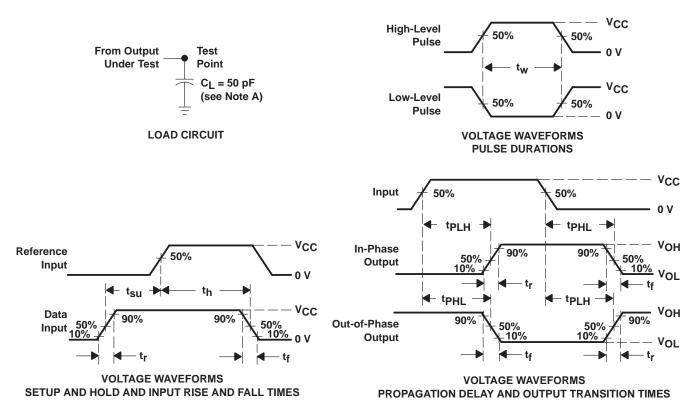
24244555	FROM	то	,,	T,	Δ = 25°C	;	SN54F	IC193	SN74F	IC193	
PARAMETER	(INPUT)	(OUTPUT)	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V	4.2	8		2.8		3.3		
f <sub>max</sub>			4.5 V	21	55		14		17		MHz
			6 V	24	60		16		19		
			2 V		75	165		250		205	
	UP	CO	4.5 V		24	33		50		41	
			6 V		20	28		43		35	
			2 V		75	165		250		205	
	DOWN	BO	4.5 V		24	33		50		41	
			6 V		20	28		43		35	
<sup>t</sup> pd			2 V		190	250		375		315	ns
	UP or DOWN	Any Q	4.5 V		40	50		75		63	
			6 V		35	43		64		54	
			2 V		190	260		390		325	
	LOAD	Any Q	4.5 V		40	52		78		65	
			6 V		35	44		66		55	
			2 V		170	240		360		300	
tPHL	CLR	Any Q	4.5 V		36	48		72		60	ns
			6 V		31	41		61		51	
			2 V		38	75		110		95	
t <sub>t</sub>		Any	4.5 V		8	15		22		19	ns
			6 V		6	13		19		16	

# operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	No load	50	pF

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#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>I</sub> includes probe and test-fixture capacitance.

- B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \ \Omega$ ,  $t_f = 6 \ ns$ ,  $t_f = 6 \ ns$ .
- C. For clock inputs,  $f_{\text{max}}$  is measured when the input duty cycle is 50%.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



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#### **PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
5962-87724012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-8772401EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Call TI	
SN54HC193J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SN74HC193D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC193DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC193DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC193DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC193DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC193DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC193DT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC193DTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC193DTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC193N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74HC193NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74HC193NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC193NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC193NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC193PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC193PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	





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Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN74HC193PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC193PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC193PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC193PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC193PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC193PWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC193PWTG4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SNJ54HC193FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54HC193J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### **PACKAGE OPTION ADDENDUM**

5-Sep-2011

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF SN54HC193, SN74HC193:

Catalog: SN74HC193

Automotive: SN74HC193-Q1, SN74HC193-Q1

• Military: SN54HC193

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military QML certified for Military and Defense Applications

### PACKAGE MATERIALS INFORMATION

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#### TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

All differsions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC193DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC193NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74HC193PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC193PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

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\*All dimensions are nominal

7 til dillionsions are nominal							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC193DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74HC193NSR	SO	NS	16	2000	346.0	346.0	33.0
SN74HC193PWR	TSSOP	PW	16	2000	346.0	346.0	29.0
SN74HC193PWT	TSSOP	PW	16	250	346.0	346.0	29.0

#### 14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## FK (S-CQCC-N\*\*)

### LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



## N (R-PDIP-T\*\*)

### PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



## D (R-PDS0-G16)

#### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



# D (R-PDSO-G16)

## PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G16)

#### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



# PW (R-PDSO-G16)

## PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



#### **MECHANICAL DATA**

### NS (R-PDSO-G\*\*)

# 14-PINS SHOWN

#### PLASTIC SMALL-OUTLINE PACKAGE



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- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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