SDAS210C - DECEMBER 1982 - REVISED JULY 1996

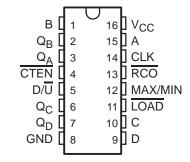
- Single Down/Up Count-Control Line
- Look-Ahead Circuitry Enhances Speed of Cascaded Counters
- Fully Synchronous in Count Modes
- Asynchronously Presettable With Load Control
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

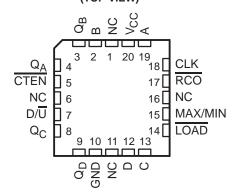
The 'ALS191A are synchronous 4-bit reversible up/down binary counters. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock (CLK) input if the count enable (\overline{CTEN}) input is low. A high at \overline{CTEN} inhibits counting. The direction of the count is determined by the level of the down/up (D/ \overline{U}) input. When D/ \overline{U} is low, the counter counts up, and when D/ \overline{U} is high, the counter counts down.

SN54ALS191A . . . J PACKAGE SN74ALS191A . . . D OR N PACKAGE (TOP VIEW)



SN54ALS191A . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

These counters feature a fully independent clock circuit. Changes at the control inputs ($\overline{\text{CTEN}}$ and $\overline{\text{D/U}}$) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter is dictated solely by the conditions meeting the stable setup and hold times.

These counters are fully programmable. Each output can be preset to either level by placing a low on the $\overline{\text{LOAD}}$ input and entering the desired data at the data inputs. The output changes to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

CLK, D/\overline{U} , and \overline{LOAD} are buffered to lower the drive requirement, which significantly reduces the loading on (current required by) clock drivers, for long parallel words.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



SN54ALS191A, SN74ALS191A SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS

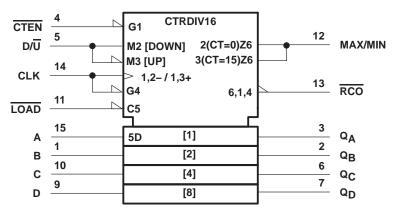
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description (continued)

Two outputs are available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is minimum (0) counting down or maximum (15) counting up. The ripple-clock output (\overline{RCO}) produces a low-level output pulse under those same conditions, but only while the clock input is low. The counter easily can be cascaded by feeding the ripple-clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count (MAX/MIN) output can be used to accomplish look ahead for high-speed operation.

The SN54ALS191A is characterized for operation over the full military temperature range of -55° C to 125° C. The SN74ALS191A is characterized for operation from 0° C to 70° C.

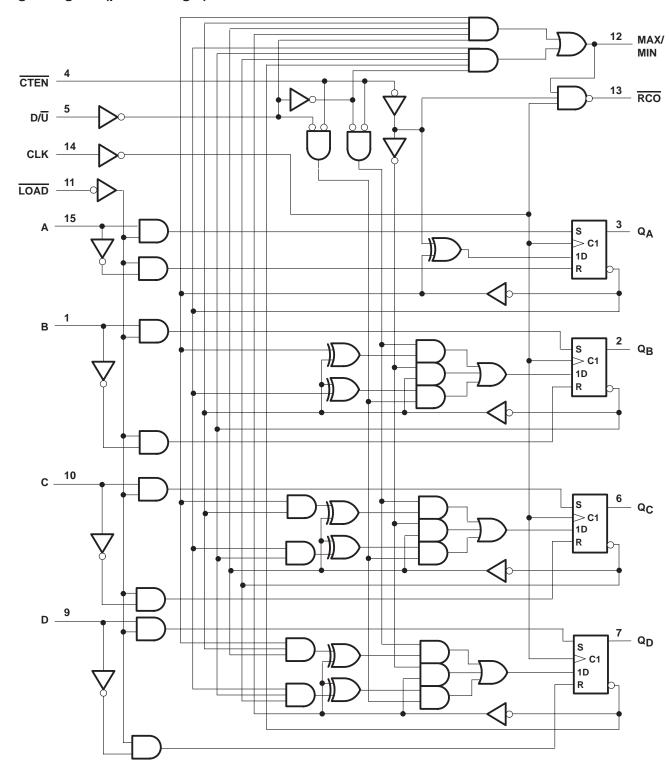
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, and N packages.



logic diagram (positive logic)



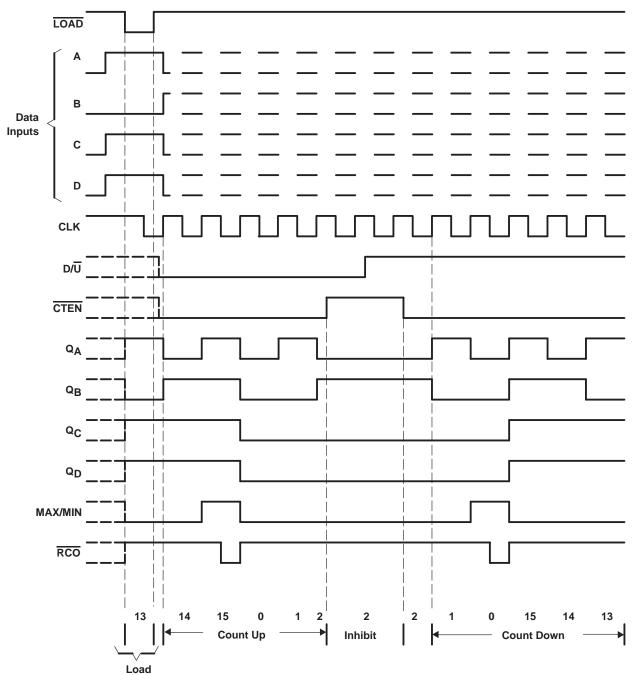
Pin numbers shown are for the D, J, and N packages.

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typical load, count, and inhibit sequences

The following sequence is illustrated below:

- 1. Load (preset) to binary 13
- 2. Count up to 14, 15 (maximum), 0, 1, and 2
- 3. Inhibit
- 4. Count down to 1, 0 (minimum), 15, 14, and 13





SN54ALS191A, SN74ALS191A SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS

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absolute maximum ratings over operating free-air temperature range (unless of	herwise noted)†
Supply voltage, V _{CC}	7 V
Input voltage, V _I	7 V
Operating free-air temperature range, T _A : SN54ALS191A	55°C to 125°C
SN74ALS191A	0°C to 70°C
Storage temperature range, T _{stg}	–65°C to 150°C

recommended operating conditions

			SN	SN54ALS191A			SN74ALS191A			
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
VCC	Supply voltage		4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage		2			2			V	
V_{IL}	Low-level input voltage				0.7			0.8	V	
IOH	High-level output current				-0.4			-0.4	mA	
lOL	Low-level output current				4			8	mA	
fclock	Clock frequency		0		20	0		30	MHz	
	Pulse duration	CLK high or low	20			16.5				
t _W		LOAD low	25			20			ns	
		Data before LOAD↑	25			20				
١.	Outros times	CTEN before CLK↑	45			20			7	
t _{su}	Setup time	D/U before CLK↑	30			20			ns	
		LOAD inactive before CLK↑	20			20				
		Data after LOAD↑	5			5				
t _h	Hold time	CTEN after CLK↑	0			0			ns	
		D/U after CLK↑	0			0				
TA	Operating free-air temperature		-55		125	0		70	°C	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SN54ALS191A, SN74ALS191A SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		SN54ALS1	91A	SN7					
PARAMETER	TEST CON	MIN TYPT	MAX	MIN	TYP†	MAX	UNIT		
VIK	V _{CC} = 4.5 V,	$I_1 = -18 \text{ mA}$		-1.5			-1.5	V	
VOH	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} - 2		V _{CC} - 2	<u>)</u>			
Mari	V 45V	I _{OL} = 4 mA	0.25	0.4		0.25	0.4	V	
VOL	V _{CC} = 4.5 V	$I_{OL} = 8 \text{ mA}$			0.35		0.5		
IĮ	$V_{CC} = 5.5 V,$	V _I = 7 V		0.2			0.1	mA	
liH	$V_{CC} = 5.5 V,$	V _I = 2.7 V		20			20	μΑ	
CTEN or CLK	V 55V	V 04V		-0.2			-0.2	A	
I _{IL} All others	$V_{CC} = 5.5 \text{ V},$	$V_{ } = 0.4 \text{ V}$		-0.2			-0.1	mA	
10 [‡]	V _{CC} = 5.5 V,	V _O = 2.25 V	-20	-112	-30		- 112	mA	
Icc	V _{CC} = 5.5 V,	All inputs at 0	12	22		12	22	mA	

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics (see Figure 1)

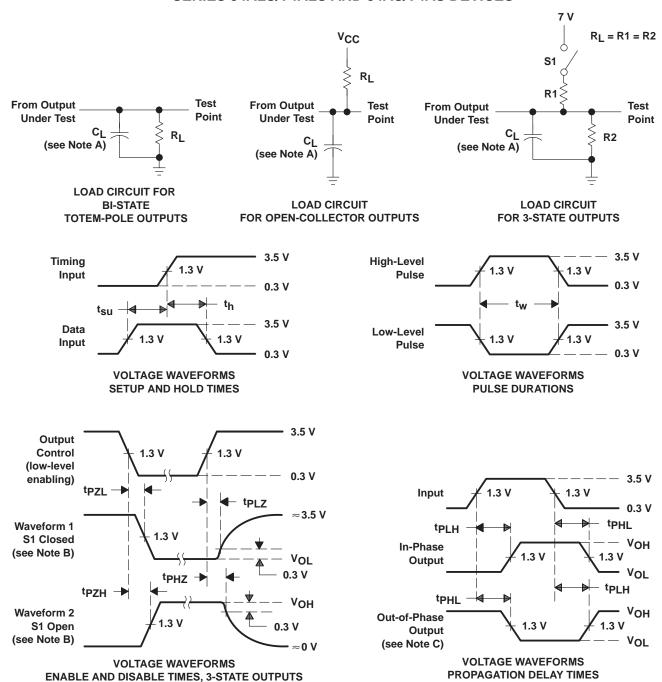
PARAMETER	FROM (OUTPUT)	TO (OUTPUT)	V _C (C _L R _L T _A	UNIT			
	(001101)	(001101)	SN54AL	S191A	SN74AL	ı	
			MIN	MAX	MIN	MAX	
f _{max}			20		30		MHz
t _{PLH}	I CAB	A O	7	37	7	30	
t _{PHL}	LOAD	Any Q	8	34	8	30	ns
t _{PLH}	4.5.0.5	A O	3	25	3	21	
t _{PHL}	A, B, C, D	Any Q	4	25	4	21	ns
t _{PLH}	011/	RCO	5	24	5	20	ns
^t PHL	CLK	RCO	5	25	5	20	
t _{PLH}	CLK	Any 0	3	26	3	18	20
t _{PHL}	CLK	Any Q	3	22	3	18	ns
t _{PLH}	OL K	A A A V/A AIA I	8	37	8	31	
t _{PHL}	CLK	MAX/MIN	8	34	8	31	ns
t _{PLH}			8	45	8	37	
^t PHL	D/Ū	RCO	10	36	10	28	ns
tPLH		A A A X/A AIA I	8	35	8	25	
t _{PHL}	D/Ū	MAX/MIN	8	30	8	25	ns
t _{PLH}	CTEN	RCO	4	21	4	18	ne
^t PHL	CIEN	KCO	4	23	4	18	ns

[§] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
- D. All input pulses have the following characteristics: PRR \leq 1 MHz, $t_{\Gamma} = t_{\Gamma} = 2$ ns, duty cycle = 50%.
- E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms







5-Sep-2011

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-86840012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-8684001EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Call TI	
5962-8684001FA	ACTIVE	CFP	W	16	1	TBD	Call TI	Call TI	
SN54ALS191AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SN74ALS191AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS191ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS191ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS191ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS191ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS191ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS191AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74ALS191ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SNJ54ALS191AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54ALS191AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SNJ54ALS191AW	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



PACKAGE OPTION ADDENDUM

5-Sep-2011

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54ALS191A, SN74ALS191A:

Catalog: SN74ALS191A

Military: SN54ALS191A

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

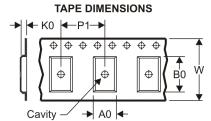
Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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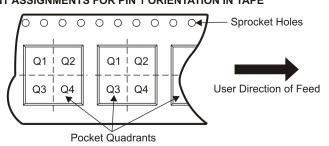
TAPE AND REEL INFORMATION





1	40	Dimension designed to accommodate the component width
		Dimension designed to accommodate the component length
ŀ	⟨0	Dimension designed to accommodate the component thickness
	W	Overall width of the carrier tape
T	P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS191ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

www.ti.com 23-Jul-2010



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS191ADR	SOIC	D	16	2500	333.2	345.9	28.6

14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC



FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



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